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H8/38602R Group

Data Communication with EEPROM in 4-Line Bus Communication Mode

Introduction

This application note discusses data communication with an EEPROM using 4-line bus communication mode of the synchronous serial communication unit (SSU).

Target Device

H8/38602R

HN58X2532I (EEPROM)

Contents

1. Specifications

- The H8/38602R communicates with an EEPROM by using the SSU in 4-line bus communication mode.
- In this sample task, the H8/38602R writes 32-byte data into the EEPROM and then reads the 32-byte data that have been written.
- The transfer clock rate is ϕ/16* (ϕ = 10 MHz).

Note: * The programs of this sample task can operate at a maximum transfer clock rate of ϕ/16. If the transfer clock rate is faster than ϕ/16, a transfer of one byte is completed before the transfer of the next byte becomes ready. This prevents the $\overline{SCS}$ pin from being fixed to the low level, and as such correct operation is unavailable.

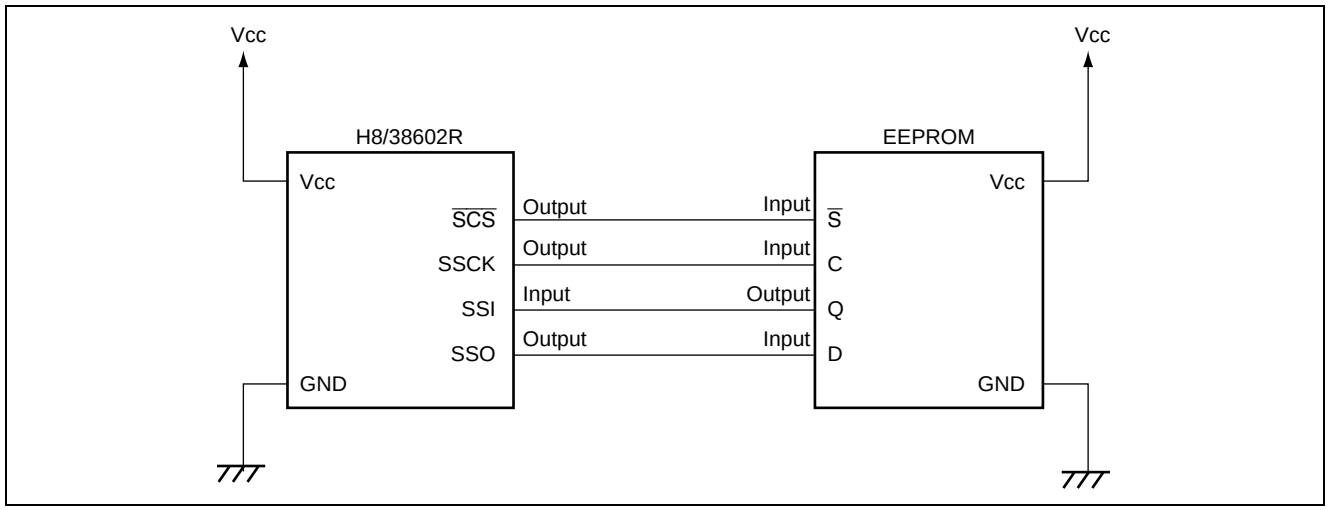


Figure 1 Connections in 4-Line Bus Communication Mode of SSU

2. Description of Functions

2.1 Functions

This sample task implements data communication with an EEPROM using the 4-line bus communication mode of the SSU incorporated in the H8/38602R. Figure 2 shows a block diagram of the SSU, and below is the functional explanation.

2.1.1 Functions of SSU in 4-Line Bus Communication Mode

The H8/38602R writes 32-byte data to the EEPROM and reads the 32-byte data, with a transfer clock rate of ϕ/16 (ϕ = 10 MHz).

- SS Control Register H (SSCRH)
  SSCRH is a register that selects whether the SSU operates as a master or slave device, and selects the functions of the SSCK and $\overline{\text{SCS}}$ pins.
- SS Control Register L (SSCRL)
  SSCRL is a register that selects the operating mode of the SSU.
- SS Mode Register (SSMR)
  SSMR is a register that selects MSB-first or LSB-first, and selects transfer clock rate.
- SS Enable Register (SSER)
  SSER is a register that enables transmit or receive operation.
- SS Status Register (SSSR)
  SSSR is a register that consists of interrupt flags.
- SS Receive Data Register (SSRDR)
  SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the data from SSTRSR to SSRDR. The SSTRSR is then ready to receive the next byte. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
- SS Transmit Data Register (SSTDR)
  SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR and then starts serial transmission. By writing the next transmit data to SSTDR during serial transmission of the data in SSTRSR, continuous serial transmission is possible. The initial value of SSTDR is H'00.
- SS Shift Register (SSTRSR)
  SSTRSR is a shift register used to transmit and receive serial data. When transmit data is transferred from SSTDR to SSTRSR, bit 0 in SSTDR is transferred to bit 0 in SSTRSR if the MLS bit in SSMR is 0 (LSB-first transfer), and bit 7 in SSTDR is transferred to bit 0 in SSTRSR if the MLS bit is 1 (MSB-first transfer). SSTRSR cannot be directly accessed by the CPU.

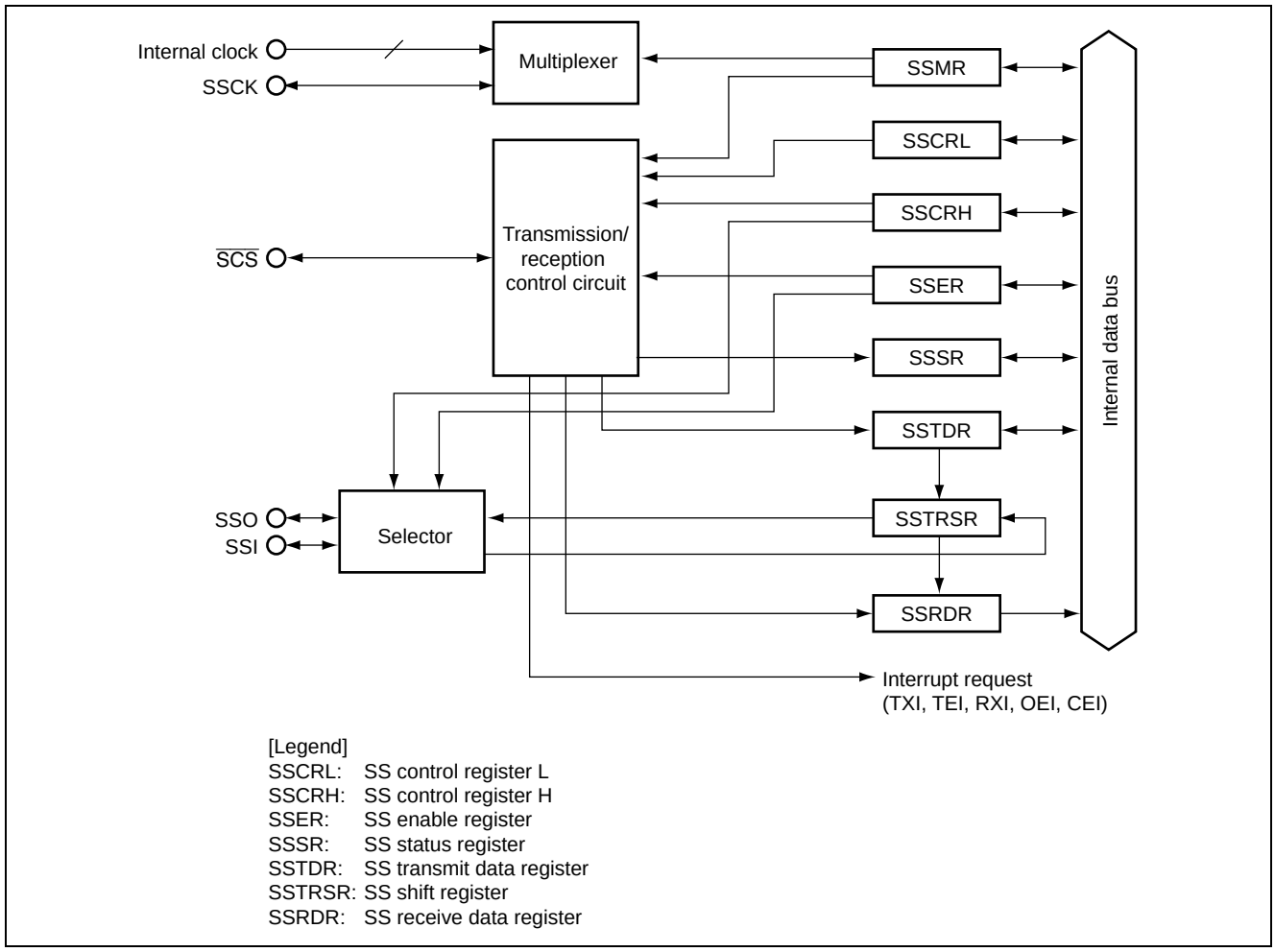


Figure 2 Block Diagram of SSU

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.3 Module Standby Function

The module standby function places the SSU in the module standby mode after the reset is released. The module standby mode can be cancelled by setting the SSUCKSTP bit of the clock halt register 2 (CKSTPR2) to 1.

- Clock Halt Register 2 (CKSTPR2)
  CKSTPR2 allows the on-chip peripheral modules to enter standby mode in module units.

2.2 Function Assignment

Assignment of the functions used in this sample task are listed in table 1. The H8/38602R communicates with an EEPROM using 4-line bus communication mode of the SSU by assigning the functions as shown in table 1.

Table 1 Assignment of Functions

Function	Category	Description
SSCK	Pin	SSU clock output
SSI	Pin	SSU data input
SSO	Pin	SSU data output
$\overline{\text{SCS}}$	Pin	SSU chip-select output
SSCRH	SSU	Selects master mode and selects the SSCK and $\overline{\text{SCS}}$ pin functions.
SSCRL	SSU	Selects 4-line bus communication mode.
SSMR	SSU	Selects MSB-first and a transfer clock rate of ϕ/16.
SSER	SSU	Enables data transmission or reception.
SSSR	SSU	Status flags
SSRDR	SSU	A register that stores received data
SSTDR	SSU	A register that stores transmit data
SSTRSR	SSU	A shift register used to transmit or receive data
CKSTPR2	Low power	Cancels module standby mode of the SSU.
TCSRWD1	WDT	Stops the watchdog timer.

3. Specifications of EEPROM

This chapter provides a brief description of the specifications of the EEPROM used for this sample task (HN58X2532). For detailed information, see the Renesas HN58X2532I/HN58X2564I series manual.

3.1 Pin Functions

- Serial Data Output (Q): Serial data is transmitted via this output pin. The output data changes at the rising edge of Serial Clock (C).
- Serial Data Input (D): Serial data is received via this input pin. It receives instruction codes, addresses, and data to be written. Values are latched at the rising edge of Serial Clock (C).
- Serial Clock (C): A clock signal is received via this input pin to provide timing of the serial interface. Instruction codes, addresses, or data to be written on the Serial Data Input pin is latched at the rising edge of Serial Clock (C). Data is output at the falling edge of Serial Clock (C).
- Chip Select ($\overline{S}$): This input pin is used to indicate that the device is selected. When this signal is high, the device is not selected and Serial Data Output (Q) is in a high impedance state. Unless an internal write cycle is in progress, the device will be in standby mode. Driving Chip Select ($\overline{S}$) low makes the device active. After power-up, a certain instruction code must be input when Chip Select ($\overline{S}$) is driven low.
- Hold ($\overline{HOLD}$): This pin is used to pause any serial communications with a device without deselecting the device. During the hold condition, Serial Data Output (Q) is in a high impedance state, and Serial Data Input (D) and Serial Clock (C) are don't care. During the hold condition, the device must be made active, with Chip Select ($\overline{S}$) driven low.
- Write Protect ($\overline{W}$): The main purpose of this input signal is to freeze the size of memory area that is protected against write instructions (as is specified by the BP1 and BP0 bits in the status register). This pin must be fixed to high or low during any write operation.

3.2 Status Register

Figure 3 shows the status register format. The Status Register can be read or written by specific instructions.

- WIP bit: The Write In Progress (WIP) bit indicates whether the memory device is busy with writing operation.
- WEL bit: This bit indicates the status of the internal Write Enable Latch.
- BP0 and BP1 bits: The Block Protect (BP1 and BP0) bits are used to set the size of the area to be software protected against write instructions. Since these bits are non-volatile, they retain information even after power is turned off.
- SRWD bit: The Status Register Write Disable (SRWD) bit operates in combination with the Write Protect ($\overline{W}$) signal. According to the states of the SRWD bit and the Write Protect ($\overline{W}$) signal, the device can be placed in Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits.

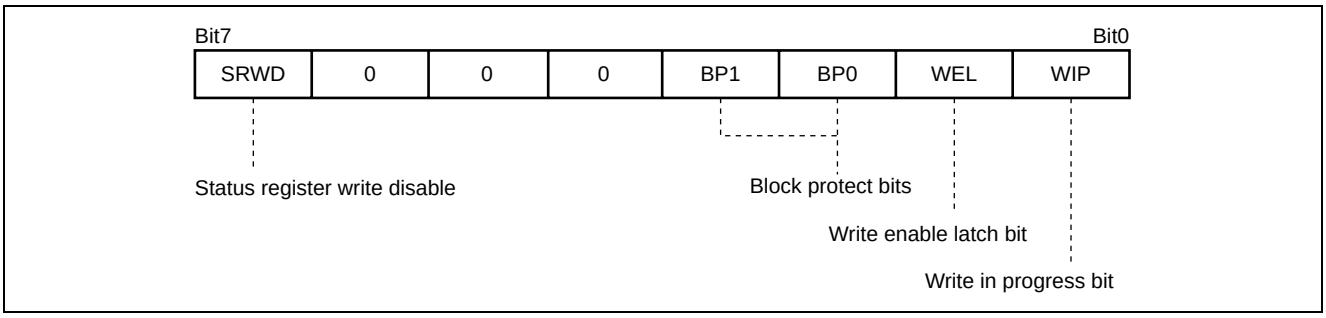


Figure 3 EEPROM Status Register Format

3.3 Instructions

Each instruction consists of a single-byte code, as summarized in Table 2. If an invalid instruction is received, the device is deselected (with the $\overline{S}$ pin driven high). This task uses the WREN, RDSR, READ and WRITE instructions.

Table 2 Instruction Codes

Instruction	Description	Instruction Code
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

3.3.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to data write operation (Write). The only way to do this is to send a Write Enable instruction to the memory device.

To send this instruction to the memory device, drive Chip Select ($\overline{S}$) low and input the instruction code to the Serial Data Input (D) pin. The WEL bit is set by deselecting the device with Chip Select ($\overline{S}$).

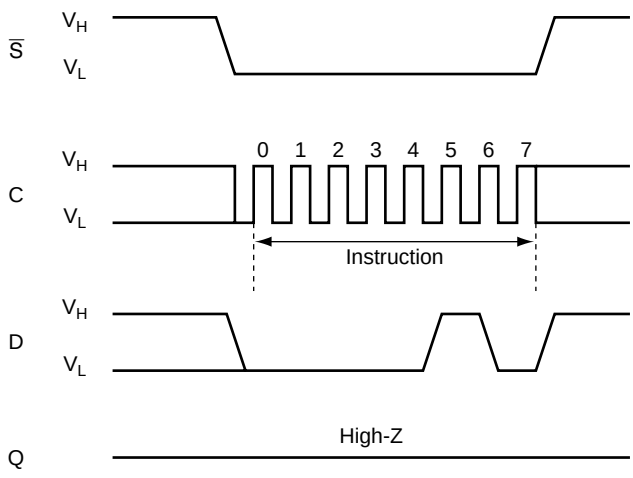


Figure 4 Write Enable (WREN) Sequence

3.3.2 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while the device is in writing operation. It is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. The Status Register is read continuously, as shown in the following figure.

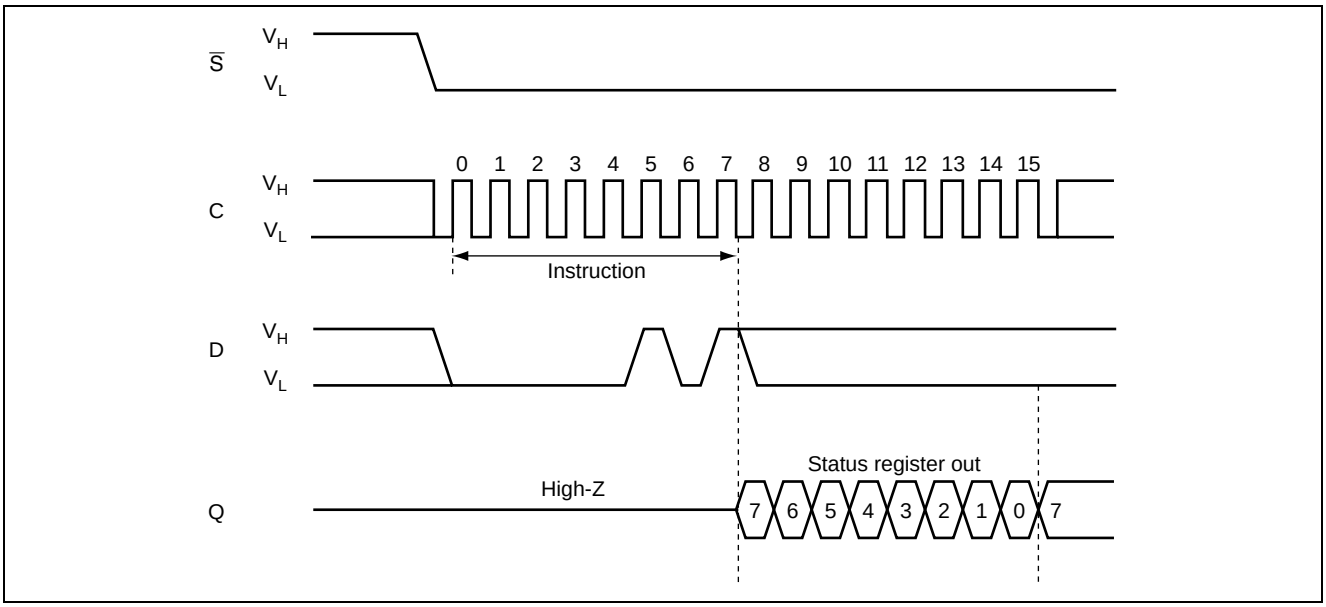


Figure 5 Read Status Register (RDSR) Sequence

The status and control bits of the Status Register are as follows:

- WIP bit: The Write In Progress (WIP) bit indicates whether the memory is busy with a WRITE or Write Status Register cycle. When this bit is set to 1, such a write cycle is in progress. When it is reset to 0, no such cycles are in progress.
- WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set. When cleared to 0, the internal Write Enable Latch is reset and no WRITE or Write Status Register instructions are accepted.
- BP0 and BP1 bits: The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against the Write to Memory Array (WRITE) instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits are set to 1, the relevant memory area (as defined in the Status Register Format table) becomes protected against the Write to Memory Array (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.
- SRWD bit: The Status Register Write Disable (SRWD) bit operates in combination with the Write Protect ($\overline{W}$) signal. The SRWD bit and the $\overline{W}$ signal allow the device to be placed in the Hardware Protected mode (when the SRWD bit is set to 1, and the $\overline{W}$ signal is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

3.3.3 Read from Memory Array (READ)

As shown in figure 6, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction and address bytes are then shifted in as Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out as Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented after 8 serial clock cycles, and the byte of data at the new address is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to be continued indefinitely.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The Chip Select ($\overline{S}$) signal can be driven high at any time during the cycle. The READ instruction is not accepted or is not executed if a write cycle is currently in progress.

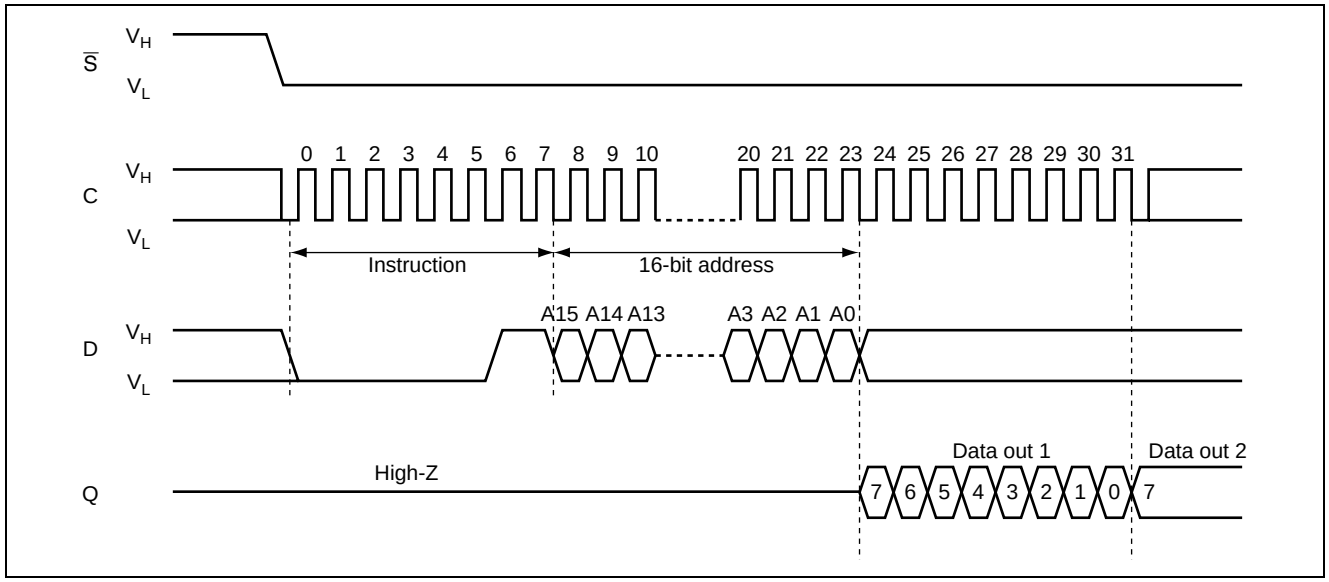


Figure 6 Read from Memory Array (READ) Sequence

Table 3 Address Range Bits

Device	HN58X2564I	HN58X2532I
Address bits	A12 to A0	A11 to A0

Notes: 1. b15-b13 are don't care on the HN582564.
2. b15-b12 are don't care on the HN582532.

3.3.4 Write to Memory Array (WRITE)

As shown in figure 7, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in on Serial Data Input (D).

The self-timed WRITE cycle is started by driving Chip Select ($\overline{S}$) high after the data byte has been latched in or before the next rising edge of the serial clock is input.

If Chip Select ($\overline{S}$) stays low and the next byte of input data is shifted in, as shown in figure 7, the device continues to receive data while incrementing the address counter towards the end of the same page as that specified by the given address. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data.

This instruction is not accepted or not executed under the following conditions:

- The Write Enable Latch (WEL) bit has not been set to 1. (WEL bit must be set immediately before the WRITE instruction)
- A Write cycle is already in progress
- The addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

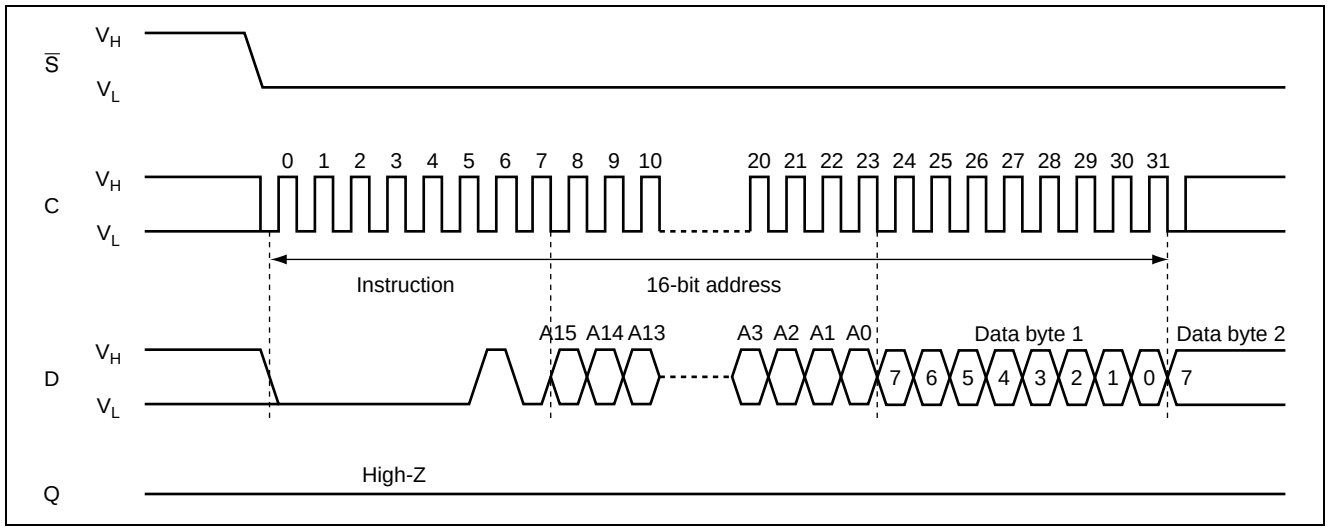


Figure 7 WRITE Sequence

4. Description of Operation

4.1 Transmit Mode

Figure 8 illustrates the operation timing in transmit mode for this sample task, with description of the hardware and software processing.

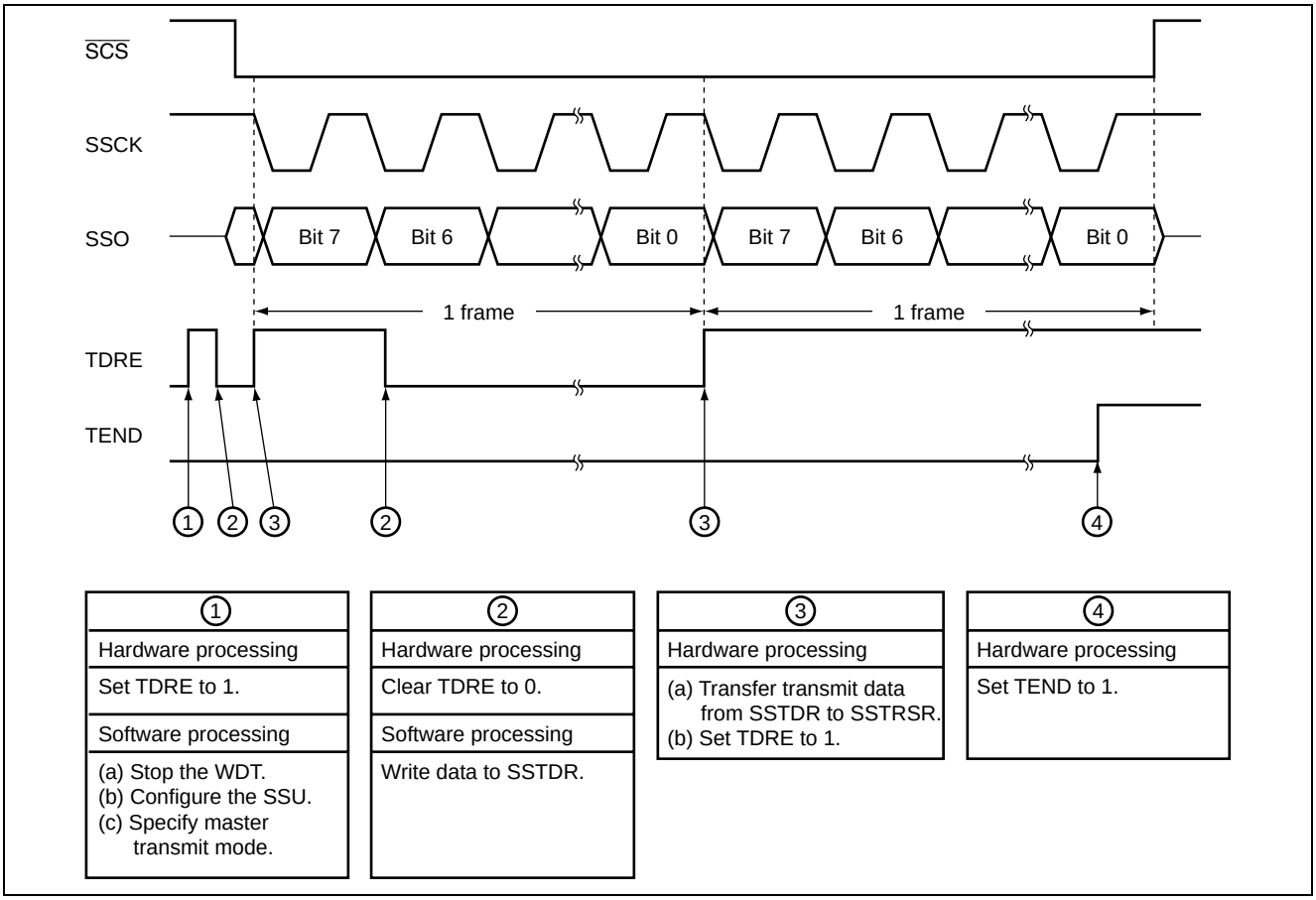


Figure 8 Timing of Operation in Transmit Mode

4.2 Transmit-and-Receive Mode

Figure 9 illustrates the operation timing in transmit-and-receive mode for this sample task, with description of the hardware and software processing.

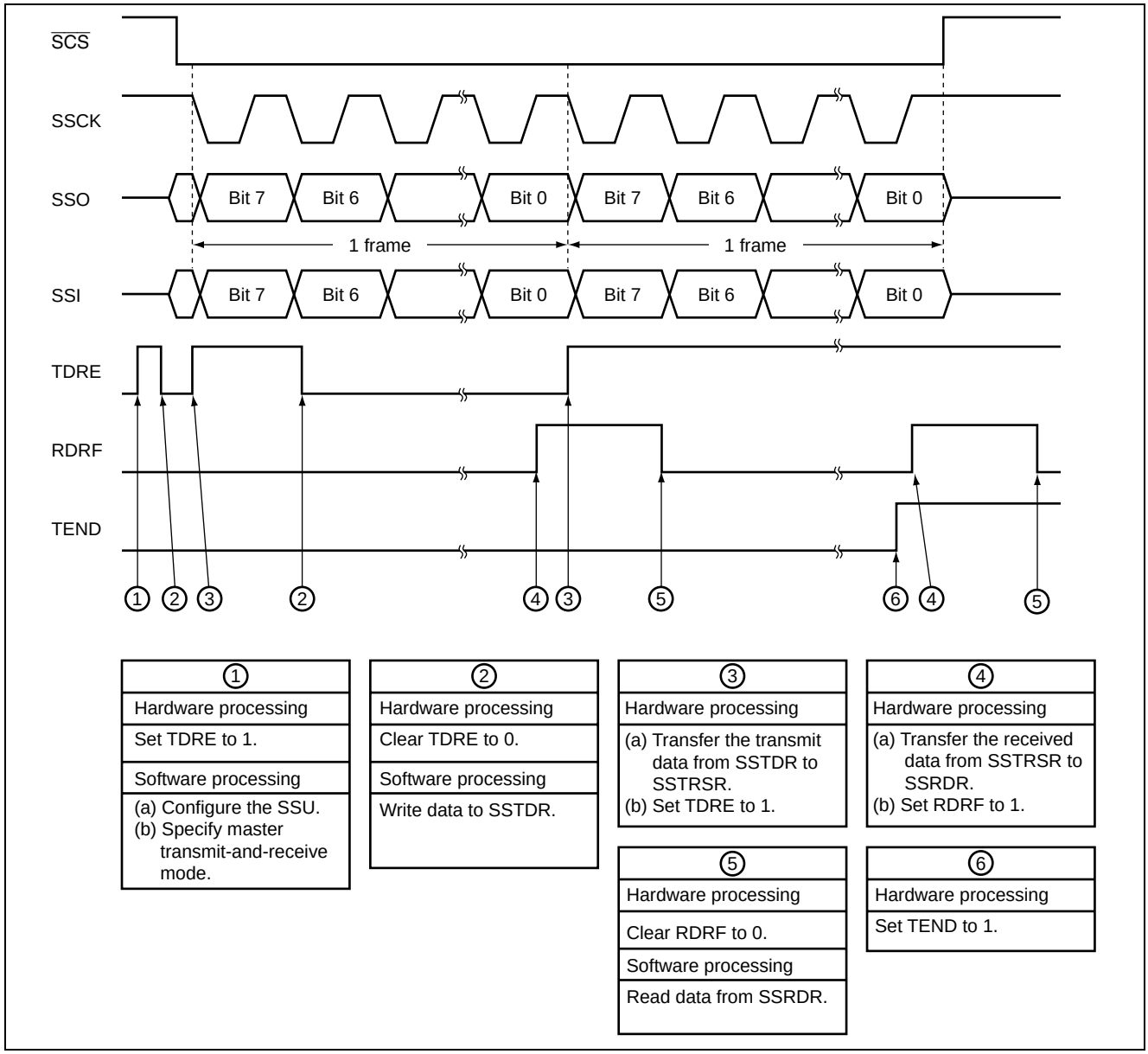


Figure 9 Timing of Operation in Transmit-and-Receive Mode

5. Description of Software

This sample task initializes the SSU in SPI mode (4-line bus communication mode) and performs processing for master transmission and master transmission/reception.

5.1 List of Functions

Table 4 lists the functions used in this sample task.

Table 4 List of Functions

Function Name	Description
main	Stops the watchdog timer, controls master transmission/reception, and initializes the RAM area to be used.
SSU_spi_int	Initializes the SSU in SPI mode and cancels module standby mode of the SSU.
select_movement	Selects the operating mode.
transmit	Transmit processing
receive	Receive processing

5.2 Constants

Table 5 lists the constants used in this sample task.

Table 5 Descriptions of Constants

Constant Name	Value	Description	Used In
SLAVE_ADRS	H'0000	Start address of EEPROM to be written or read	main
WREN	H'06	EEPROM write enable instruction	main
RDSR	H'05	Instruction to read the status register of EEPROM	main
READ	H'03	Instruction to read from EEPROM	main
WRITE	H'02	Instruction to write to EEPROM	main
WIP	H'01	Bit to indicate that a write to EEPROM is in progress	main
TR_RE	H'C0	Transmit-and-receive mode	main
TRANSMIT	H'80	Transmit mode	main
SIZE	H'20	Size of 1 page of EEPROM	main

5.3 RAM Usage

Table 6 describes the RAM usage in this sample task.

Table 6 Description of RAM

Label Name	Function	Data Length	Used In
m_trs[SIZE]	Buffer that stores transmit data	32 bytes	main
m_rcv[SIZE]	Buffer that stores received data	32 bytes	main

5.4 Description of Modules

5.4.1 main() Function

(1) **Module Specifications**

Function: Stops the watchdog timer, controls master transmission and reception and initializes the RAM area for use.

Table 7 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) **Internal Registers**

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from their initial values.

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation.
6	RE	0	R/W	Receive enable When this bit is 1, receive operation is enabled. 0: Disables receive operation.

- SS Status Register (SSSR) Address: H'F0E4

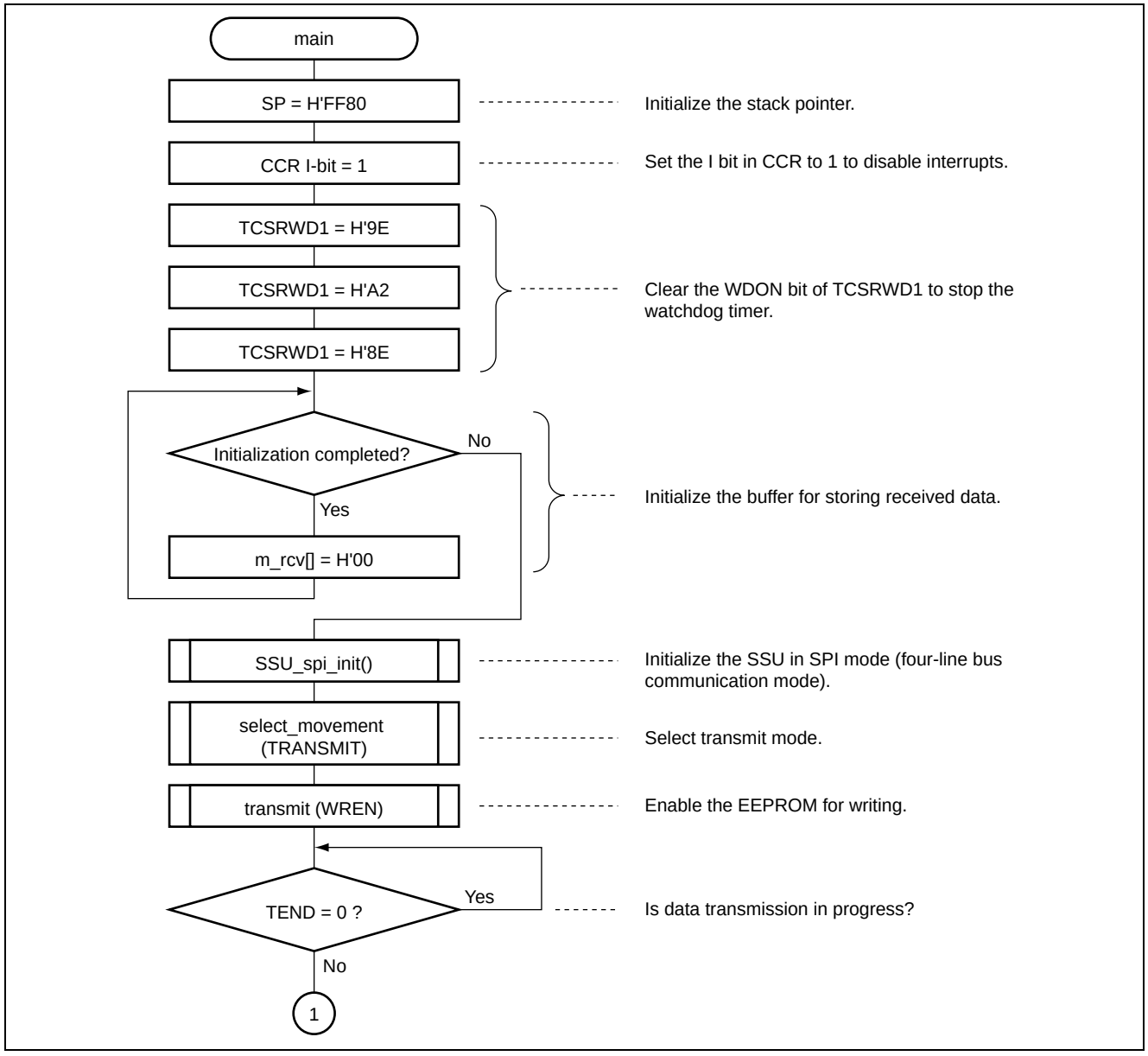
Bit	Bit Name	Setting	R/W	Function
3	TEND	—	R/(W)*	Transmit end [Setting condition] • When the last bit of data is transmitted with the TDRE bit set to 1. [Clearing conditions] • 0 is written to this bit after reading 1. • Data is written to SSTDR.

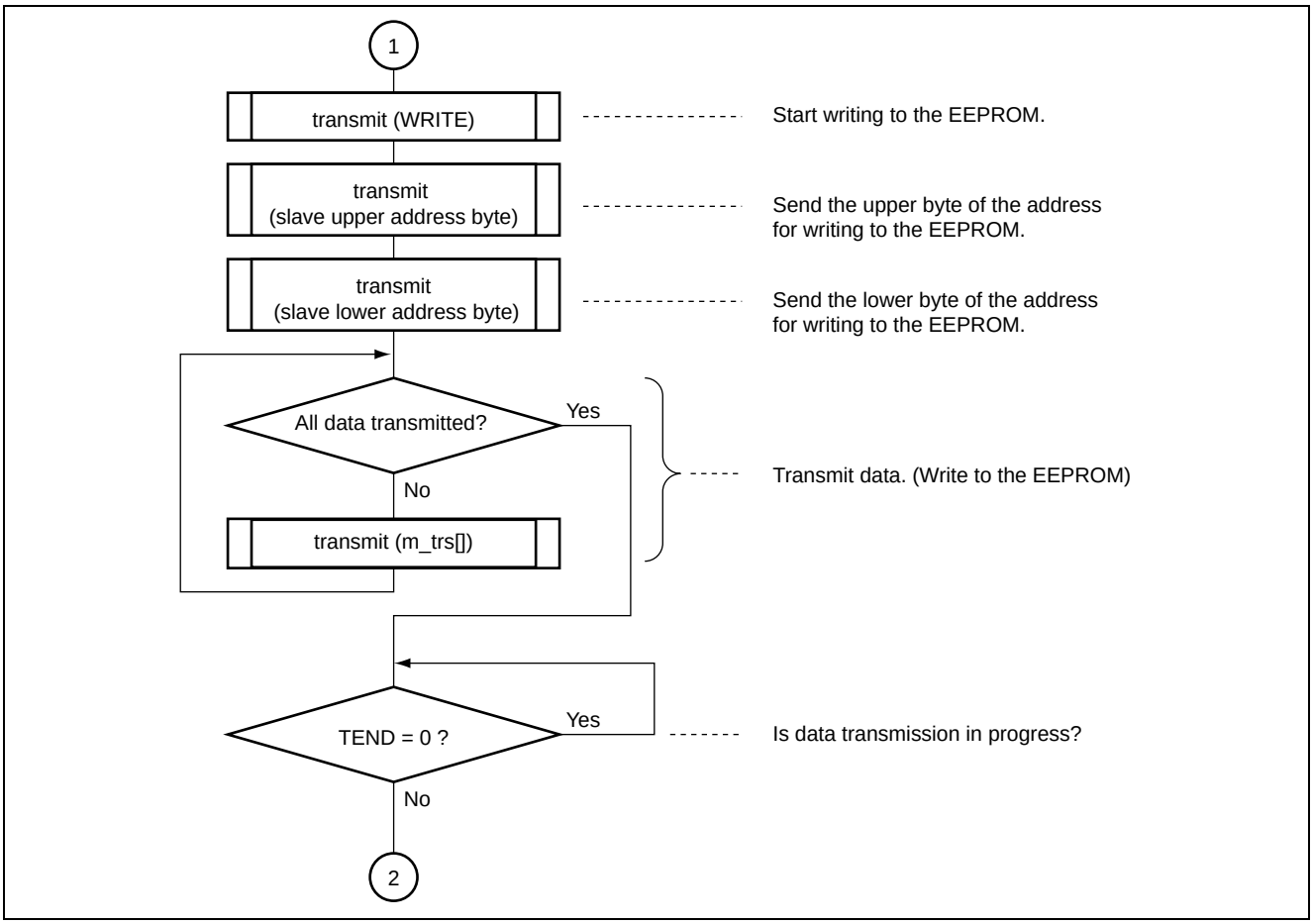
Note: Only 0 can be written to clear the flag.

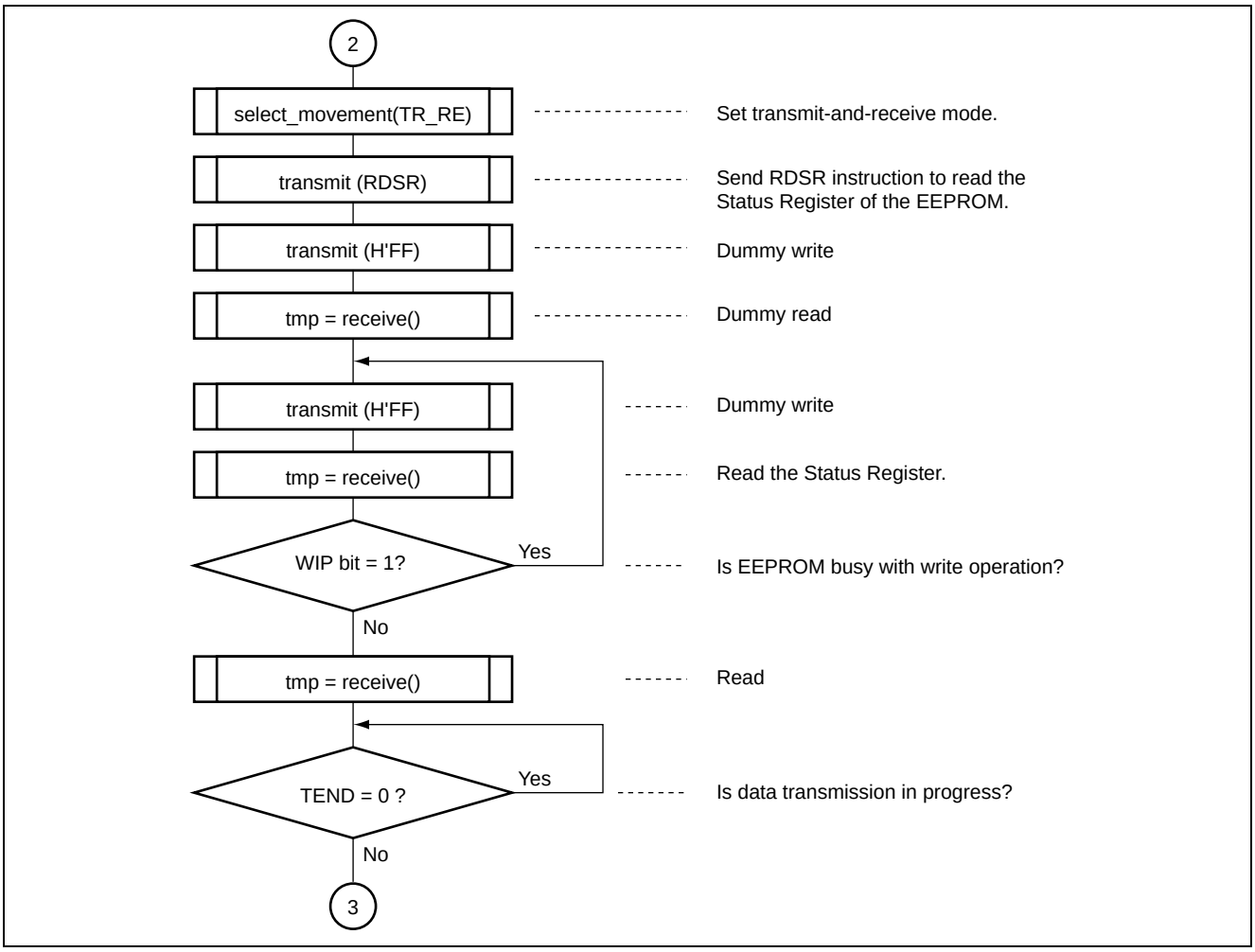
- Timer Control Register/Status Register WD1 (TCSRWD1) Address: H'FFB1

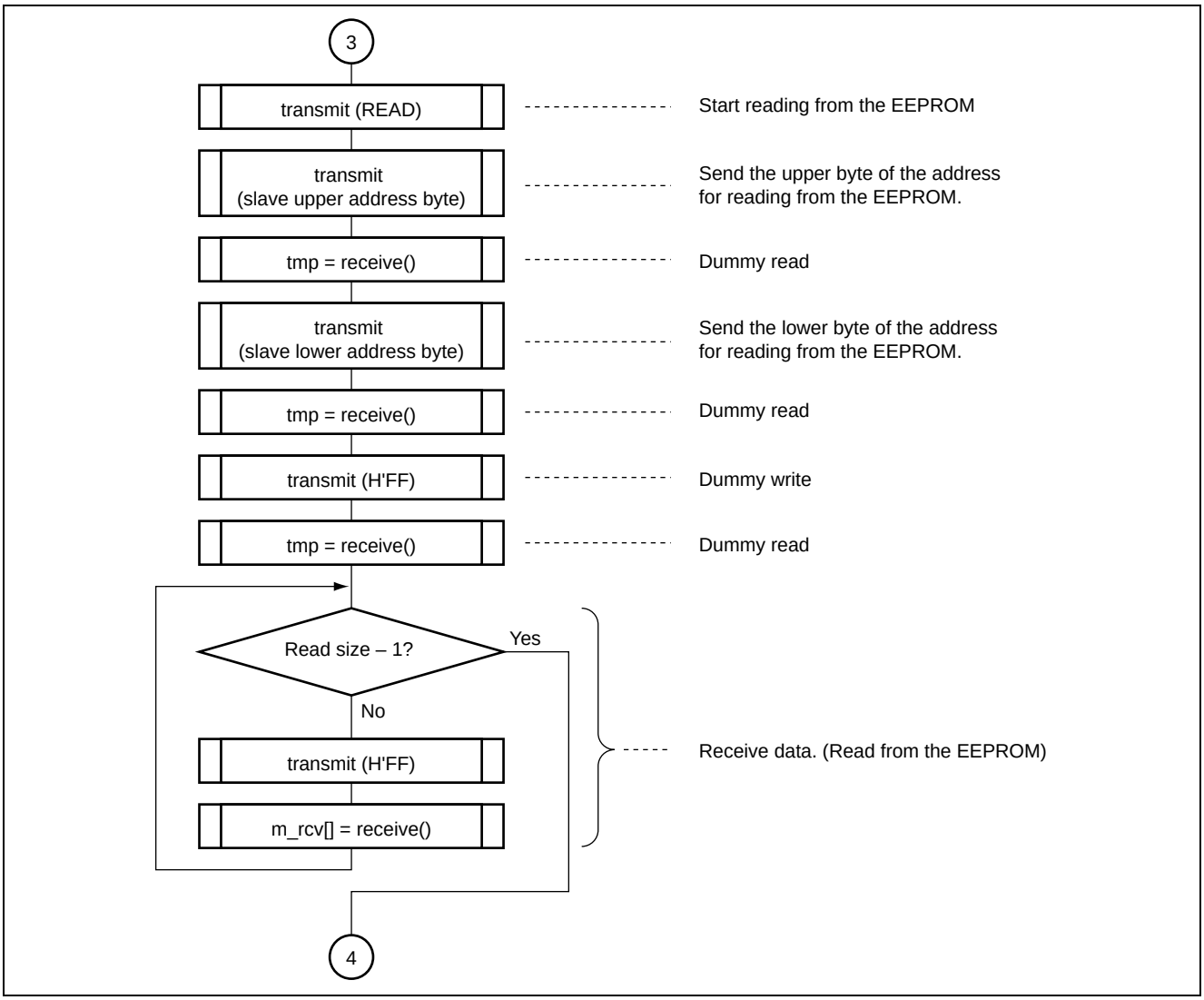
Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

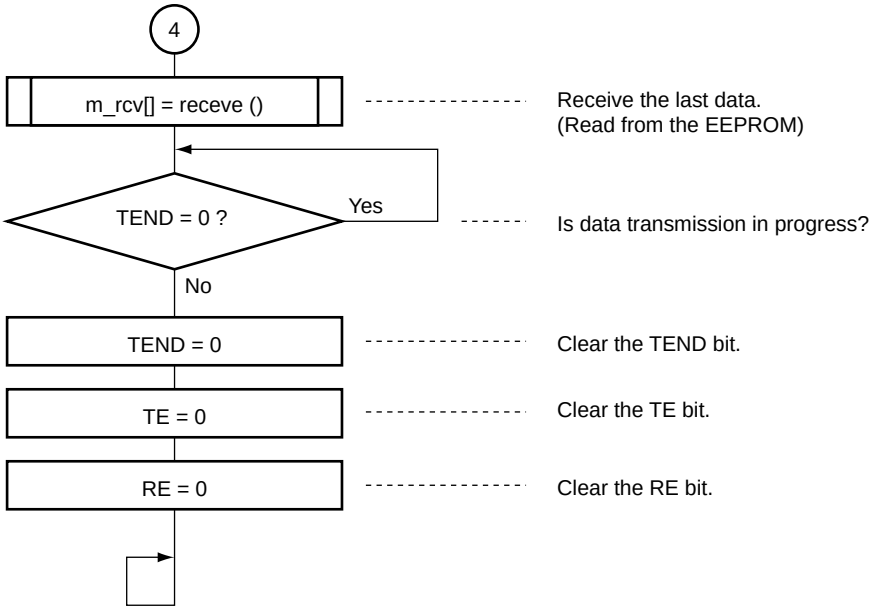
(3) **Flowchart**


main
SP = H'FF80
Initialize the stack pointer.
CCR I-bit = 1
Set the I bit in CCR to 1 to disable interrupts.
TCSRWD1 = H'9E
TCSRWD1 = H'A2
TCSRWD1 = H'8E
Clear the WDON bit of TCSRWD1 to stop the watchdog timer.
Initialization completed?
No
Yes
m_rcv[] = H'00
Initialize the buffer for storing received data.
SSU_spi_init()
Initialize the SSU in SPI mode (four-line bus communication mode).
select_movement (TRANSMIT)
Select transmit mode.
transmit (WREN)
Enable the EEPROM for writing.
TEND = 0 ?
Yes
No
Is data transmission in progress?
1


1
transmit (WRITE)
Start writing to the EEPROM.
transmit
(slave upper address byte)
Send the upper byte of the address
for writing to the EEPROM.
transmit
(slave lower address byte)
Send the lower byte of the address
for writing to the EEPROM.
All data transmitted?
Yes
No
transmit (m_trs[])
Transmit data. (Write to the EEPROM)
TEND = 0 ?
Yes
No
Is data transmission in progress?
2


2
select_movement(TR_RE)
Set transmit-and-receive mode.
transmit (RDSR)
Send RDSR instruction to read the Status Register of the EEPROM.
transmit (H'FF)
Dummy write
tmp = receive()
Dummy read
transmit (H'FF)
Dummy write
tmp = receive()
Read the Status Register.
WIP bit = 1?
Yes
Is EEPROM busy with write operation?
No
tmp = receive()
Read
TEND = 0 ?
Yes
Is data transmission in progress?
No
3


3
transmit (READ)
Start reading from the EEPROM
transmit
(slave upper address byte)
Send the upper byte of the address
for reading from the EEPROM.
tmp = receive()
Dummy read
transmit
(slave lower address byte)
Send the lower byte of the address
for reading from the EEPROM.
tmp = receive()
Dummy read
transmit (H'FF)
Dummy write
tmp = receive()
Dummy read
Read size – 1?
Yes
No
transmit (H'FF)
m_rcv[] = receive()
Receive data. (Read from the EEPROM)
4


4
m_rcv[] = receve ()
Receive the last data.
(Read from the EEPROM)
TEND = 0 ?
Yes
Is data transmission in progress?
No
TEND = 0
Clear the TEND bit.
TE = 0
Clear the TE bit.
RE = 0
Clear the RE bit.

5.4.2 SSU_spi_init() Function

(1) **Module Specifications**

Function: Initializes the SSU in SPI mode (4-line bus communication mode), and cancels SSU module standby mode.

Table 8 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) **Internal Registers**

The internal registers used in this sample task are described below. The setting values in the tables below are used for this task and are different from the initial values.

- SS Control Register H (SSCRH) Address: H'F0E0

Bit	Bit Name	Setting	R/W	Function
7	MSS	1	R/W	Master/Slave Device Select Selects whether this module is used as a master device or a slave device. When this module is used as a master device, transfer clock is output from the SSCK pin. When the CE bit in SSSR is set, the MSS bit is automatically cleared. 1: Operates as a master device
6	BIDE	0	R/W	Bidirectional Mode Enable Selects whether two pins are used as the serial data input pin and serial data output pin each or only one pin is used in bi-directional mode. 0: Normal mode. Two pins are used separately for data input and output.
2	SCKS	1	R/W	SSCK Pin Select Selects whether the SSCK pin functions as a port pin or a serial clock pin. 1: Functions as a serial clock pin.
1	CSS1	1	R/W	$\overline{\text{SCS}}$ Pin Select
0	CSS0	1	R/W	Selects whether the $\overline{\text{SCS}}$ pin functions as a port pin or as an $\overline{\text{SCS}}$ input or $\overline{\text{SCS}}$ output pin. CSS1 = 1, CSS0 = x: The $\overline{\text{SCS}}$ pin functions as an $\overline{\text{SCS}}$ output pin (however, functions as an $\overline{\text{SCS}}$ input before transfer is started).

[Legend] x: Don't care.

- SS Control Register L (SSCRL) Address: H'F0E1

Bit	Bit Name	Setting	R/W	Function
6	SSUMS	1	R/W	SSU Mode Select Selects which combination of the serial data input pin and serial data output pin is used. 1: Four-line bus communication mode When MSS = 1 and BIDE = 0 in SSCRH, data input: SSI pin, data output: SSO pin.

- SS Mode Register (SSMR) Address: H'F0E2

Bit	Bit Name	Setting	R/W	Function
7	MLS	1	R/W	MSB-First/LSB-First Select Selects whether data transfer is performed in MSB-first or LSB-first. 1: MSB-first
2	CKS2	1	R/W	Transfer Clock Rate Select
1	CKS1	0	R/W	Sets transfer clock rate (prescaler division ratio) when the internal clock is selected. Table 9 shows the transfer rate.
0	CKS0	0	R/W	CKS2 = 1, CKS1 = 0, CKS0 = 0: ϕ/16

Table 9 Transfer Rate

Bit 2	Bit 1	Bit 0		Transfer Rate
CKS2	CKS1	CKS0	Clock	ϕ = 10 MHz
1	0	0	ϕ/16	625 kHz

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation.
6	RE	0	R/W	Receive Enable When this bit is 1, receive operation is enabled. 0: Disables receive operation.

- SS Status Register (SSSR) Address: H'F0E4

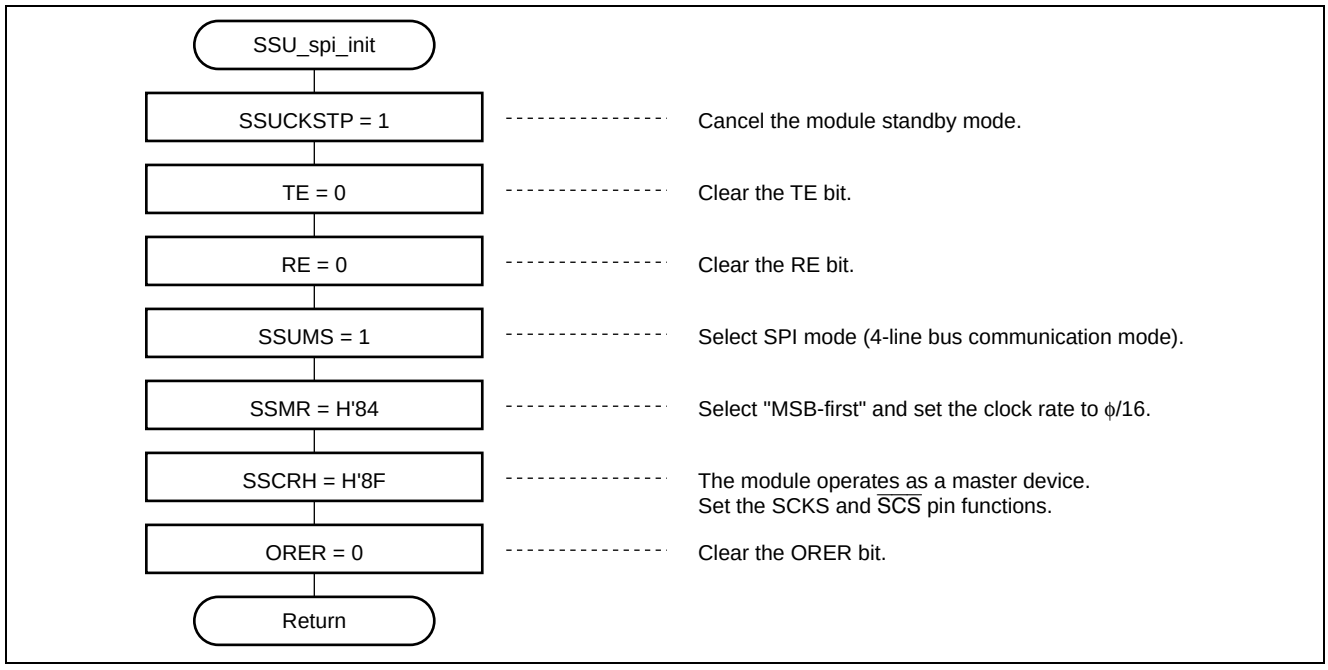
Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.

Note: Only 0 can be written to clear the flag.

- Clock Halt Register (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Setting	R/W	Function
4	SSUCKSTP	0	R/W	SSU Module Standby SSU enters module standby mode when this bit is cleared to 0. 1: Cancels the SSU module standby mode

(3) **Flowchart**



5.4.3 select_movement() Function

(1) **Module Specifications**

Function: Selects the operating mode.

Table 10 Module Specifications

Item	Type	Variable Name	Description
Argument	unsigned char	mode	Operating mode to be selected

(2) **Internal Registers**

The internal registers used in this sample task are described below. The setting values in the tables below are used for this task and are different from the initial values.

- SS Enable Register (SSMR) Address: H'F0E3

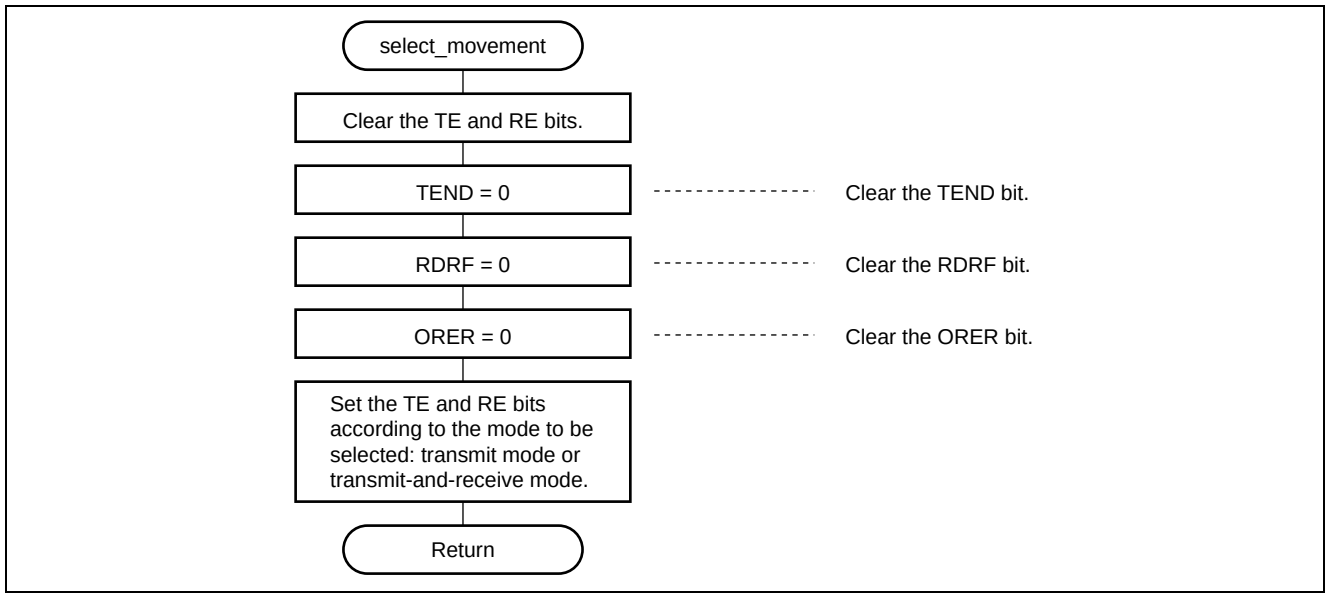
Bit	Bit Name	Setting	R/W	Function
7	TE	Argument	R/W	Transmit Enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation. 1: Enables transmit operation.
6	RE	Argument	R/W	Receive Enable When this bit is 1, receive operation is enabled. 0: Disables receive operation. 1: Enables receive operation.

- SS Status Register (SSSR) Address: H'F0E4

Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
3	TEND	0	R/(W)*	Transmit end [Setting condition] • When the last bit of data is transmitted with the TDRE bit set to 1. [Clearing conditions] • 0 is written to this bit after reading 1. • Data is written to SSTDR.
1	RDRF	0	R/(W)*	Receive Data Register Full [Setting condition] • When serial reception ended normally and the received data is transferred from SSTRSR to SSRDR. [Clearing conditions] • When 0 is written to this bit after reading 1. • When data is read from SSRDR.

Note: * Only 0 can be written to clear the flag.

(3) **Flowchart**



5.4.4 transmit() Function

(1) **Module Specifications**

Function: Transmit processing

Table 11 Module Specifications

Item	Type	Variable Name	Description
Argument	unsigned char	trs_data	Transmit data

(2) **Internal Registers**

The internal registers used in this sample task are described below. The setting values in the tables below are used for this task and are different from the initial values.

- SS Status Register (SSMR) Address: H'F0E4

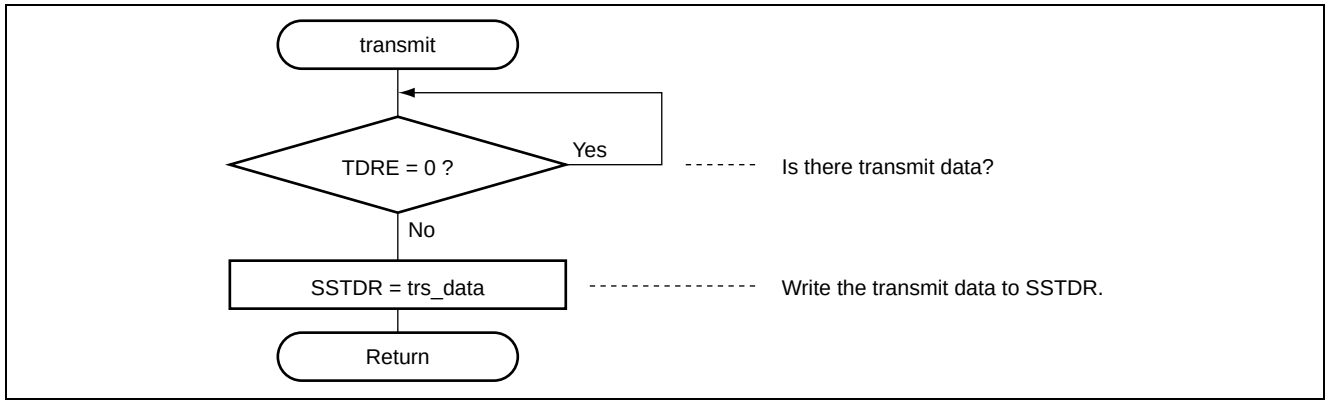
Bit	Bit Name	Setting	R/W	Function
2	TDRE	indefinite	R/(W)*	Transmit Data Empty [Setting condition] • When the TE bit in SSER is 0. • When the data in SSTDR is transferred to SSTRSR, and writing to SSTDR has become possible. [Clearing conditions] • When 0 is written to this bit after reading 1. • When data is written to SSTDR.

Note: Only 0 can be written to clear the flag.

- SS Transmit Data Register (SSTDR) Address: H'F0EB

Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R/W	SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read from or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR to start serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, continuous serial transmission is possible. The initial value of SSTDR is H'00.
6	bit6	—	R/W	
5	bit5	—	R/W	
4	bit4	—	R/W	
3	bit3	—	R/W	
2	bit2	—	R/W	
1	bit1	—	R/W	
0	bit0	—	R/W	

(3) **Flowchart**



5.4.5 receive() Function

(1) **Module Specifications**

Function: Receive processing

Table 12 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None
Return value	unsigned char	—	Received data

(2) **Internal Registers**

The internal registers used in this sample task are described below. The setting values in the tables below are used for this task and are different from the initial values.

- SS Status Register (SSMR) Address: H'F0E4

Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.

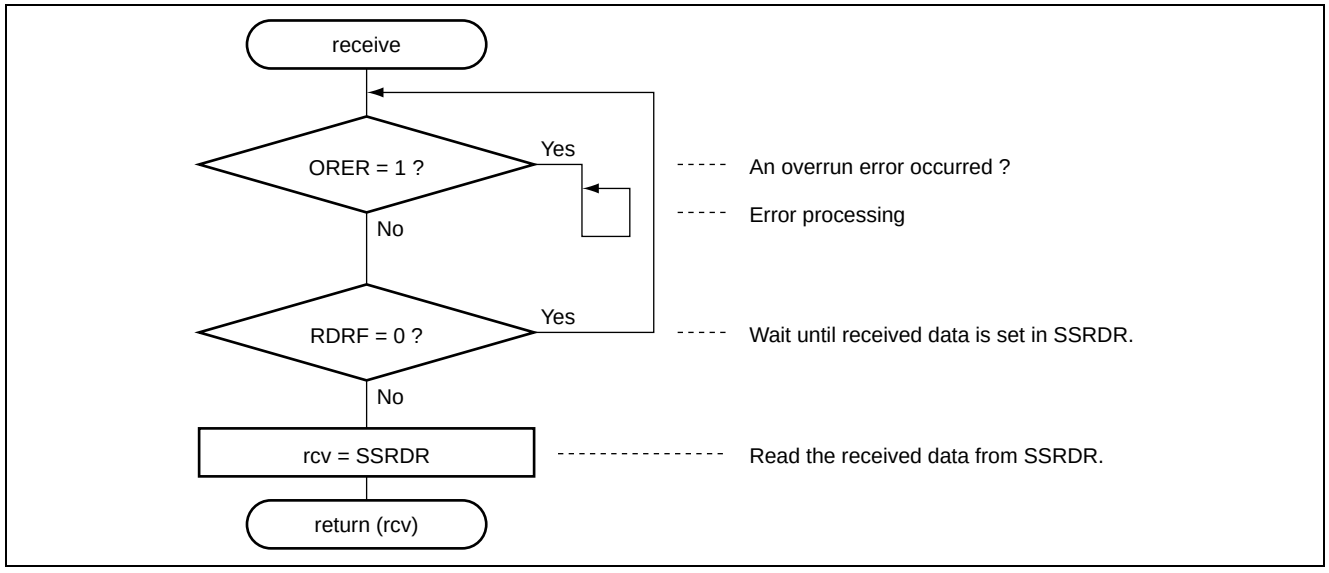
Bit	Bit Name	Setting Value	R/W	Function
1	RDRF	0	R/(W)*	Receive Data Register Full [Setting condition] • When serial reception ended normally and the received data is transferred from SSTRSR to SSRDR. [Clearing conditions] • When 0 is written to this bit after reading 1. • When data is read from SSRDR.

Note: * Only 0 can be written to clear the flag.

- SS Receive Data Register (SSRDR) Address: H'F0E9

Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

(3) **Flowchart**



5.5 Link Addressing

Section name	Address
CVECT	H'0000
P	H'0100
D,B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

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