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## H8/38602R Group

### Counting Seconds by Using Timer B1

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#### Introduction

A second counter is implemented by using Timer B1. The second counter is placed in on-chip RAM in BCD representation, and the input clock source of Timer B1 is a subclock of 38.4 kHz.

#### Target Device

H8/38602R

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### 1. Specifications

The auto-reload function of Timer B1 is used to count seconds with the input of a  $\phi_w$ -derived clock. Using  $\phi_w/256$  as the input clock of timer counter B1 (TCB1), an interrupt is generated every second by the auto-reload function to increment the second counter in on-chip RAM. The second counter counts up from 00 to 59 seconds with the counter value represented in BCD code. Figure 1 shows a block diagram of counting seconds using Timer B1. This sample task uses a 38.4 kHz crystal oscillator to generate the subclock.

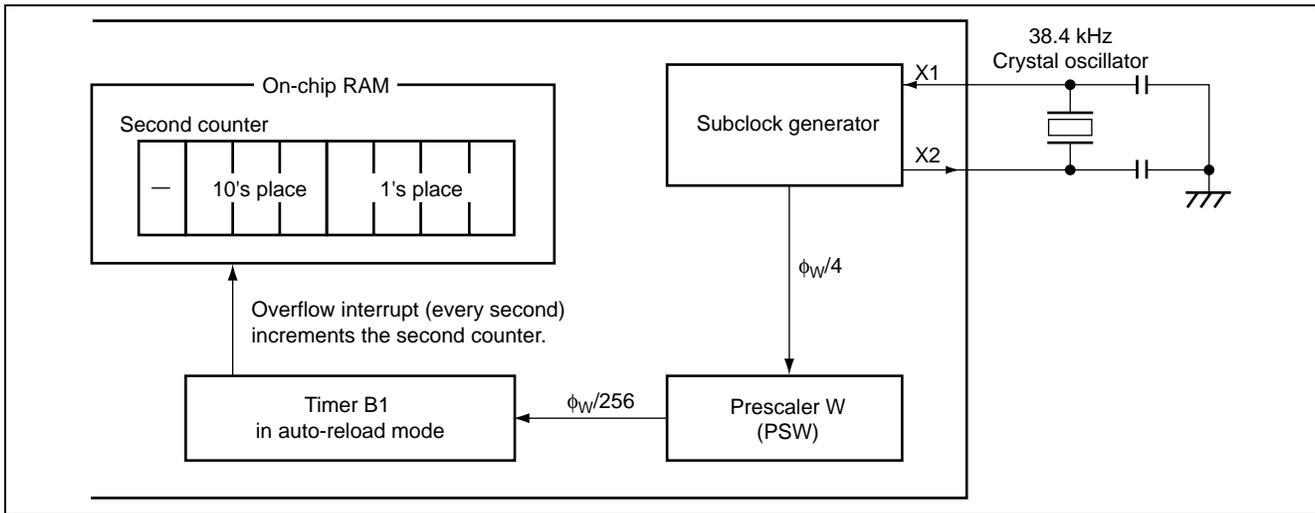


Figure 1 Counting Seconds Using Timer B1

## 2. Description of Functions

### 2.1 Functions

This sample task uses the auto-reload function of Timer B1 to generate an interrupt every second to increment the BCD second counter in on-chip RAM. The functions used by this sample task are described below.

#### 2.1.1 Timer B1 Auto-Reload Function

The auto-reload function uses the subclock of  $\phi w/256$  to cause timer counter B1 (TCB1) to overflow every second. Figure 2 shows a block diagram of the auto-reload function of Timer B1.

- **Timer Mode Register B1 (TMB1)**  
TMB1 selects whether Timer B1 operates in interval timer mode or auto-reload mode, starts/stops the counter, and selects the input clock of timer counter B1 (TCB1).
- **Timer Counter B1 (TCB1)**  
TCB1 is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock input to this counter is selected by the TMB12 to TMB10 bits in TMB1. When TCB1 overflows (H'FF → H'00 or H'FF → setting value of TLB1), the IRRTB1 flag in Interrupt Flag Register 2 (IRR2) is set to 1. TCB1 is allocated to the same address as TLB1. The initial value of TCB1 is H'00.
- **Timer Load Register (TLB1)**  
TLB1 is an 8-bit write-only register that sets the reload value of TCB1. Writing the reload value to TLB1 must be done while the TMB16 bit in TMB1 is 0. When a reload value is written to TLB1, the same value is set in TCB1 as well, and TCB1 starts counting up from that value. When TCB1 overflows during auto-reload operation, the TLB1 value is loaded into TCB1. Accordingly, the overflow period can be set in the range of 1 to 256 input clock cycles. TLB1 is allocated to the same address as TCB1. The initial value of TLB1 is H'00.

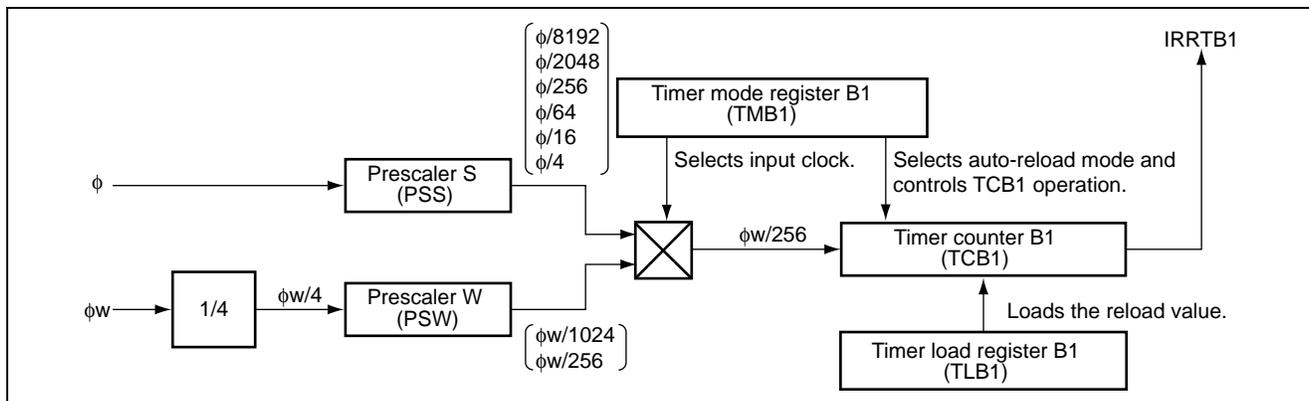


Figure 2 Block Diagram of Timer B1 Auto-Reload Function

#### 2.1.2 Module Standby Function

By the module standby function, Timer B1 is placed in module standby mode after a reset. Module standby mode of Timer B1 can be cancelled by setting the TB1CKSTP bit in Clock Halt Register 1 (CKSTPR1) to 1.

- **Clock Halt Register 1 (CKSTPR1)**  
CKSTPR1 is used to place the on-chip peripheral modules in standby mode in module units.

### 2.1.3 Watchdog Timer Function

The H8/38602R includes a watchdog timer, which is active after a reset. The timer counter WD (TCWD) counts up, and the H8/38602R is internally reset if the TCWD overflows. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)  
TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. The setting value cannot be changed by bit manipulation instructions.

### 2.1.4 Exception Handling Function

This sample task increments the second counter by the interrupt processing routine for the Timer B1 overflow interrupt, which is generated every second.

- Interrupt Enable Register 2 (IENR2)  
IENR2 is used to enable Timer B1 interrupt requests.
- Interrupt Flag Register 2 (IRR2)  
IRR2 includes the status flag of Timer B1 interrupt request.

## 2.2 Example of Calculating Reload Value for Timer B1

The reload value that is set in TLB1 of Timer B1 is calculated in the following way:

$$\text{TCB1 Overflow Period} = \text{TCB1 Input Clock Period} \times (256 - \text{TLB1 setting value}) \dots (1)$$

In this sample task, the TCB overflow period is 1 second and the TCB1 input clock is  $\phi_w/256$ . From the formula (1), we can obtain:

$$\begin{aligned} 1 &= (1 / (38400 / 256)) \times (256 - \text{TLB1 setting value}) \\ 256 - \text{TLB1 setting value} &= 38400 / 256 \\ \text{TLB setting value} &= 256 - 150 = 106 \end{aligned}$$

Accordingly, 106 (H'6A) is written to TLB1 in this sample task.

## 2.3 Function Assignment

Table 1 shows the assignment of functions used in this sample task. The second counter is implemented using Timer B1 by assigning the functions as shown in table 1.

**Table 1 Functions Assignment**

Function	Description
TMB1	Selects the auto-reload mode, controls the counter operation, and selects the clock input to the TCB1.
TCB1	8-bit up-counter with the input clock of $\phi_w/4$
TLB1	Sets the reload value for TCB1.
CKSTPR1	Cancels module standby mode of Timer B1.
TCSRWD1	Stops the watchdog timer.
IENR2	Enables Timer B1 interrupt requests.
IRR2	Indicates the status of Timer B1 interrupt request.

### 3. Description of Operation

This sample task uses the auto-reload function of Timer B1 with the input of a subclock to increment the BCD second counter in on-chip RAM by generating an interrupt every second. Figure 3 illustrates the operation of counting seconds using Timer B1.

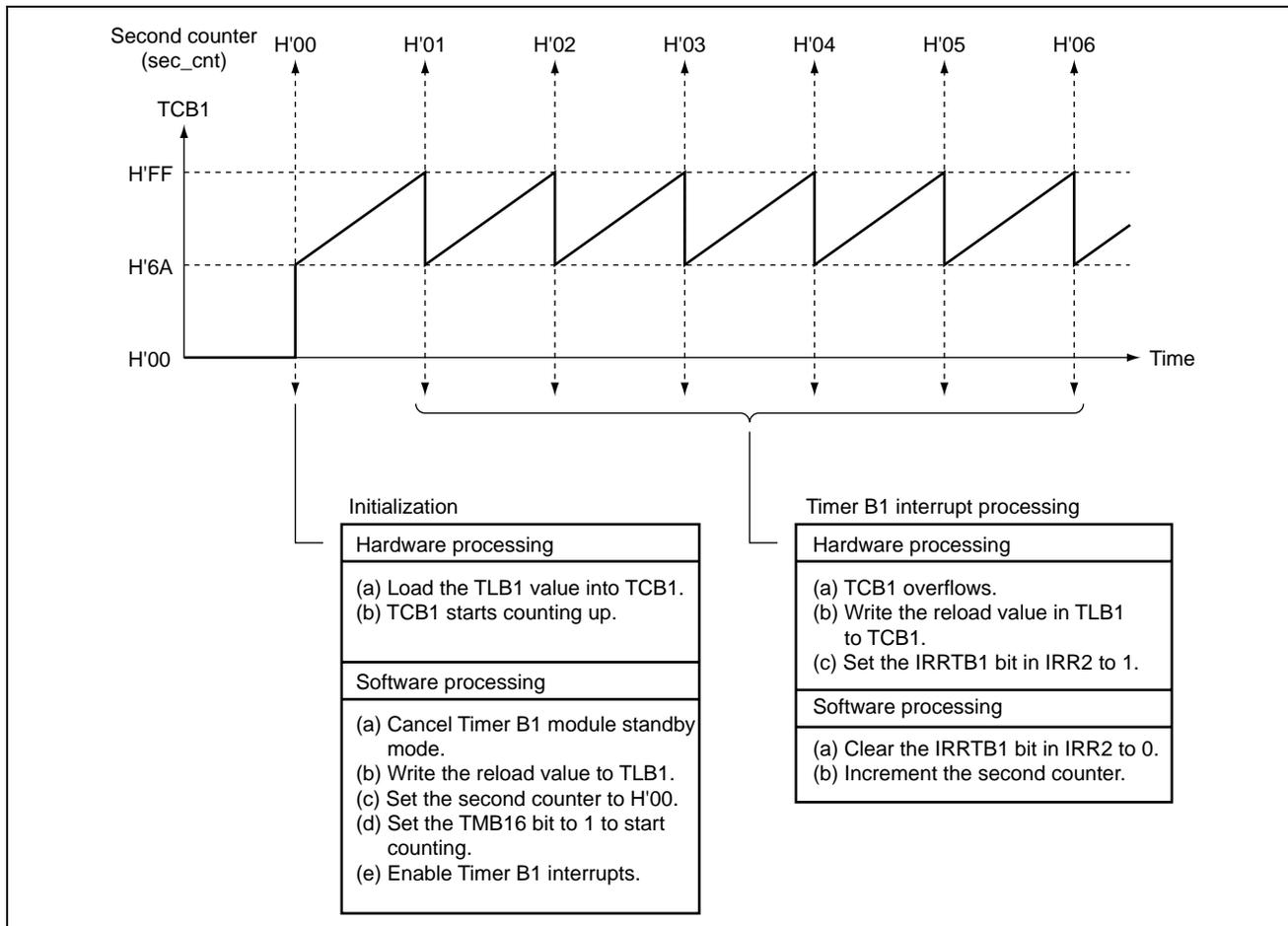


Figure 3 Operation Timing

## 4. Description of Software

### 4.1 Modules

Table 2 lists the modules used in this sample task.

**Table 2 Description of Modules**

Function Name	Description
main	Stops the watchdog timer, cancels Timer B1 module standby mode, initializes Timer B1 and RAM area to be used, and controls Timer B1 counting operation and interrupts.
int_tmb1	Timer B1 interrupt processing
cnt_up	Increments the second counter in on-chip RAM (sec_cnt).

### 4.2 Arguments

This sample task does not use any arguments.

### 4.3 Internal Registers Used

The internal registers used in this sample task are described below.

- Timer Mode Register B1 (TMB1) Address: H'F0D0

Bit	Bit Name	Setting	R/W	Function
7	TMB17	1	R/W	Auto-reload Function Select 0: Interval timer function selected. 1: Auto-reload function selected.
6	TMB16	1	R/W	Counter Operation/Stop Select 0: Counter stops. 1: Counter operates.
2	TMB12	1	R/W	Counter Clock Select
1	TMB11	1	R/W	000: internal clock $\phi/8129$
0	TMB10	1	R/W	001: internal clock $\phi/2048$ 010: internal clock $\phi/256$ 011: internal clock $\phi/64$ 100: internal clock $\phi/16$ 101: internal clock $\phi/4$ 110: internal clock $\phi_w/1024$ 111: internal clock $\phi_w/256$

• Timer Counter B1 (TCB1)

Address: H'F0D1

Bit	Bit Name	Setting	R/W	Function
7	TCB17	0	R	TCB1 is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock input to this counter is selected by bits TMB12 to TMB10 in TMB1. When TCB1 overflows (H'FF → H'00 or H'FF → setting value of TLB1), the IRRTB1 flag in Interrupt Flag Register 2 (IRR2) is set to 1. TCB1 is allocated to the same address as TLB1. The initial value of TCB1 is H'00.
6	TCB16	0	R	
5	TCB15	0	R	
4	TCB14	0	R	
3	TCB13	0	R	
2	TCB12	0	R	
1	TCB11	0	R	
0	TCB10	0	R	

• Timer Load Register B1 (TLB1)

Address: H'F0D1

Bit	Bit Name	Setting	R/W	Function
7	TLB17	0	W	TLB1 is an 8-bit write-only register that sets the reload value of TCB1. Writing the reload value to TLB1 must be done while the TMB16 bit in TMB1 is 0. When a reload value is written to TLB1, the same value is set in TCB1 as well, and TCB1 starts counting up from that value. When TCB1 overflows during auto-reload operation, the TLB1 value is loaded into TCB1. Accordingly, the overflow period can be set in the range of 1 to 256 input clock cycles. TLB1 is allocated to the same address as TCB1. The initial value of TLB1 is H'00. TLB1 setting value = H'6A (106)
6	TLB16	1	W	
5	TLB15	1	W	
4	TLB14	0	W	
3	TLB13	1	W	
2	TLB12	0	W	
1	TLB11	1	W	
0	TLB10	0	W	

• Clock Halt Register 1 (CKSTPR1)

Address: H'FFFA

Bit	Bit Name	Setting	R/W	Function
2	TB1CKSTP	1	R/W	Timer B1 Module Standby 0: Timer B1 is placed in module standby state. 1: Timer B1 module standby state is canceled

- Timer Control Register/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4WI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] <ul style="list-style-type: none"> <li>• If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1.</li> <li>• Reset</li> </ul> [Clearing condition] <ul style="list-style-type: none"> <li>• If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.</li> </ul>
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] <ul style="list-style-type: none"> <li>• When the TCWD overflows and an internal reset signal is generated.</li> </ul> [Clearing condition] <ul style="list-style-type: none"> <li>• Reset by the <math>\overline{\text{RES}}</math> pin</li> <li>• If 0 is written to both the B0WI and WRST bits while the TCSRWE bit is 1.</li> </ul>

- Interrupt Enable Register 2 (IENR2) Address: H'FFF4

Bit	Bit Name	Setting	R/W	Function
2	IENRB1	1	R/W	Timer B1 Interrupt Request Enable Setting this bit to 1 enables Timer B1 interrupt requests.

- Interrupt Flag Register 2 (IPR2) Address: H'FFF7

Bit	Bit Name	Setting	R/W	Function
2	IRRTB1	0	R/W	Timer B1 Interrupt Request Flag [Setting condition] <ul style="list-style-type: none"> <li>• When Timer B1 overflows</li> </ul> [Clearing condition] <ul style="list-style-type: none"> <li>• When 0 is written to this bit</li> </ul>

#### 4.4 RAM Usage

Table 3 describes the RAM usage in this sample task.

**Table 3 Description of RAM**

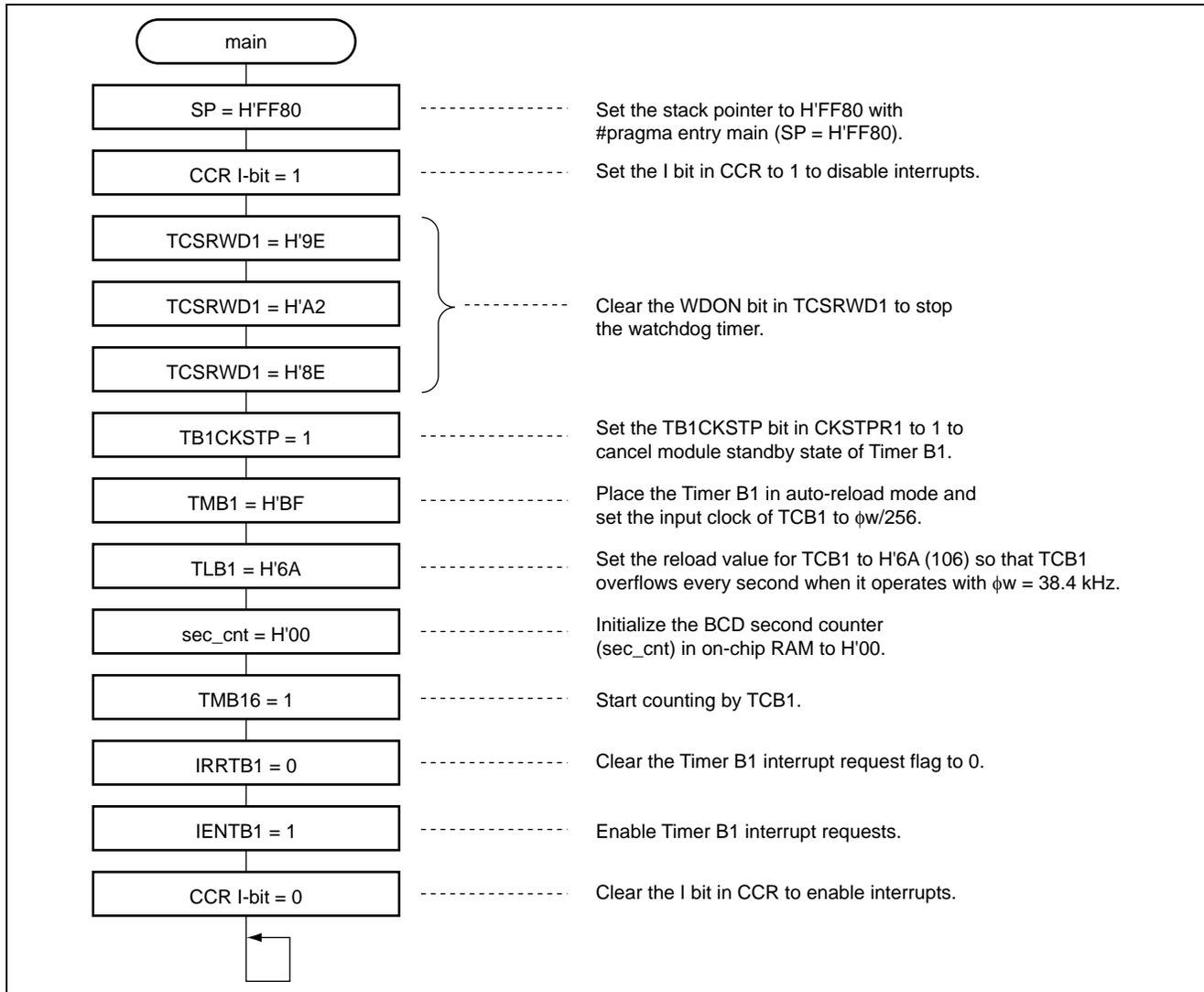
Label Name	Function	Data Length	Used In
sec_cnt	Second counter in BCD code	1 byte	main, cnt_up

- Second Counter (sec\_cnt) Address: H'FB80

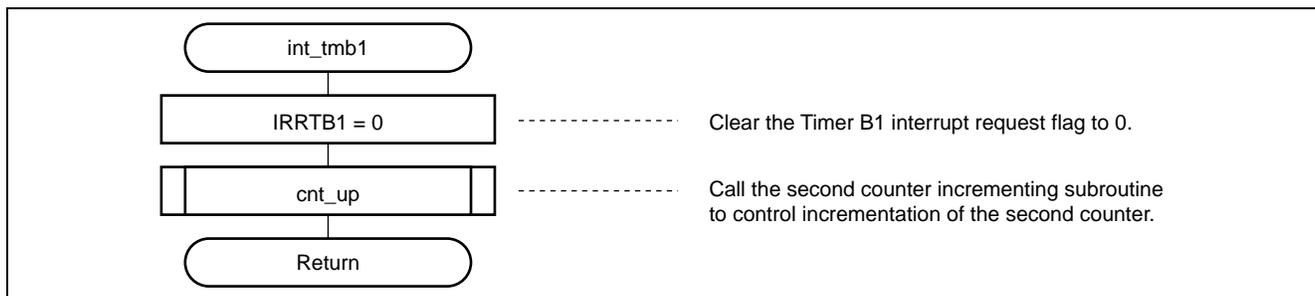
Bit	Bit Name	Initial Value	Function
7	—	0	Not used
6	sec12	0	10's place of the second counter
5	sec11	0	Incremented from 0 to 5 in the counting of 60 seconds.
4	sec10	0	
3	sec03	0	1's place of the second counter
2	sec02	0	Incremented from 0 to 9. When a carry is generated, the 10's place is incremented by 1.
1	sec01	0	
0	sec00	0	

### 5. Flowchart

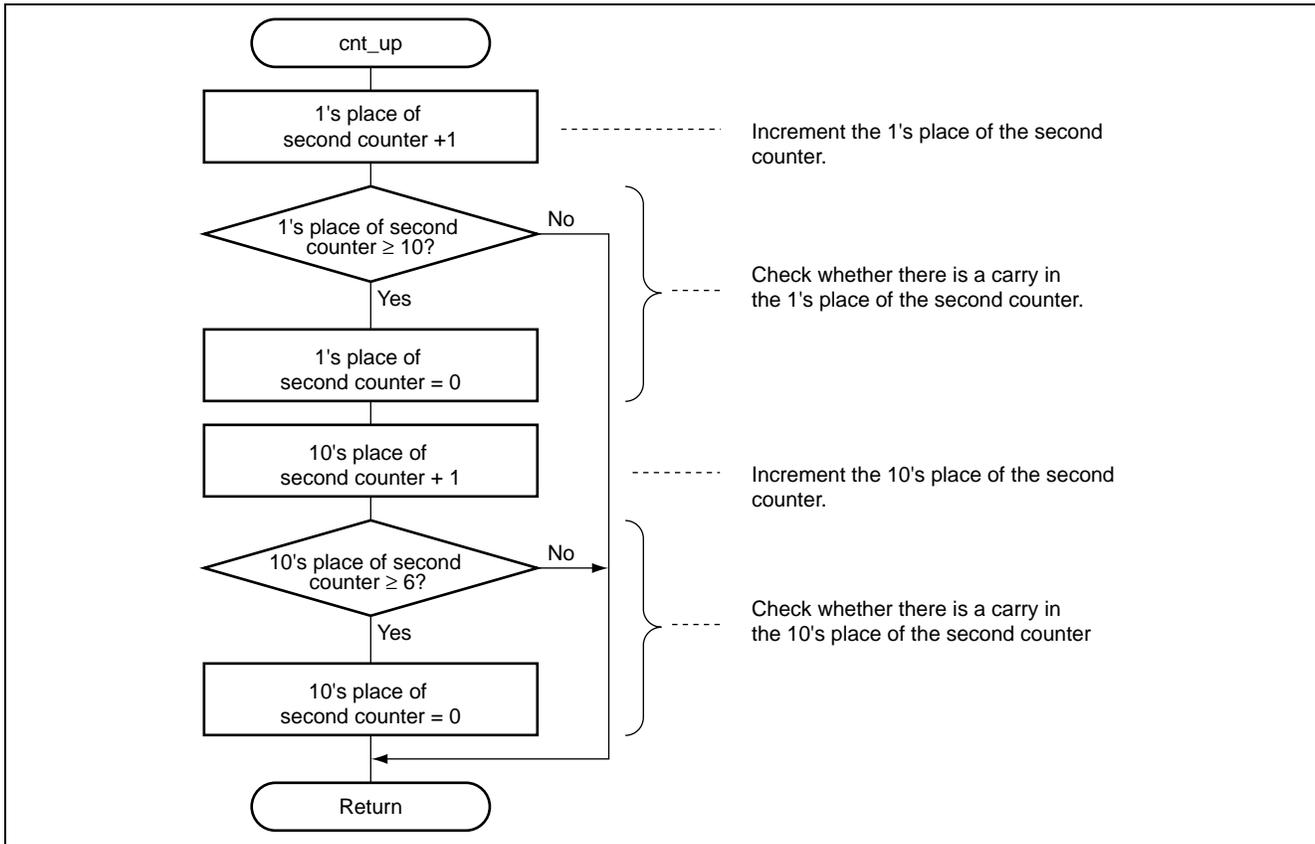
#### 5.1 main



#### 5.2 int\_tmb1



5.3 cnt\_up



5.4 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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