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H8/38602R Group

AECPWM Output

Introduction

The H8/38602R outputs a PWM waveform from the AECPWM pin by using the event-counter PWM function of the Asynchronous Event Counter (ACE).

Target Device

H8/38602R

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1. Specifications

The H8/38602R outputs a PWM waveform with a fixed duty cycle of 93.75% from the AECPWM pin, using the event-counter PWM function of the AEC. The AEC is used as a single-channel independent 16-bit event counter and an internal clock of $\phi/8$ is selected as the clock source for the event-counter PWM. The period of the output PWM waveform is 6.5536 ms, and the low pulse width is 409.6 μ s. Figure 1 shows a block diagram of the AECPWM output operation.

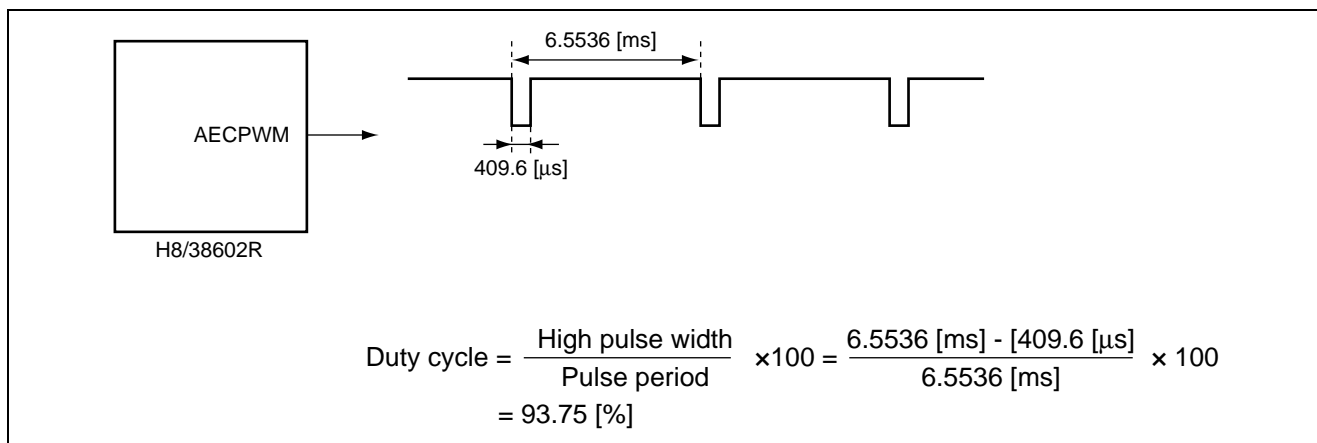


Figure 1 AECPWM Output Operation

2. Description of Functions

2.1 Functions

This sample task outputs a PWM waveform with a fixed duty cycle of 93.75% from the AECPWM pin using the event-counter PWM function of the AEC. An internal clock, $\phi/8$, is used as the input clock for the event-counter PWM. The functions used by this sample task are described below.

2.1.1 Event-Counter PWM Function of AEC

Figure 2 shows a block diagram of the event-counter PWM function of the AEC.

- Event Counter PWM Compare Register (ECPWCR)
ECPWCR is used to specify one conversion period of the event-counter PWM waveform. When the ECPWME bit in AEGSR is 1, the event-counter PWM is in operation, and therefore ECPWCR must not be modified. To change the conversion period, the event-counter PWM must be halted by clearing the ECPWME bit in AEGSR to 0 before modifying ECPWCR.
- Event Counter PWM Data Register (ECPWDR)
ECPWDR is used to specify the low-pulse width of the PWM waveform. When the ECPWME bit in AEGSR is 1, the event-counter PWM is in operation, and therefore ECPWDR must not be modified. To change the low-pulse width, the event-counter PWM must be halted by clearing the ECPWME bit in AEGSR to 0 before modifying ECPWCR.
- Input Pin Edge Select Register (AEGSR)
AEGSR is used to control IRQAEC/IECPWM.
- Event Counter Control Register (ECCR)
ECPWDR is used to select the clock for the event-counter PWM.

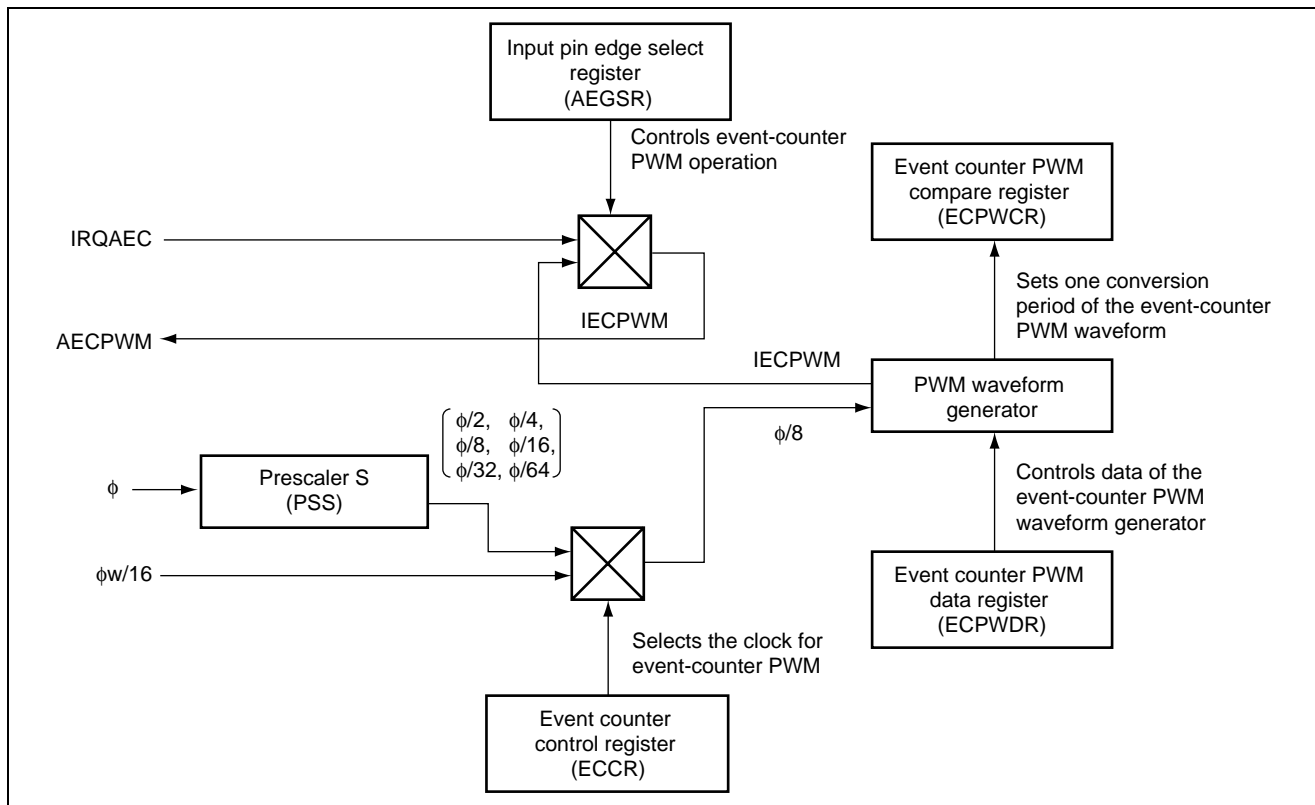


Figure 2 Event-Counter PWM Function of AEC

2.1.2 Module Standby Function

The module standby function places the AEC in module standby mode after a reset is released. Module standby mode of the AEC can be cancelled by setting the AECCKSTP bit in CKSTPR2 to 1.

- Clock Halt Register 2 (CKSTPR2)
CKSTPR2 allows the on-chip peripheral modules to enter standby mode in module units.

2.1.3 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and, if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.4 I/O Port Function

In this sample task, the P12/IRQAEC/AECPWM pin is set to be used as the IRQAEC input or AECPWM output pin.

- Port Mode Register 1 (PMR1)
PMR1 is used to select the functions of port 1 pins.

2.2 Setting PWM Waveform Period and Duty Cycle

Figure 3 shows how to specify the period and duty cycle of the PWM waveform generated by this sample task. This sample task uses a 10-MHz system clock.

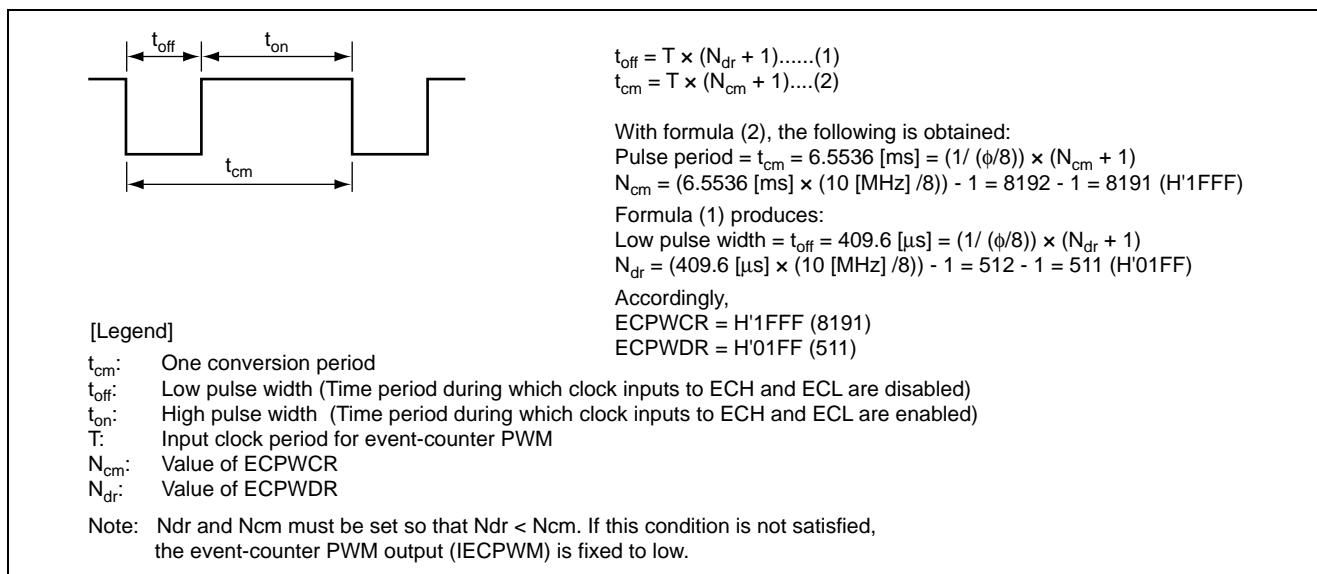


Figure 3 Setting the Period and Duty Cycle of the PWM Waveform

2.3 Assignment of Functions

Table 1 lists the function assignment for this sample task. By assigning the functions as shown in table 1, the H8/38602R outputs a PWM waveform from the AECPWM pin using the event-counter PWM function of the AEC.

Table 1 Assignment of Functions

Register	Description
ECPWCR	Specifies the period of the PWM waveform.
ECPWDR	Specifies the low pulse width of the PWM waveform.
AECSR	Enables event-counter PWM operation and disables IRQAEC.
ECCR	Selects an internal clock of $\phi/8$ as the input clock for event-counter PWM.
CKSTPR2	Cancels AEC module standby mode.
TCSRWD1	Stops the watchdog timer.
PMR1	Sets so that the P12/IRQAEC/AECPWM pin is used as the AECPWM output pin.

3. Principles of Operation

This sample task outputs a waveform with a fixed duty cycle of 93.75% using the event-counter PWM function of the ACE. An internal clock of $\phi/8$ is used as the input clock for the event-counter PWM. Figure 4 illustrates the AECPWM output operation.

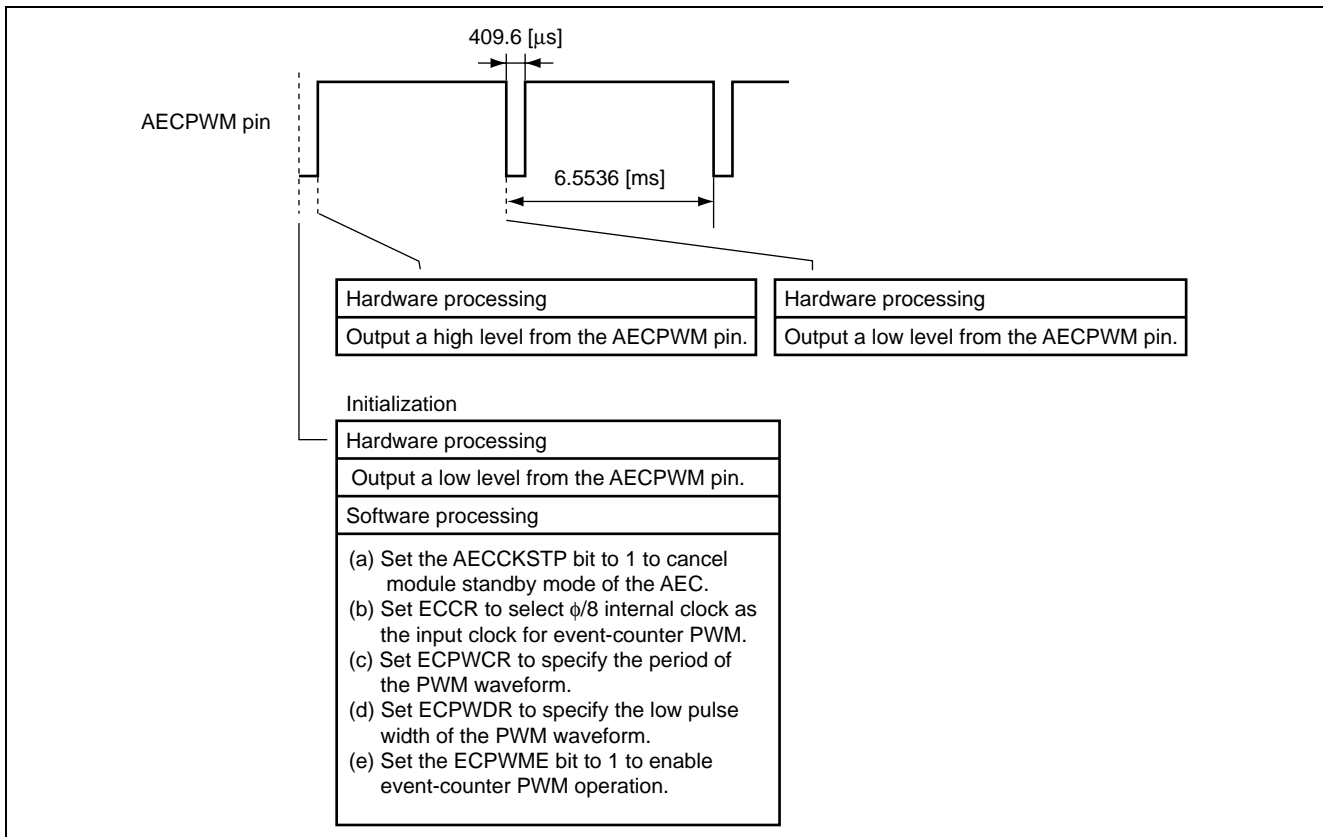


Figure 4 AECPWM Output Operation

4. Description of Software

4.1 Module

Table 2 shows the module of this sample task.

Table 2 Description of Module

Function Name	Description
main	Stops the watchdog timer, selects the AECPWM pin function, cancels AEC's module standby mode, initialize the AEC, and controls interrupts.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- Event Counter PWM Compare Register (ECPWCR) Address:H'FF8C

Bit	Bit Name	Setting	R/W	Function
15	ECPWCR15	0	R/W	One Conversion Period of Event Counter PWM Waveform
14	ECPWCR14	0	R/W	When the ECPWME bit in AEGSR is 1, the event-counter PWM is in operation and therefore ECPWCR should not be modified. To change the conversion period, the event-counter PWM must be halted by clearing the ECPWME bit in AEGSR to 0 before modifying ECPWCR.
13	ECPWCR13	0	R/W	
12	ECPWCR12	1	R/W	Setting value of ECPWCR = H'1FFF (8191)
11	ECPWCR11	1	R/W	
10	ECPWCR10	1	R/W	
9	ECPWCR9	1	R/W	
8	ECPWCR8	1	R/W	
7	ECPWCR7	1	R/W	
6	ECPWCR6	1	R/W	
5	ECPWCR5	1	R/W	
4	ECPWCR4	1	R/W	
3	ECPWCR3	1	R/W	
2	ECPWCR2	1	R/W	
1	ECPWCR1	1	R/W	
0	ECPWCR0	1	R/W	

- Event Counter PWM Data Register (ECPWDR) Address:H'FF8E

Bit	Bit Name	Setting	R/W	Function
15	ECPWDR15	0	W	Data Control of Event Counter PWM Waveform Generator
14	ECPWDR14	0	W	When the ECPWME bit in AEGSR is 1, the event-counter PWM is in operation, and therefore ECPWDR should not be modified. To modify the value of ECPWDR, the event-counter PWM must be halted by clearing the ECPWME bit in AEGSR to 0 in advance. Setting value of ECPWDR = H'01FF (511)
13	ECPWDR13	0	W	
12	ECPWDR12	0	W	
11	ECPWDR11	0	W	
10	ECPWDR10	0	W	
9	ECPWDR9	0	W	
8	ECPWDR8	1	W	
7	ECPWDR7	1	W	
6	ECPWDR6	1	W	
5	ECPWDR5	1	W	
4	ECPWDR4	1	W	
3	ECPWDR3	1	W	
2	ECPWDR2	1	W	
1	ECPWDR1	1	W	
0	ECPWDR0	1	W	

- Event Counter Control Register (ECCR) Address: H'FF94

Bit	Bit Name	Setting	R/W	Function
3	PWCK2	0	R/W	Event Counter PWM Clock Select
2	PWCK1	1	R/W	These bits select the input clock for the event-counter PWM.
1	PWCK0	0	R/W	000: $\phi/2$ 001: $\phi/4$ 010: $\phi/8$ 011: $\phi/16$ 100: $\phi/32$ 101: $\phi/64$ 110: $\phi_w/16$ 111: Setting prohibited

Note: To change the clock for the event-counter PWM, the event-counter PWM must be halted by clearing the ECPWME bit in AEGSR to 0 before modifying ECCR.

- Input Pin Edge Select Register (AEGSR) Address: H'FF92

Bit	Bit Name	Setting	R/W	Function
1	ECPWME	1	R/W	Event Counter PWM Enable Controls the operation of the event-counter PWM and selection of IRQAEC. 0: Event-counter PWM operation is halted and IRQAEC is selected. 1: Event-counter PWM operation is enabled and IRQAEC is not selected.

- Clock Halt Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Setting	R/W	Function
3	AECCKSTP	1	R/W	AEC Module Standby 0: AEC is placed in module standby mode. 1: AEC module standby mode is canceled.

- Timer Control/Status Register WD1 (TCSRWD1) Address H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.

Bit	Bit Name	Setting	R/W	Function
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] <ul style="list-style-type: none"> • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] <ul style="list-style-type: none"> • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	BOWI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the BOWI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] <ul style="list-style-type: none"> • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] <ul style="list-style-type: none"> • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

- Port Mode Register 1 (PMR1) Address: H'FFC0

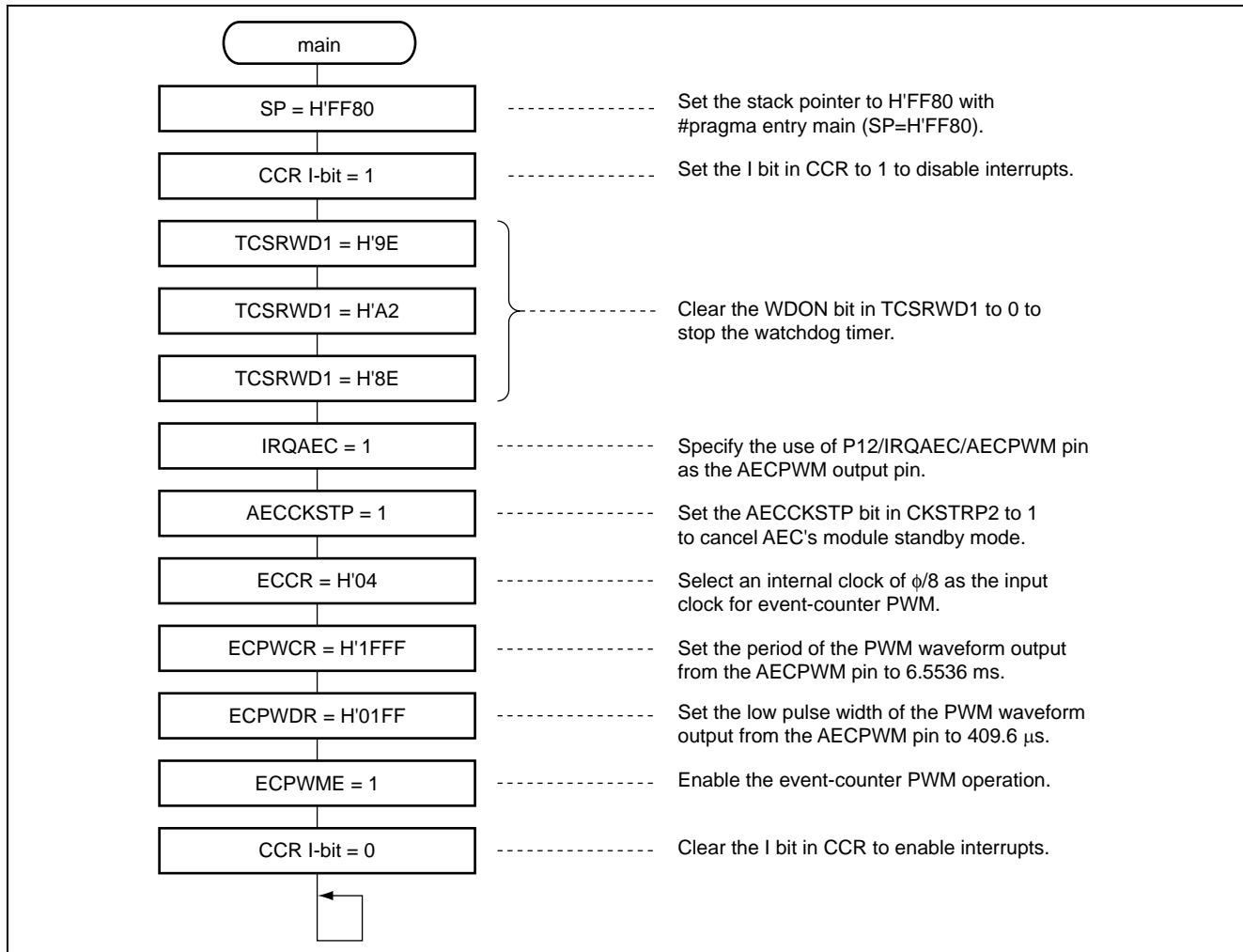
Bit	Bit Name	Setting	R/W	Function
5	IRQAEC	1	R/W	R12/IRQAEC/AECPWM Pin Function Select 0: The pin functions as a P12 I/O pin. 1: The pin functions as an IRQAEC input pin or AECPWM output pin.

4.4 RAM Usage

This sample task does not use on-chip RAM.

5. Flowchart

5.1 main



5.2 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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