To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8/38076R

Transition to the Subactive Mode

Introduction

In this example the power-down mode function of the H8/38076R is used to transition from the active (high-speed) mode to the subactive mode. After a reset is cleared, the SLEEP instruction is executed to directly enter the subactive mode from the active (high-speed) mode and one-second interrupts are generated from the RTC (realtime clock). The SLEEP instruction is then executed a second time to perform a direct transition to the active (high-speed) mode. P92 is connected to an LED, which illuminates when the device is in the subactive mode.

Target Device

H8/38076R

Contents

1. Specifications

- The power-down mode function of the H8/38076R is used to transition from the active (high-speed) mode to the subactive mode.
- After a reset is cleared, the SLEEP instruction is executed to perform a direct transition from the active (high-speed) mode to the subactive mode.
- After entering the subactive mode, the RTC function generates one-second interrupts.
- The SLEEP instruction is executed a second time to perform a direct transition to the active (high-speed) mode.
- P92 is connected to an LED, which is off when the device is in the active (high-speed) mode and illuminates when the device is in the subactive mode.
- A block diagram of the transition to the subactive mode is shown in figure 1.

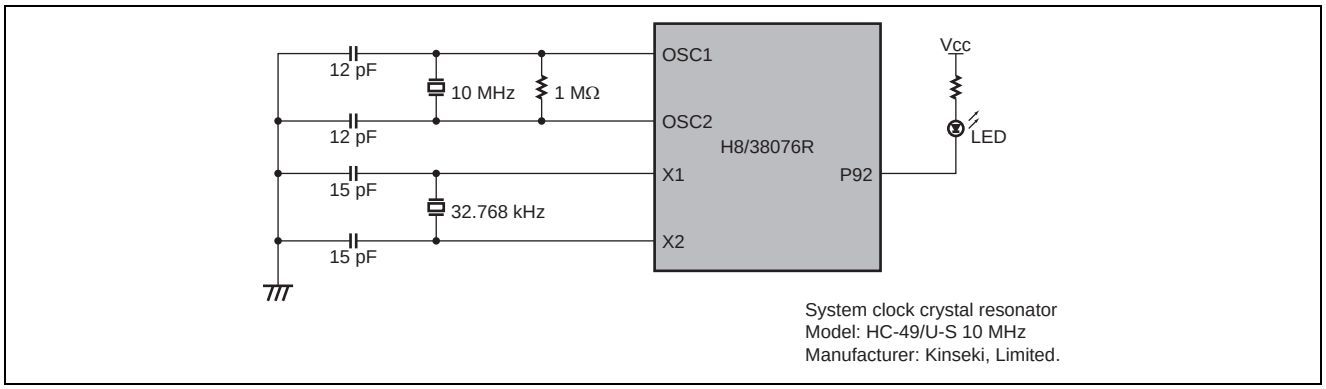


Figure 1 Block Diagram of Transition to the Subactive Mode

2. Description of Functions

2.1 Functions Used

1. The Subactive Mode

   In the subactive mode, the system clock oscillator (when the WDT (watchdog timer) disables internal oscillator operation) stops, but internal peripheral modules other than the A/D converter and PWM continue to function. As long as the required voltage is applied, the contents of some registers of the internal peripheral modules are retained.

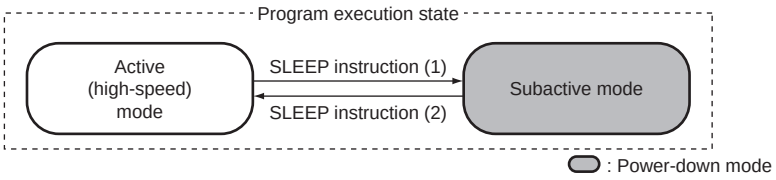
   The subactive mode is cleared by the SLEEP instruction. When the subactive mode is cleared a transition to the subsleep mode, the active mode, or the watch mode is made, depending on the combination of the SSBY, LSON, and TMA3 bits in system control register 1 (SYSCR1) and the MSON and DTON bits in system control register 2 (SYSCR2). The subactive mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the requested interrupt is disabled by one of the interrupt enable registers.

   When the $\overline{\text{RES}}$ signal goes low in the subactive mode, the system clock pulse oscillator starts. The $\overline{\text{RES}}$ signal must be kept low until the oscillator output stabilizes because system clock signals are supplied to the entire chip as soon as the system clock oscillator starts functioning. After the oscillation stabilization time has elapsed the CPU starts reset exception handling if the $\overline{\text{RES}}$ signal is driven high.

   The operating frequency of the subactive mode is selected from among 1/2, 1/4, and 1/8 of the watch clock (ϕ_W) by the SA1 and SA0 bits in SYSCR2. After the SLEEP instruction is executed the operating frequency changes to the frequency which was set before execution of the instruction.

2. Direct Transition

   The CPU can execute programs in the active mode or the subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition can be made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. A direct transition can also be used to change the operating frequency in the active or the subactive mode. After the mode transition, direct transition interrupt handling starts. If direct transition interrupts are disabled by the interrupt enable register 2 (IENR2), a transition is made instead to the sleep mode or the watch mode. Note that if a direct transition is attempted while the I bit in the control code register (CCR) is set to 1, the sleep mode or the watch mode will be entered, and the resulting mode cannot be cleared by an interrupt. Figure 2 shows direct transition between the active (high-speed) and subactive modes.



Conditions for mode transition

	LSON	MSON	SSBY	TMA3	DTON
SLEEP instruction (1)	1	*	1	1	1
SLEEP instruction (2)	0	0	1	1	1

Note: * indicates that this bit does not matter.

Figure 2 Mode Transition Diagram for the Active (High-Speed) Mode and the Subactive Mode

3. Description of Power-Down Mode Registers
   The registers related to the power-down modes are described below.

- System control register 1 (SYSCR1)
  Together with SYSCR2, SYSCR1 controls the power-down modes.
- System control register 2 (SYSCR2)
  Together with SYSCR1, SYSCR2 controls the power-down modes.
- Interrupt enable register 2 (IENR2)
  IENR2 enables direct transition interrupt requests.
- Interrupt request register 2 (IRR2)
  IRR2 is a status register that indicates direct transition interrupt requests.

4. Duration of Direct Transition from the Subactive Mode to the Active (High-Speed) Mode
   The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by the following equation.

$$\begin{aligned}\text{Direct transition time} = \{ &(\text{Number of SLEEP instruction execution states}) \\ &+ (\text{Number of internal processing states}) \} \times (t_{subcyc} \text{ before transition}) \\ &+ (\text{Wait time specified by STS2 to STS0}) \\ &+ (\text{Number of interrupt exception handling execution states}) \\ &\times (t_{cyc} \text{ after transition})\end{aligned}$$

Legend
t_{cyc}: System clock (ϕ) cycle time
t_{subcyc}: Subclock (ϕ_{SUB}) cycle time

5. Oscillation Stabilization Wait Time

   Figure 3 shows the oscillation waveform (OSC2), system clock (ϕ), and H8/38076R operating mode when a transition is made from the subactive mode to the active (high-speed or medium-speed) mode, with a resonator connected to the system clock oscillator.

   As shown in figure 3, a transition to the active (high-speed) mode requires the sum of the following two times (oscillation stabilization time and wait time) because the system clock oscillator is halted in the subactive mode.

- Oscillation stabilization time (t_{rc})

  The duration from the point at which the oscillation waveform from the system clock oscillator starts to change when an interrupt is generated, until the amplitude of the oscillation waveform increases and the oscillation frequency stabilizes.

- Wait time

  The time required for the CPU and peripheral function modules to start operating after the oscillation waveform frequency and system clock have stabilized. The wait time is selected by bits STS2 to STS0 in SYSCR1.

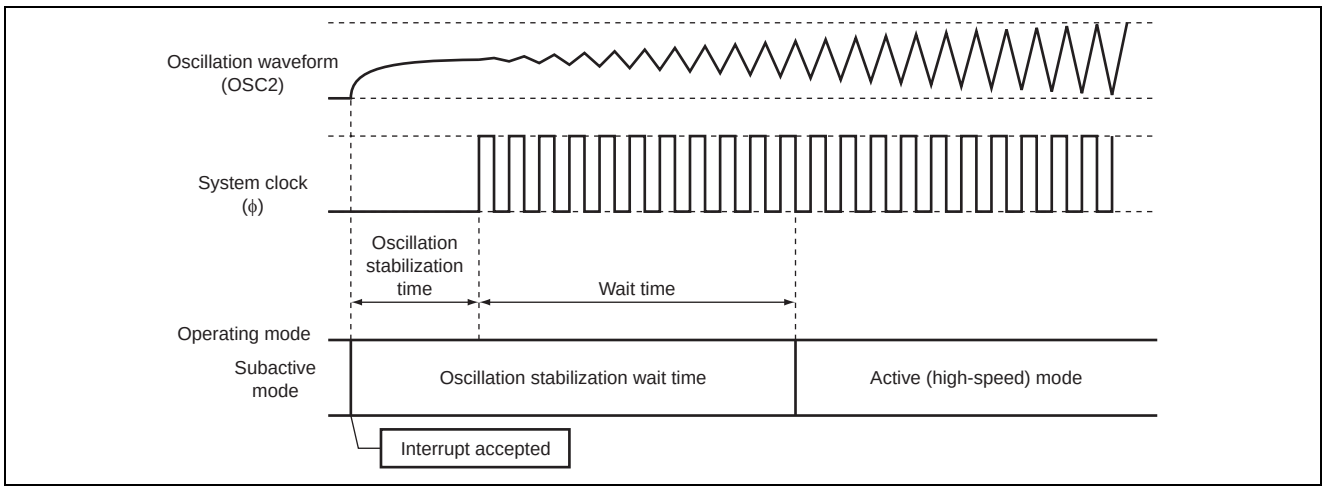


Figure 3 Oscillation Stabilization Wait Time

When the subactive mode is cleared by an interrupt or a reset, and a transition is made to the active mode, the oscillation waveform begins to change at the point at which the interrupt is accepted. Therefore, when a resonator is connected in the subactive mode, the oscillation stabilization time is necessary because the system clock oscillator is halted.

The oscillation stabilization time for this state transition is the same as the oscillation stabilization time at power-on (the duration from the point at which the power supply voltage reaches the prescribed level until oscillation stabilizes) specified as "oscillation stabilization time t_{rc}" in the AC characteristics.

Once the system clock has halted, a wait time of at least 8 states is necessary for the CPU and peripheral function modules to operate normally.

Thus, the time required from interrupt generation until operation of the CPU and peripheral function modules is the sum of the oscillation stabilization time and wait time described above. This total time is called the oscillation stabilization wait time and is expressed the following equation.

Oscillation stabilization wait time = oscillation stabilization time + wait time = t_{rc} + (8 to 16,384 states)

Therefore, when a transition is made from the subactive mode to the active (high-speed) mode, with an resonator connected to the system clock oscillator, the mounted circuit components must be evaluated carefully before deciding the oscillation stabilization wait time. Specifically, a suitable value should be determined in consultation with the resonator manufacturer, since the oscillation stabilization time may differ depending on the mounted circuit component constants, stray capacitance, and so on. Confirm that the oscillation amplitude is approximately 1 V or greater during the wait time.

6. Operating Frequency and Wait Time
   Table 1 shows the relationship between the settings of bits STS2 to STS0 in SYSCR1, the operating frequency, and the wait time.

Table 1 Settings of Bits STS2 to STS0, Operating Frequency, and Wait Time

Bit				Wait Time		
STS2	STS1	STS0	Number of Wait States	Operating Frequency: 10 MHz	Operating Frequency: 5 MHz	Operating Frequency: 2 MHz
0	0	0	8,192 states	0.819 ms	1.638 ms	4.1 ms
0	0	1	16,384 states	1.638 ms	3.277 ms	8.2 ms
0	1	0	1,024 states	0.102 ms	0.205 ms	0.512 ms
0	1	1	2,048 states	0.205 ms	0.410 ms	1.024 ms
1	0	0	4,096 states	0.410 ms	0.819 ms	2.048 ms
1	0	1	2 states (external clock input)	0.0002 ms	0.0004 ms	0.001 ms
1	1	0	8 states	0.0008 ms	0.002 ms	0.004 ms
1	1	1	16 states	0.002 ms	0.003 ms	0.008 ms

In this sample task a crystal resonator (Kinseki, Limited HC-49/U-S 10 MHz) is connected to the system clock oscillator. Therefore, to accommodate the oscillation stabilization time t_{rc} of 0.8 ms (typ.) (Vcc = 2.7 to 3.3 V) specified in the AC characteristics, bits STS2 to STS0 in SYSCR1 are set to 000 to produce a wait time of approximately 0.819 ms.

7. State of Device in the Subactive Mode
   Table 2 shows the state of the H8/38076R in the subactive mode.

Table 2 State of the H8/38076R in the Subactive Mode

Function		Status
System clock oscillator		Halted
Subclock oscillator		Functioning
CPU	Instructions	Functioning
	RAM	Functioning
	Registers	Functioning
	I/O	Functioning
External interrupts	IRQ0	Functioning
	IRQ1	Functioning
	IRQ3	Functioning
	IRQ4	Functioning
	IRQAEC	Functioning
	WKP0 to WKP7	Functioning
Peripheral modules	Timer F	Functioning/retained*1
	AEC (Asynchronous event counter)	Functioning
	RTC (realtime clock)	Functioning/retained*2
	TPU (timer pulse unit)	Retained
	Watchdog timer (WDT)	Functioning*3/retained*4
	SCI3/IrDA module	Functioning/retained*5
	I^2C2 module	Retained
	PWM module	Retained
	A/D converter	Retained
	LCD controller/driver	Functioning/retained*6

Notes: 1. Functioning if $\phi_W/4$ is selected as an internal clock. Halted and retained otherwise.
2. Functioning if the RTC function is selected. Retained if the free running counter function is selected.
3. Functioning only if the internal oscillator is selected.
4. Functioning if $\phi_W/32$ is selected as an internal clock. Halted and retained otherwise.
5. Functioning if $\phi_W/2$ is selected as an internal clock. Halted and retained otherwise.
6. Functioning if ϕ_W, $\phi_W/2$, or $\phi_W/4$ is selected as the clock to be used. Halted and retained otherwise.

2.2 RTC Function

In this sample task the RTC function is used to generate interrupts at 1-second intervals. The RTC function is described below.

1. Registers for RTC Function
   The registers related to the RTC function are described below.

- Second data register/free running counter data register (RSECDR)
  RSECDR counts seconds. It indicates BCD codes and counts from 0 to 59. It is an 8-bit read register used as a counter when it operates as a free running counter.
- Minute data register (RMINDR)
  RMINDR counts minutes on the carry generated by RSECDR. It indicates BCD codes and counts from 0 to 59.
- Hour data register (RHRDR)
  RHRDR counts hours on the carry generated by RMINDR. It indicates BCD codes and counts from 0 to 11 or from 0 to 23, depending on the setting of the 12/24 bit in RTCCR1.
- Day-of-week data register (RWKDR)
  RWKDR counts the days of the week on the carry generated by RHRDR. It indicates the day of the week as a binary code from 0 to 6 using bits WK2 to WK0.
- RTC control register 1 (RTCCR1)
  RTCCR1 controls start, stop and reset of the clock timer.
- RTC control register 2 (RTCCR2)
  RTCCR2 controls RTC periodic interrupts of week, day, hour, minute, one second, 0.5 seconds, and 0.25 seconds. Enabling interrupts of week, day, hour, minute, one second, 0.5 seconds, and 0.25 seconds sets the corresponding flag to 1 in the RTC interrupt flag register (RTCFLG) when an interrupt occurs. It also controls overflow interrupts of a free running counter when RTC operates as a free running counter.
- Clock source select register (RTCCSR)
  RTCCSR selects the clock source. A free running counter controls start/stop of counter operation by the RUN bit setting in RTCCR1. When a clock other than 32.768 kHz is selected, the RTC is disabled and operates as an 8-bit free running counter. When the RTC operates as an 8-bit free running counter, RSECDR enables reading of counter values. An interrupt can be generated by setting the FOIE bit in RTCCR2 to 1 and enabling overflow interrupts of the free running counter. A clock whose frequency is the system clock divided by 32, 16, 8, or 4 is output in the active and sleep modes.
- RTC interrupt flag register (RTCFLG)
  RTCFLG sets the corresponding flag when an interrupt occurs. Each flag is not cleared automatically even if the interrupt is accepted. Flags can are cleared by writing 0 to them.
- Interrupt enable register 1 (IENR1)
  IENR1 enables RTC interrupts.

2.3 I/O Port Functions

In this sample task the P92 pin is connected to an LED, which is turned on and off by the port output. The functions of port 9 are described below.

1. Port 9 registers
   The registers related to port 9 are described below.

- Port control register 9 (PCR9)
  PCR9 selects the input/output state of the pins of port 9 in bit units.
- Port data register 9 (PDR9)
  PDR9 is a register that stores data for pins of port 9.

2.4 Assignment of Functions

Table 3 shows the assignment of functions in this sample task.

Table 3 Assignment of Functions

Elements	Description
SYSCR1	Together with SYSCR2, controls transitions between the active (high-speed) mode and subactive modes
SYSCR2	Together with SYSCR1, controls transitions between the active (high-speed) mode and subactive modes
IENR2	Set to enable direct transition interrupts
IRR2	Direct transition interrupt request flag
RSECDR	Counts seconds
RMINDR	Counts minutes
RHRDR	Counts hours
RWKDR	Counts days of the week
RTCCR1	Controls operation start/stop of the clock timer, controls resets
RTCCR2	Set to enable one-second periodic interrupts
RTCCSR	Selects RTC operation by setting the clock source to 32.768 kHz
RTCFLG	One-second periodic interrupt request flag
IENR1	Set to enable RTC interrupt requests
PCR9	Sets P92 as output pin
PDR9	Stores output data of P92 output pin

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 4.

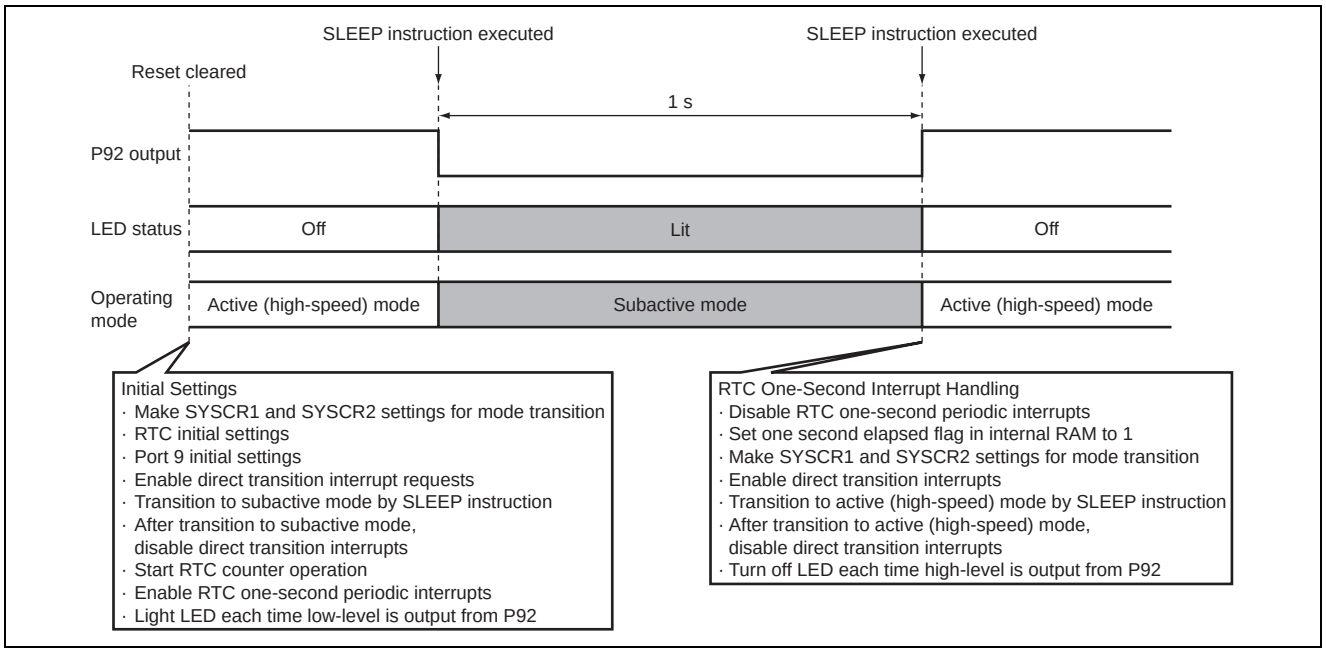


Figure 4 Principles of Operation

4. Description of Software

4.1 Modules

Table 4 shows the modules used in this sample task.

Table 4 Modules

Function Name	Description
main	Makes initial settings for mode transition, makes initial settings for RTC, makes initial settings for pin P92, enables direct transition interrupt requests, transitions to the subactive mode, starts RTC count operation, enables RTC one-second periodic interrupt requests, lights LED by outputting low level from output pin P92, makes SYSCR1 and SYSCR2 settings for mode transition, enters the active (high-speed) mode, disables direct transition interrupt requests, turns off LED by outputting high level from output pin P92
int_sleep	Clears direct transition interrupt flag as part of direct transition interrupt handling
int_rtc	Clears RTC one-second periodic interrupt flag as part of RTC one-second periodic interrupt handling, disables RTC one-second periodic interrupt requests, halts RTC operation, sets one second elapsed flag

4.2 Internal Registers Used

The internal registers used in this sample task are shown below.

- SYSCR1 System control register 1 Address: H'FFF0

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	SSBY	0	R/W	Software standby Selects the mode to transition to after execution of the SLEEP instruction. 0: A transition is made to the sleep mode or the subsleep mode 1: A transition is made to the standby mode or the watch mode	1
6	STS2	0	R/W	Standby timer selection 2 to 0	0
5	STS1	0	R/W	Specifies the number of wait states that must	0
4	STS0	0	R/W	elapse after the system clock oscillator begins functioning until the clock is supplied when transitioning from the standby mode, the subactive mode, the subsleep mode, or the watch mode to the active mode or the sleep mode. 000: 8,192 wait states 001: 16,384 wait states 010: 1,024 wait states 011: 2,048 wait states 100: 4,096 wait states 101: 2 wait states 110: 8 wait states 111: 16 wait states	0
3	LSON	0	R/W	Low speed on flag Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when the watch mode is cleared. 0: CPU operates on system clock (ϕ) 1: CPU operates on subclock (ϕ_{SUB})	1
2	TMA3	0	R/W	In combination with the SSBY and LSON bits in SYSCR1 and the DTON and MSON bits in SYSCR2, selects the mode to which transition is made after the SLEEP instruction is executed.	1
1	MA1	1	R/W	Active mode clock selection 1 and 0	1
0	MA0	1	R/W	Selects the operating clock frequency in the active (medium-speed) mode and the sleep (medium-speed) mode. 00: ϕ_{OSC}/8 01: ϕ_{OSC}/16 10: ϕ_{OSC}/32 11: ϕ_{OSC}/64	1

- SYSCR2 System control register 2 Address: H'FFF1

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	—	1	—	Reserved	1
6	—	1	—	These bits are always read as 1 and cannot be	1
5	—	1	—	modified.	1
4	NESEL	1	R/W	Noise elimination sampling frequency selection The subclock oscillator generates the watch clock (ϕ_W) and the system clock oscillator generates the oscillator clock (ϕ_{OSC}). This bit selects the sampling frequency of ϕ_{OSC} when ϕ_W is sampled. 0: Sampling rate is ϕ_{OSC}/16 1: Sampling rate is ϕ_{OSC}/4	0
3	DTON	0	R/W	Direct transfer on flag In combination with the SSBY, TMA3, and LSON bits in SYSCR1 and the MSON bit in SYSCR2, this bit selects the mode to which transition is made after the SLEEP instruction is executed.	1
2	MSON	0	R/W	Middle speed on flag This bit selects whether operation continues in the active (high-speed) mode or the active (medium-speed) mode after the standby mode, the watch mode, or the sleep mode is cleared. 0: Active (high-speed) mode 1: Active (medium-speed) mode	0
1	SA1	0	R/W	Subactive mode clock selection 1 and 0	0
0	SA0	0	R/W	Selects the operating clock frequency in the subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: ϕ_W/8 01: ϕ_W/4 1X: ϕ_W/2	0

Note: x: Don't care

- IENR2 Interrupt enable register 2 Address: H'FFF4

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	IENDT	0	R/W	Direct transition interrupt request enable 0: Direct transition interrupt requests disabled 1: Direct transition interrupt requests enabled	1

- IRR2 Interrupt request register 2 Address: H'FFF7

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	IRRDT	0	R/W	Direct transition interrupt request flag [Setting condition] When the SLEEP instruction is executed and direct transition is made while the DTON bit in SYSCR2 is set to 1 [Clearing condition] When 0 is written to this bit	0

- RSECDR Second data register/free running counter data register Address: H'F068

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	BSY	—	R	RTC busy This bit is set to 1 when the RTC is updating (operating) the values of the second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers may be used when this bit is 0.	0
6	SC12	—	R/W	Seconds ten's position count	0
5	SC11	—	R/W	Counts the tens position value from 0 to 5 for 60-second counting.	0
4	SC10	—	R/W		0
3	SC03	—	R/W	Seconds one's position count	0
2	SC02	—	R/W	Counts the ones position value from 0 to 9, incrementing once per second. When a carry is generated, 1 is added to the tens position value.	0
1	SC01	—	R/W		0
0	SC00	—	R/W		0

- RMINDR Minute data register Address: H'F069

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	BSY	—	R	RTC busy This bit is set to 1 when the RTC is updating (operating) the values of the second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers may be used when this bit is 0.	0
6	MN12	—	R/W	Minutes tens position count	0
5	MN11	—	R/W	Counts the ten's position value from 0 to 5 for 60-minute counting.	0
4	MN10	—	R/W		0
3	MN03	—	R/W	Minutes ones position count	0
2	MN02	—	R/W	Counts the one's position value from 0 to 9, incrementing once per minute. When a carry is generated, 1 is added to the tens position value.	0
1	MN01	—	R/W		0
0	MN00	—	R/W		0

- RHRDR Hour data register Address: H'F06A

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	BSY	—	R	RTC busy This bit is set to 1 when the RTC is updating (operating) the values of the second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers may be used when this bit is 0.	0
6	—	0	—	Reserved This bit is always read as 0.	0
5	HR11	—	R/W	Hours tens position count	0
4	HR10	—	R/W	Counts the ten's position value for hours from 0 to 2.	0
3	HR03	—	R/W	Hours ones position count	0
2	HR02	—	R/W	Counts the one's position value from 0 to 9,	0
1	HR01	—	R/W	incrementing once per hour. When a carry is	0
0	HR00	—	R/W	generated, 1 is added to the tens position value.	0

- RWKDR Day-of-week data register Address: H'F06B

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	BSY	—	R	RTC busy This bit is set to 1 when the RTC is updating (operating) the values of the second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers may be used when this bit is 0.	0
6	—	0	—	Reserved	0
5	—	0	—	These bits are always read as 0.	0
4	—	0	—		0
3	—	0	—		0
2	WK2	—	R/W	Day-of-week count	0
1	WK1	—	R/W	Day-of-week is indicated with in binary.	0
0	WK0	—	R/W	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday 111: Setting disabled	0

- RTCCR1 RTC control register 1 Address: H'F06C

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	RUN	—	R/W	RTC operation start 0: Stops RTC operation 1: Starts RTC operation	1
6	12/24	—	R/W	Operating mode 0: RTC operates in 12-hour mode. RHRDR is used to count from 0 to 11 1: RTC operates in 24-hour mode. RHRDR is used to count from 0 to 23	0
5	PM	—	R/W	A.m./p.m. 0: Indicates a.m. when RTC is in the 12-hour mode 1: Indicates p.m. when RTC is in the 12-hour mode	0
4	RST	0	R/W	Reset 0: Normal operation 1: Resets all registers and control circuits except RTCCSR and this bit. Always clear this bit to 0 after setting it to 1	0
3	—	0	—	Reserved	0
2	—	0	—	These bits are always read as 0.	0
1	—	0	—		0
0	—	0	—		0

- RTCCR2 RTC control register 2 Address: H'F06D

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	FOIE	—	R/W	Free running counter overflow interrupt enable 0: Free running counter overflow interrupts disabled 1: Free running counter overflow interrupts enabled	0
6	WKIE	—	R/W	Week periodic interrupt enable 0: Week periodic interrupts disabled 1: Week periodic interrupts enabled	0
5	DYIE	—	R/W	Day periodic interrupt enable 0: Day periodic interrupts disabled 1: Day periodic interrupts enabled	0
4	HRIE	—	R/W	Hour periodic interrupt enable 0: Hour periodic interrupts disabled 1: Hour periodic interrupts enabled	0
3	MNIE	—	R/W	Minute periodic interrupt enable 0: Minute periodic interrupts disabled 1: Minute periodic interrupts enabled	0
2	1SEIE	—	R/W	One-second periodic interrupt enable 0: One-second periodic interrupts disabled 1: One-second periodic interrupts enabled	1
1	05SEIE	—	R/W	0.5-second periodic interrupt enable 0: 0.5-second periodic interrupts disabled 1: 0.5-second periodic interrupts enabled	0
0	025SEIE	—	R/W	0.25-second periodic interrupt enable 0: 0.25-second periodic interrupts disabled 1: 0.25-second periodic interrupts enabled	0

- RTCCSR Clock source select register Address: H'F06F

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	—	0	—	Reserved This bit is always read as 0.	0
6	RCS6	0	R/W	Clock output selection	0
5	RCS5	0	R/W	Selects the clock output from the TMOW pin when	0
4	SUB32K	0	R/W	the TMOW bit in port mode register 3 (PMR3) has been set to 1. 000: ϕ/4 001: ϕ/8 010: ϕ/16 011: ϕ/32 xx1: ϕ_W	0
3	RCS3	1	R/W	Clock source selection	1
2	RCS2	0	R/W	0000: ϕ/8 Free running counter operation	0
1	RCS1	0	R/W	0001: ϕ/32 Free running counter operation	0
0	RCS0	0	R/W	0010: ϕ/128 Free running counter operation 0011: ϕ/256 Free running counter operation 0100: ϕ/512 Free running counter operation 0101: ϕ/2,048 Free running counter operation 0110: ϕ/4,096 Free running counter operation 0111: ϕ/8,192 Free running counter operation 1xxx: 32.768 kHz RTC operation	0

Note: x: Don’t care

- RTCFLG RTC interrupt flag register Address: H'F067

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	FOIFG	0	R/W*	Free running counter overflow interrupt request flag [Setting condition] When a free running counter overflows [Clearing condition] When 0 is written to FOIFG when FOIFG = 1	0
6	WKIFG	0	R/W*	Week periodic interrupt request flag [Setting condition] When a week periodic interrupt occurs [Clearing condition] When 0 is written to WKIFG when WKIFG = 1	0
5	DYIFG	0	R/W*	Day periodic interrupt request flag [Setting condition] When a day periodic interrupt occurs [Clearing condition] When 0 is written to DYIFG when DYIFG = 1	0
4	HRIFG	0	R/W*	Hour periodic interrupt request flag [Setting condition] When an hour periodic interrupt occurs [Clearing condition] When 0 is written to HRIFG when HRIFG = 1	0
3	MNIFG	0	R/W*	Minute periodic interrupt request flag [Setting condition] When a minute periodic interrupt occurs [Clearing condition] When 0 is written to MNIFG when MNIFG = 1	0
2	SEIFG	0	R/W*	One-second periodic interrupt request flag [Setting condition] When a one-second periodic interrupt occurs [Clearing condition] When 0 is written to SEIFG when SEIFG = 1	0
1	05SEIFG	0	R/W*	0.5-second periodic interrupt request flag [Setting condition] When a 0.5-second periodic interrupt occurs [Clearing condition] When 0 is written to 05SEIFG when 05SEIFG = 1	0
0	025SEIFG	0	R/W*	0.25-second periodic interrupt request flag [Setting condition] When a 0.25-second periodic interrupt occurs [Clearing condition] When 0 is written to 025SEIFG when 025SEIFG = 1	0

Note: * Only 0 can be written to clear the flag.

- IENR1 Interrupt enable register 1 Address: H'FFF3

Bit	Bit Name	Initial Value	R/W	Description	Set Value
7	IENRTC	0	R/W	RTC interrupt request enable 0: RTC interrupt requests disabled 1: RTC interrupt requests enabled	1

- PCR9 Port control register 9 Address: H'FFEC

Bit	Bit Name	Initial Value	R/W	Description	Set Value
2	PCR92	0	W	Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and in PDR9 are valid when the corresponding pin is designated as a general I/O pin. PCR9 is a write-only register. This bit is always read as 1.	1

- PDR9 Port data register 9 Address: H'FFDC

Bit	Bit Name	Initial Value	R/W	Description	Set Value
2	P92	1	R/W	If port 9 is read while this bit is set to 1, the corresponding value stored in PDR9 is read directly, regardless of the actual pin state. If port 9 is read while this bit is cleared to 0, the state of the corresponding pin is read.	1

4.3 RAM Usage

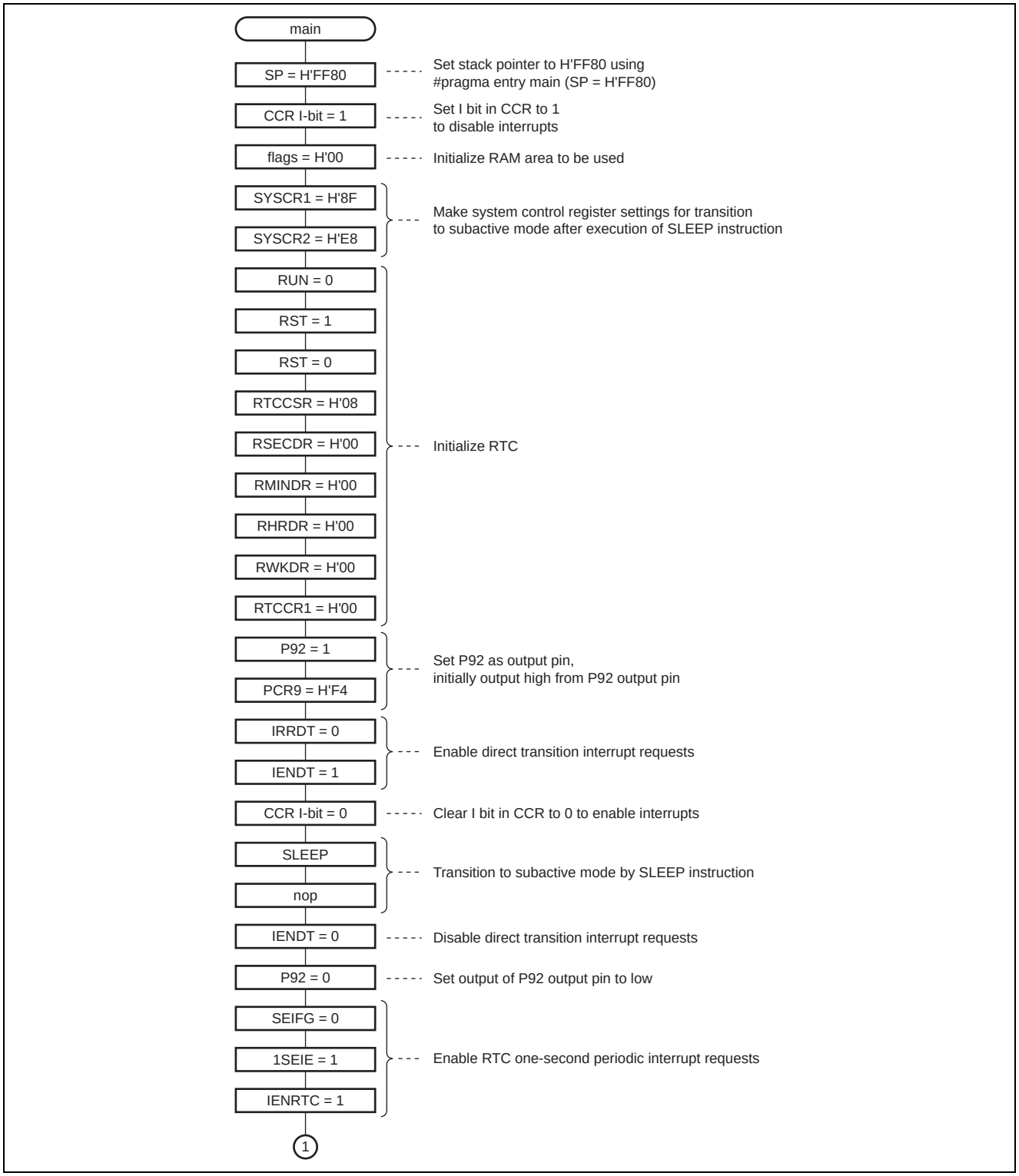
The RAM used in this sample task is shown below.

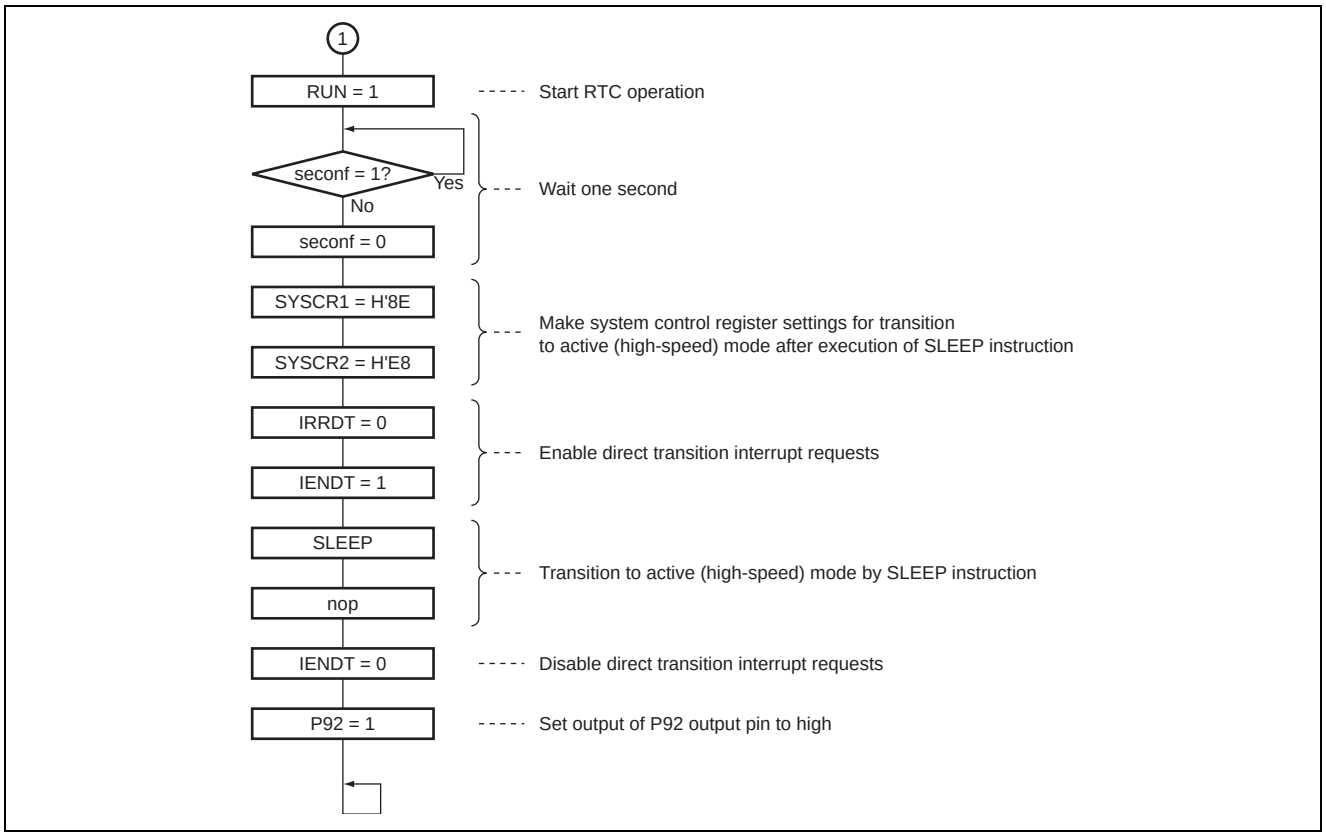
- flags User flag area Address: H'FB80

Bit	Bit Name	Initial Value	Description	Used in
7	seconf	0	Flag showing that the RTC has generated a one-second interrupt following a transition to the subactive mode	main int_rtc

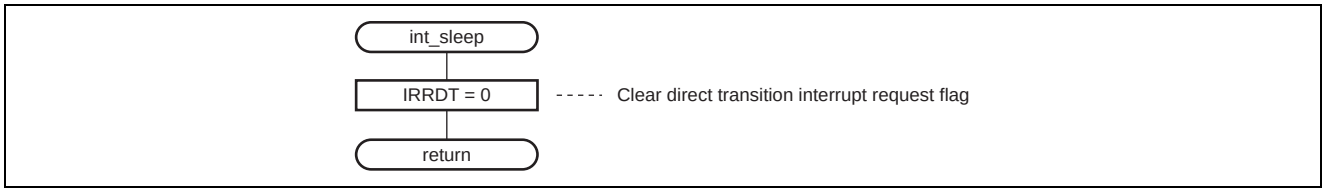
5. Flowcharts

5.1 main (Main Routine)

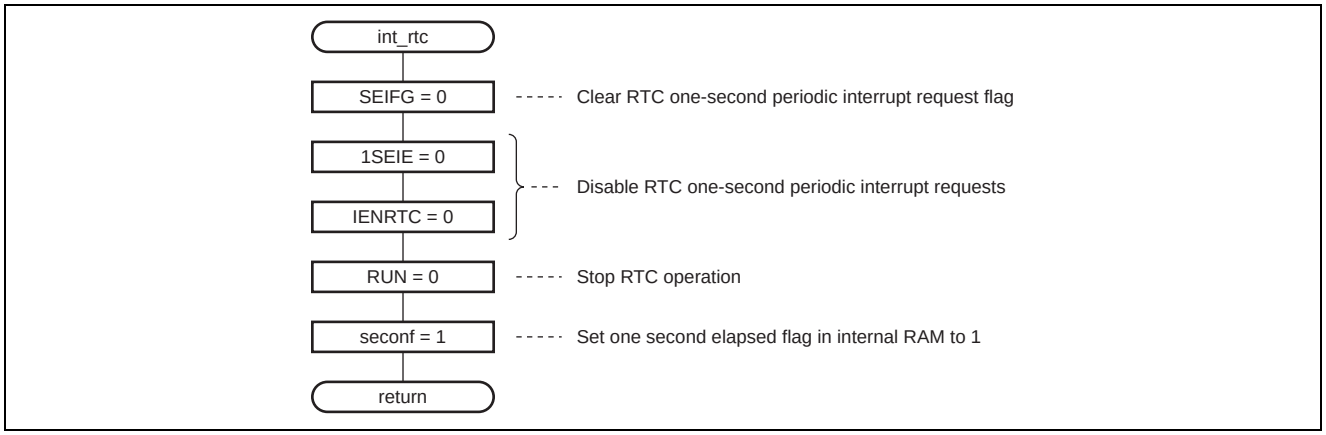




5.2 int_sleep (Direct Transition Interrupt Handling Routine)



5.3 int_rtc (RTC Interrupt Handling Routine)



5.4 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.18.05	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.