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H8/38076R

Transition to the Standby Mode

Introduction

In this example a transition is made from the active (high-speed) mode to the standby mode, one of the power-down modes of the H8/38076R.

Target Device

H8/38076R

Contents

1. Specifications 2
2. Description of Functions 2
3. Principles of Operation 4
4. Internal Registers Used 5

1. Specifications

After a reset is cleared the H8/38076R can transition to any of seven power-down modes, in which power consumption is reduced substantially, in addition to the normal active (high-speed) mode. In this sample task a transition is made from the active (high-speed) mode to the standby mode, one of the power-down modes.

2. Description of Functions

2.1 Functions Used

In this sample task a transition is made from the active (high-speed) mode to the standby mode, one of the power-down modes.

The state of the H8/38076R in the standby mode is shown in table 1, and the functions used as described below.

1. System Clock (ϕ)
   This 10-MHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

2. Subclock (ϕ_W)
   This 32.768-kHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

3. Power-Down Mode (Standby Mode) Function
   In the standby mode the system clock oscillator stops, so the CPU and internal peripheral modules stop functioning when the WDT disables internal oscillator operation. However, the contents of CPU registers, internal RAM, and some internal peripheral module registers are retained as long as the rated voltage is supplied. Internal RAM contents are retained as long as the voltage set by the RAM data retention voltage is provided. The I/O ports enters the high-impedance state.
   The standby mode is cleared by an interrupt. When an interrupt is requested, the system clock oscillator starts. After the time set in bits STS2 to STS0 in SYSCR1 has elapsed, the standby mode is cleared and interrupt exception handling starts. After the standby mode is cleared, a transition is made to the active (high-speed) or the active (medium-speed) mode according to the MSON bit in SYSCR2. The standby mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable bit.
   When the $\overline{\text{RES}}$ signal goes low in the standby mode, the system clock oscillator starts. System clock signals are supplied to the entire device as soon as the system clock oscillator starts functioning. Make sure to keep the $\overline{\text{RES}}$ signal low level until the system clock oscillator output stabilizes (unless the power-on reset circuit is used). After the oscillation stabilization time has elapsed the CPU starts reset exception handling if the $\overline{\text{RES}}$ signal is driven high (unless the power-on reset circuit is used).

- System control register 1 (SYSCR1)
  Together with SYSCR2, SYSCR1 controls the power-down modes.

- System control register 2 (SYSCR2)
  Together with SYSCR1, SYSCR2 controls the power-down modes.

Table 1 State of the H8/38076R in the Standby Mode

Function		Standby Mode
System clock oscillator		Halted
Subclock oscillator		Functioning
CPU	Instructions	Halted
	RAM	Retained
	Registers	Retained
	I/O	Retained[*1]
External interrupts	IRQ0	Functioning
	IRQ1	Functioning
	IRQ3	Retained[*2]
	IRQ4	Retained[*2]
	IRQAEC	Retained[*2]
	WKP0 to WKP7	Functioning
Peripheral modules	Timer F	Retained
	Asynchronous event counter	Functioning[*3]
	RTC (realtime clock)	Functioning/Retained[*4]
	TPU (timer pulse unit)	Retained
	WDT (watchdog timer)	Functioning[*5]/Retained
	SCI3/IrDA module	Reset
	I^2C2 module	Retained
	PWM module	Retained
	A/D converter	Retained
	LCD controller/driver	Retained

Notes: 1. Register contents are retained. Output is the high-impedance state.
2. External interrupt requests are ignored. The contents of the interrupt request register are not affected.
3. The counter can be incremented.
4. Functioning if the clock time-base function is selected and retained if the interval timer is selected.
5. Functioning if the internal oscillator is selected.

2.2 Assignment of Functions

Table 2 shows the assignment of functions in this sample task. A transition is made from the active (high-speed) mode to the standby mode, one of the power-down modes, using functions assigned as shown in table 2.

Table 2 Assignment of Functions

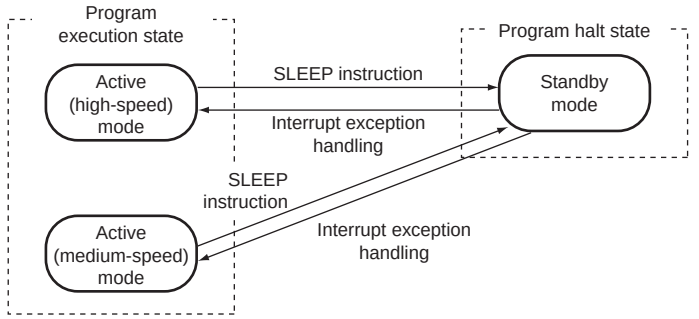
Elements	Description
SYSCR1	Together with SYSCR2, controls transition to the standby mode
SYSCR2	Together with SYSCR1, controls transition to the standby mode

3. Principles of Operation

The principles of operation of this sample task are described below. Using the procedure shown, a transition is made from the active (high-speed) mode to the standby mode, one of the power-down modes. The mode transitions in this sample task are illustrated in figure 1.

1. Transition to the standby mode
   a. Set the SSBY bit to 1 and clear the LSON and TMA3 bits to 0 in SYSCR1.
   b. Clear the DTON bit to 0 in SYSCR2.
   c. Execute the SLEEP instruction.

2. Clearing the standby mode
   a. Receive an IRQ1, IRQ0, WKP7 to WKP0, or AEC interrupt in the standby mode.
   b. Perform interrupt handling.



Conditions at execution of SLEEP instruction

LSON	MSON	SSBY	TMA3	DTON
0	x	1	0	0

Note: x: Don't care

Condition for mode clearing by interrupt exception handling

Interrupt source
IRQ1, IRQ0, WKP7 to WKP0 interrupts, AEC

Note: A transition between different modes cannot be made to occur simply because of an interrupt source. Make sure that interrupt handling is performed after the interrupt request is accepted.

Figure 1 Mode Transition Diagram

4. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SYSCR1 System control register 1 Address: H'FFF0

Bit	Bit Name	Set Value	R/W	Description
7	SSBY	1	R/W	Software standby Selects the mode to transition to after execution of the SLEEP instruction. 0: A transition is made to the sleep mode or the subsleep mode. 1: A transition is made to the standby mode or the watch mode.
6	STS2	User defined	R/W	Standby timer selection 2 to 0 Specifies the number of wait states that must elapse after the system clock oscillator begins functioning until the clock is supplied when transitioning from the standby mode, the subactive mode, the subsleep mode, or the watch mode to the active mode or the sleep mode. The relationship between the specified value and the number of wait states is shown in table 3. The minimum value (STS2 = 1, STS1 = 0, STS0 = 1) is recommended if an external clock is used. If a setting other than the recommended value is used, operation may start before the end of the waiting time.
5	STS1	User defined	R/W	
4	STS0	User defined	R/W	
3	LSON	0	R/W	Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when the watch mode is cleared. 0: The CPU operates on the system clock (ϕ) 1: The CPU operates on the subclock (ϕ_{SUB})
2	TMA3	0	R/W	In combination with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2, TMA3 selects the mode to which transition is made after the SLEEP instruction is executed.

Table 3 Operating Frequency and Waiting Time

Bit				Waiting Time	
STS2	STS1	STS0	Number of Wait States	Operating Frequency: 5 MHz	Operating Frequency: 2 MHz
0	0	0	8,129 states	1.683 ms	4.1 ms
0	0	1	16,384 states	3.277 ms	8.2 ms
0	1	0	1,024 states	0.205 ms	0.521 ms
0	1	1	2,048 states	0.410 ms	1.024 ms
1	0	0	4,096 states	0.819 ms	2.048 ms
1	0	1	2 states (external clock input)	0.0004 ms	0.001 ms
1	1	0	8 states	0.002 ms	0.004 ms
1	1	1	16 states	0.003 ms	0.008 ms

Note: When an external clock is input, bits STS2 to STS0 should be set to the external clock input mode before mode transition is executed. These bits should not be set to the external clock input mode if an external clock is not used.

- SYSCR2 System control register 2 Address: H'FFF1

Bit	Bit Name	Set Value	R/W	Description
3	DTON	0	R/W	Direct transfer on flag Selects the mode to transition to after the SLEEP instruction is executed with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
2	MSON	User defined	R/W	Medium speed on flag Selects whether operation continues in the active (high-speed) or the active (medium-speed) mode after the standby mode, the watch mode, or the sleep mode is cleared. 0: Active (high-speed) mode 1: Active (medium-speed) mode

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

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