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H8/38076R

Multiprocessor Communication

Introduction

The multiprocessor communication function of the serial communication interface 3 (SCI3) is used to transmit data to multiple processors.

Target Device

H8/38076R

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1. Specifications 2
2. Description of Functions 3
3. Principles of Operation 8
4. Description of Software 9

1. Specifications

- The multiprocessor communication function is used to transmit data H'B8 to receiving station A and data H'DE to receiving station B.
- The format of the transmit data is 8-bit data length, 1 multiprocessor bit, and 1 stop bit.
- Data is transmitted at a bit rate of 31,250 bps, and a break is output after data transmission is completed.
- A sample connection diagram for communication between processors using data transfer in multiprocessor format is shown in figure 1.

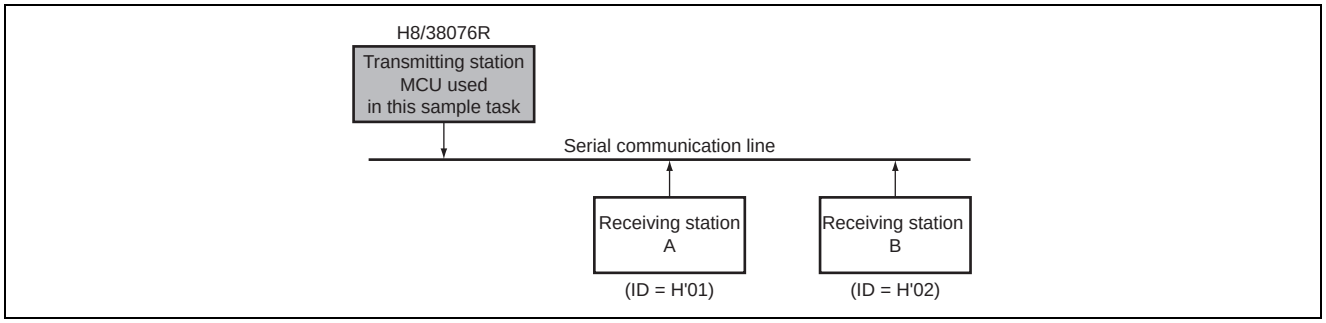


Figure 1 Communication Between Processors Using Data Transfer in Multiprocessor Format

2. Description of Functions

2.1 Functions Used

In this sample task the multiprocessor communication is implemented by using the serial communication interface 3 (SCI3) to transmit data. The functions used are described below.

1. System Clock (ϕ)
   This 10-MHz oscillation clock is the reference clock for operation of the CPU and peripheral functions.

2. Multiprocessor Communication Function
   Figure 2 shows the format of multiprocessor function. The multiprocessor communication function enables data transmission and reception in the asynchronous serial mode between multiple of processors sharing a communication line by adding a multiprocessor bit to the transfer data (multiprocessor format).
   When the multiprocessor communication is performed, each receiving station is assigned a unique ID code. The serial communication cycle consists of two component cycles: an ID transmission cycle, in which the receiving station is specified, and a data transmission cycle, in which the data is transmitted.
   The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle; if the multiprocessor bit is 0, the cycle is a data transmission cycle.
   The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a multiprocessor bit having a value of 1 added. It then sends transmit data as data with a multiprocessor bit having a value of 0 added.
   When data with the multiprocessor bit set to 1 is received, the receiving station compares that data with its own ID. If the station's ID matches it receives the data sent next. Stations whose IDs do not match continue to skip data until data with a multiprocessor bit set to 1 is again received.
   There are four transmission/reception formats from which to choose (refer to table 1). When the multiprocessor format is selected, the parity bit specification is invalid.

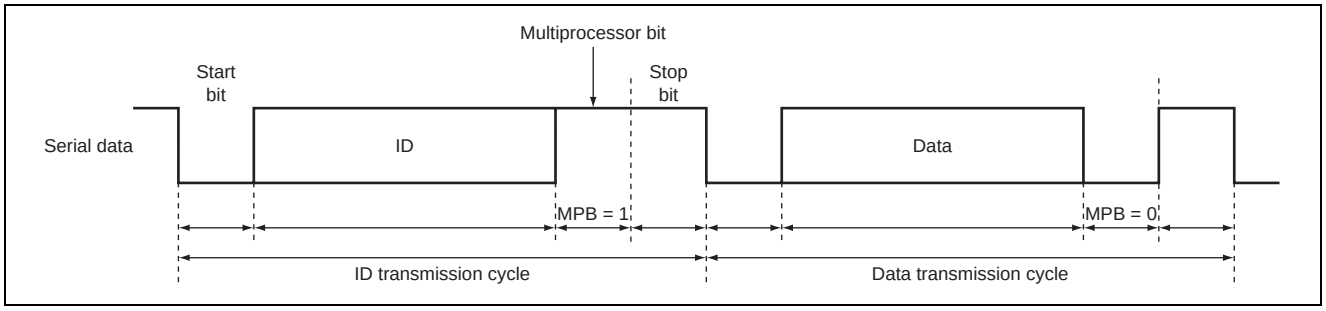


Figure 2 Multiprocessor Format

Table 1 Multiprocessor Communication Formats

SMR				Multiprocessor Communication Formats and Frame Lengths
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	1	0	START 8-bit data MPB STOP
0	0	1	1	START 8-bit data MPB STOP
1	0	1	0	START 7-bit data MPB STOP
1	0	1	1	START 7-bit data MPB STOP

<Legend>
START: Start bit
STOP: Stop bit
MPB: Multiprocessor bit

- Transmit shift register 3 (TSR3)
  TSR3 is a shift register for transmitting serial data. During serial data transmission the data written to transmit data register 3 (TDR3) is transferred automatically to TSR3 and then sent to the TXD31 or TXD32 pin in sequence, beginning with the LSB (least significant bit). However, data transfer from TDR3 to TSR3 is not performed if no data has been written to TDR3 (if the TDRE bit is set to 1). TSR3 cannot be directly accessed by the CPU.

- Transmit data register 3 (TDR3)
  TDR3 is an 8-bit register that stores data for transmission. When the SCI3 detects that TSR3 is empty it automatically transfers the data in TDR3 to TSR3. The double-buffered structure of TDR3 and TSR3 enables continuous serial transmission by successively writing data to TSR3. Transmit data is written to TDR3 only once when the TDRE bit in the serial communication interface 3 (SSR3) is set to 1. The initial value of TDR3 is H'FF. In the standby mode, the watch mode, the module standby mode, or at a reset, TDR3 is initialized to H'FF.

- Serial mode register 3 (SMR3)
  SMR3 is a register for selecting the serial communication format and the clock source for the internal baud rate generator. In this sample task the asynchronous mode, 8-bit data length, 1 stop bit, and the multiprocessor mode are selected; n = 0 is selected as the clock source.

- Serial control register 3 (SCR3)
  SCR3 is a register that controls transmission and reception and interrupts, and selects the transfer clock source. No interrupts are used in this sample task because data transfer is performed using polling.

- Serial status register 3 (SSR3)
  SSR3 consists of status flags and multiprocessor bits for transmission and reception. In this sample task control of multiprocessor bit transfer (MPBT) is performed, the TDRE bit is polled, and the next frame of data is written to TDR3 after the preceding frame has been transferred from TDR3 to TSR3.

- Serial port control register (SPCR)
  SPCR switches the functions of the TXD32 and TXD31 pins and controls data inversion of the transmit and receive pins. In this sample task the TXD31 pin is selected and data is output unmodified (without inversion).

- Bit rate register 3 (BRR3)
  BRR3 sets the bit rate. In this sample task it is set to N = 9 (10 MHz, n = 0) to obtain a transfer clock of 31,250 bps. For details, refer to the hardware manual.

A block diagram of the serial communication interface 3 is shown in figure 3.

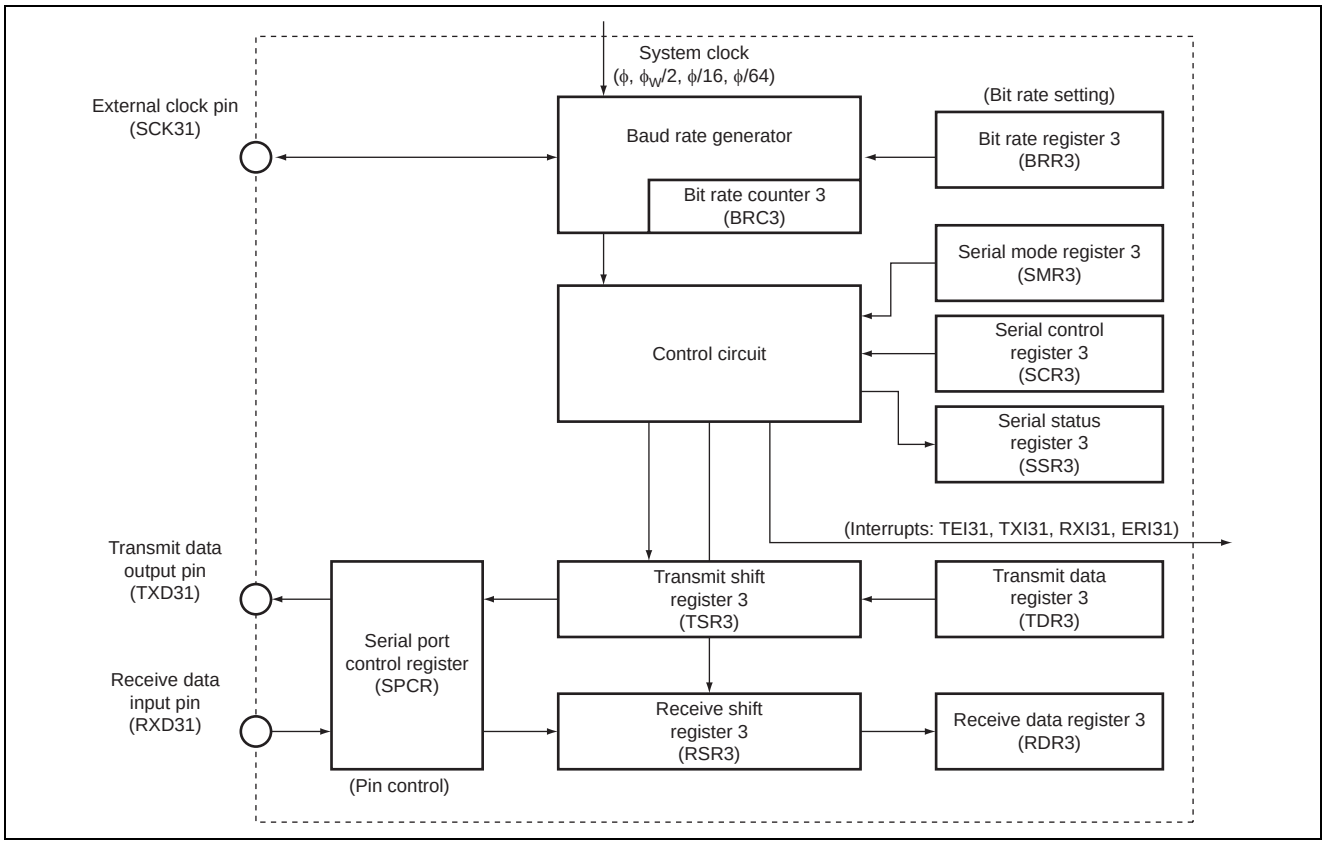


Figure 3 Block Diagram of SCI3

Table 2 shows example BBR3 settings for the asynchronous mode. The values listed in table 2 assume the active mode and an oscillation frequency of 10 MHz.

Table 2 Example BBR3 Settings at Different Bit Rates (Asynchronous Mode)

R bit rate (bps)	110	150	200	250	1200	2400	31250
n	2	2	2	2	2	0	0
N	177	129	97	77	15	129	9
Error (%)	–0.25	0.16	–0.35	0.16	1.73	0.16	0.00

Notes: 1. Select set values that produce an error of 1% or less.
2. The equation shown below is used to calculate set values for BRR3.

$$\text{N (BRR3 set value)} = \frac{\phi}{32 \times 2^{2n} \times \text{bit rate}} - 1$$

$$= \frac{10\ \text{MHz}}{32 \times 2^{2 \times 0} \times 31250} - 1$$

$$= 9$$

$$\text{Error (\%)} = \frac{\text{B (bit rate obtained from n, N, and OSC)} - \text{R (bit rate from table 2)}}{\text{R (bit rate from table 2)}} \times 100$$

<Legend>
B: B: Bit rate (bps)
N: BRR3 set value for baud rate generator (0 = N = 255)
OSC: ϕ_{OSC} value (Hz)
n: No. (n = 0, 2, 3) of input clock of baud rate generator

Table 3 Relationship between n and Clock

		SMR3 Set Values	
n	**Clock**	**CKS1**	**CKS0**
0	ϕ	0	0
0	$\phi_W/2$, ϕ_W	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

3. Asynchronous Mode

In the asynchronous mode, characters consisting of data to which a start bit signifying the start of data transfer and a stop bit signifying the end of data transfer are transmitted and received. It is a serial communication mode in which synchronization is performed in character units.

Inside the SCI3 the transmitter and receiver are independent units, enabling full duplex operation. Both the transmitter and the receiver have a double-buffered structure, so data can be read or written while transmission or reception are in progress, enabling continuous data transfer.

The communication line is maintained at mark state (high level) in the asynchronous mode. The SCI3 monitors the communication line and when a space (low level) occurs, it interprets it as a start bit and starts serial communication.

Each character consists of a start bit (low level), followed by data (in LSB-first order, meaning beginning from the lowest bit), a parity bit (high or low level), and finally a stop bit (high level).

In the asynchronous mode synchronization is performed on the falling edge of the start bit during reception. The data is sampled on the 8th pulse of a clock with a frequency 16 times the bit period, so that the transfer data is fetched at the center of each bit.

4. Interrupts

   The SCI3 has a total of six interrupt sources, which are assigned a common vector address: transmit end, transmit data empty, receive data full, and three types of receive errors (overrun error, framing error, and parity error). (Note that the parity setting is invalid in multiprocessor format.)

   Interrupt requests can be enabled or disabled by the TIE3 and RIE3 bits in SCR3.

   When the TDRE bit in SSR3 is set to 1, a TXI3 interrupt is requested. When the TEND bit in SSR3 is set to 1, a TEI3 interrupt is requested. These two interrupts are generated during transmission.

   The initial value of the TDRE flag in SSR3 is 1. Thus, if the TIE3 bit in SCR3 is set to 1 to enable transmit data empty interrupt requests (TXI3) before the transmit data is transmitted to TDR3, a TXI3 interrupt request is generated even if the transmit data is not ready.

   The initial value of the TEND flag in SSR3 is 1. Thus, if the TEIE bit in SCR3 is set to 1 to enable transmit end interrupt requests (TEI3) before the transmit data is transmitted to TDR3, a TEI3 interrupt request is generated even if the transmit data has not been sent.

   It is possible to make effective use of these interrupt requests by using interrupt routines to transfer transmit data to TDR3. To prevent the generation of these interrupt requests (TXI3 and TEI3), set the enable bits (TIE and TEIE) that correspond to them to 1 after transferring the transmit data to TDR3.

   An RXI3 interrupt is requested when the RDRF bit in SSR3 is set to 1. An ERI3 interrupt is requested if the OER, PER, or FER bit is set to 1. These two interrupt requests are generated during reception.

2.2 Assignment of Functions

Table 4 shows the assignment of functions in this sample task. Multiprocessor transmission is performed using functions assigned as shown in table 4.

Table 4 Assignment of Functions

Elements	Description
TDR3	8-bit register for storing transmit data
SMR3	Selects the asynchronous mode, selects ϕ as clock source for baud rate generator, selects 8-bit data length, 1 stop bit, and the multiprocessor mode
SCR3	Enables transmission, selects internal baud rate generator as clock source
SSR3	Flag that indicates the operating status
BRR3	Sets the bit rate (31,250 bps)
SPCR	Selects the TXD31 pin function, specifies that data is output unmodified (without inversion)
TXD31	Transmit data output pin of SCI3

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 4. Multiprocessor transmission is performed using the hardware and software processing shown in figure 4.

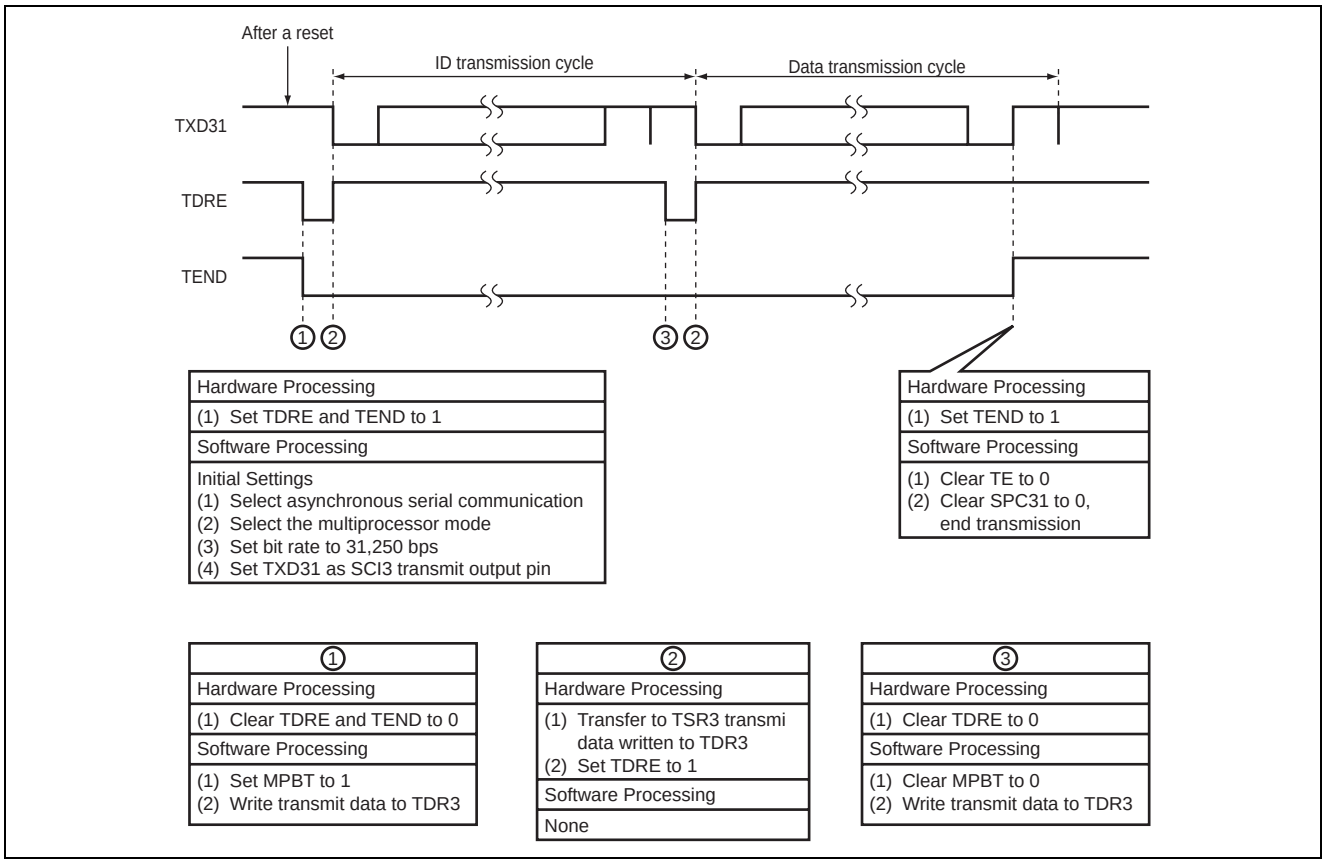


Figure 4 Principles of Operation for Multiprocessor Serial Data Communication

4. Description of Software

In this sample task the serial communication interface 3 (SCI3) is used to perform the multiprocessor communication. The functions used as listed below.

4.1 Functions

Table 5 List of Functions

Function Name	Description
main	Controls multiprocessor transmission in the asynchronous mode
init_sci3	Initializes SCI3
trns_sci3	Performs multiprocessor transmission in the asynchronous mode
stop_sci3	Ends the asynchronous mode

4.2 Constants

Table 6 shows the constants used in this sample task.

Table 6 Constants

Label Name	Constant Value	Description	Used in
DATA_NUM	4	Transmit data size	main
ID1	H'01	ID address of receiving station A	main
ID2	H'02	ID address of receiving station B	main

4.3 RAM Usage

No RAM is used in this sample task.

4.4 Modules

4.4.1 main() Function

1. Module Specifications

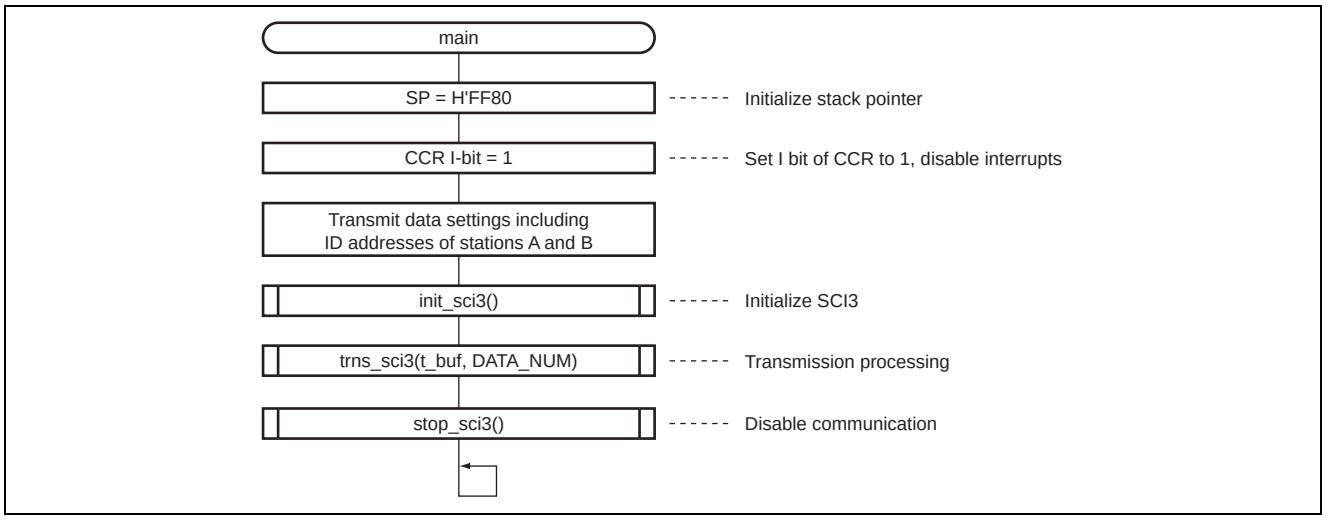
- Controls multiprocessor transmission in the asynchronous mode

Table 7 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   None

3. Flowchart



4.4.2 init_sci3 Function

1. Module Specifications

- Initializes SCI3

Table 8 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SPCR Serial port control register Address: H'FF91

Bit	Bit Name	Set Value	R/W	Description
4	SPC31	1	R/W	P42/TXD31 pin function switch Selects whether pin P42/TXD31 functions as P42 or as TXD31. 0: Functions as P42 I/O pin 1: Functions as TXD31 output pin Set the TE bit in SCR after setting this bit to 1.
1	SCINV1	0	R/W	TXD31 pin output data inversion switch Specifies whether output data of the TXD31 pin is inverted or not. 0: TXD31 output data not inverted 1: TXD31 output data inverted

- SMR3 Serial mode register 3 Address: H'FF98

Bit	Bit Name	Set Value	R/W	Description
7	COM	0	R/W	Communication mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character length (enabled only in the asynchronous mode) 0: Data length of 8 or 5 bits used for transmission and reception
3	STOP	0	R/W	Stop bit length (enabled only in the asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits Only the first stop bit is checked during reception, regardless of the value of the STOP bit. If the second stop bit is 0, it is treated as the start bit of the next transmit character.
2	MP	1	R/W	Multiprocessor mode The multiprocessor communication function is enabled when this bit is set to 1. The PE and PM bit settings become invalid. Set this bit to 0 in the clock-synchronous mode.
1	CKS1	0	R/W	Clock selection 0 and 1
0	CKS0	0	R/W	These bits select the clock source for the internal baud rate generator. 00: ϕ clock (n = 0)

- BRR3 Bit rate register 3 Address: H'FF99

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	0	R/W	BRR3 is an 8-bit readable/writable register that selects the bit rate. The initial value is H'FF. The bit rate is determined in the clock-synchronous mode by the n setting of bits CKS1 and CKS0 in SMR3 in combination with the N setting of BRR3. Refer to the hardware manual for details. In this sample task BRR3 is set to H'09 to obtain a bit rate of 31,250 bps.
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	1	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	1	R/W	

- SCR3 Serial control register 3 Address: H'FF9A

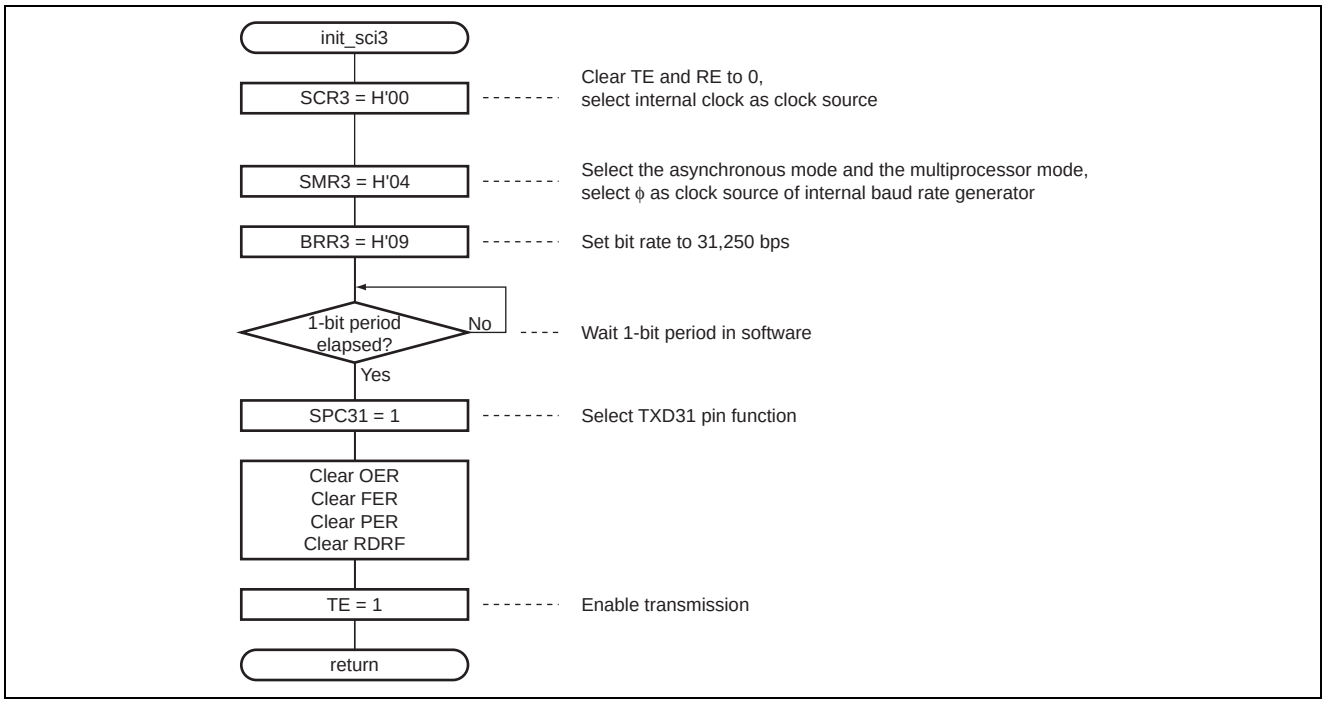
Bit	Bit Name	Set Value	R/W	Description
5	TE	1	R/W	Transmit enable Transmission is enabled when this bit is set to 1. When the TE bit is 0, the TDRE bit in SSR3 is fixed at 1. When transmit data is written in TDR3 while TE is 1, the TDRE bit in SSR3 is cleared to 0 and serial data transmission starts. Be sure to make SMR3 settings and set the SPC31 or SPC32 bit in SPCR to decide the transmission format before setting the TE bit to 1.
1	CKE1	0	R/W	Clock enable 0 and 1
0	CKE0	0	R/W	Selects the clock source. Asynchronous mode 00: Internal baud rate generator (SCK31 or SCK32 pin functions as an I/O port)

- SSR3 Serial status register 3 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
6	RDRF	0	R/(W)*	Receive data register full Indicates whether or not receive data is stored in RDR3. [Setting condition] • When reception ends normally and receive data is transferred from RSR3 to RDR3 [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When data is read from RDR3 In this sample task RDRF is only cleared when SCI3 is initialized.
5	OER	0	R/(W)*	Overrun error [Setting condition] • When an overrun error occurs during reception [Clearing condition] • When 0 is written to the OER bit after it was read as 1 When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1.
4	FER	0	R/(W)*	Framing error [Setting condition] • When a framing error occurs during reception [Clearing condition] • When 0 is written to FER after it was read as 1 When the RE bit in SCR is cleared to 0, the FER bit is not affected and retains its previous state. Note that in the 2-stop-bit mode only the first stop bit is checked for a value of 1, and the second stop bit is not checked. When a framing error occurs, the receive data is transferred to RDR3 but the RDRF bit is not set. Reception cannot be continued with the FER bit set to 1.
3	PER	0	R/(W)*	Parity error [Setting condition] • When a parity error is generated during reception [Clearing condition] • When 0 is written to the PER bit after it was read as 1 In this sample task PER is cleared only when SCI3 is initialized.

Note: * Only 0 can be written to clear the flag.

3. Flowchart


init_sci3
SCR3 = H'00
Clear TE and RE to 0,
select internal clock as clock source
SMR3 = H'04
Select the asynchronous mode and the multiprocessor mode,
select ϕ as clock source of internal baud rate generator
BRR3 = H'09
Set bit rate to 31,250 bps
1-bit period elapsed?
No
Yes
Wait 1-bit period in software
SPC31 = 1
Select TXD31 pin function
Clear OER
Clear FER
Clear PER
Clear RDRF
TE = 1
Enable transmission
return

4.4.3 trns_sci3() Function

1. Module Specifications

- Performs multiprocessor transmission in the asynchronous mode

Table 9 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char*	t_ptr	Transmit data pointer
	unsigned char*	num	Transmission count

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- TDR3 Transmit data register 3 Address: H'FF9B

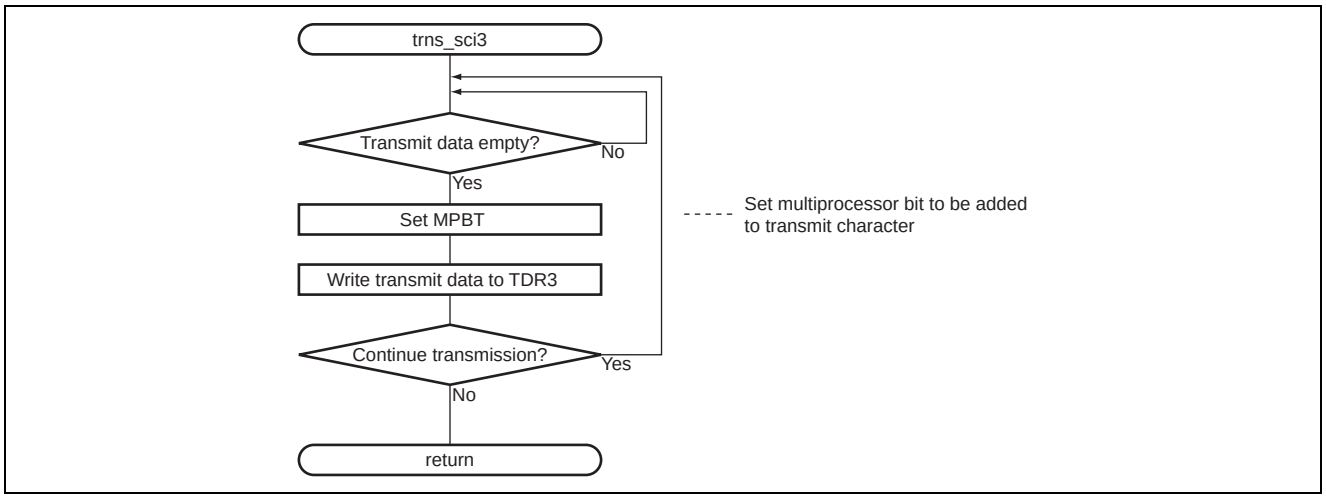
Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R/W	TDR3 is an 8-bit register that stores data for transmission. When the SCI3 detects that TSR3 is empty it transfers to TSR3 the transmit data that was written to TDR3 and starts transmission. The double-buffered structure of TDR3 and TSR3 enables continuous serial transmission. If the next frame of transmit data has already been written to TDR3 while transmission of the current frame is in progress, data transfer to TSR3 continues without pause. To achieve reliable serial transmission, write transmit data to TDR3 only once after confirming that the TDRE bit in SSR3 is set to 1. The initial value of TDR3 is H'FF. In the standby mode, the watch mode, the module standby mode, or at a reset, TDR3 is initialized to H'FF.
6	Bit 6	Undefined	R/W	
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

- SSR3 Serial status register 3 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit data register empty Indicates whether or not transmit data is stored in TDR3. [Setting conditions] • When the TE bit in SCR3 is 0 • When data is transferred from TDR3 to TSR3 [Clearing conditions] • When 0 is written to TDRE after it was read as 1 • When transmit data has been written to TDR3
0	MPBT	Undefined	R/W	Multiprocessor bit transfer MPBT specifies the multiprocessor bit value to be added to the transmit character.

Note: * Only 0 can be written to clear the flag.

3. Flowchart


trns_sci3
Transmit data empty?
No
Yes
Set MPBT
Write transmit data to TDR3
Continue transmission?
Yes
No
return
Set multiprocessor bit to be added
to transmit character

4.4.4 stop_sci3() Function

1. Module Specifications

- Ends the asynchronous mode

Table 10 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SPCR Serial port control register Address: H'FF91

Bit	Bit Name	Set Value	R/W	Description
4	SPC31	0	R/W	P42/TXD31 pin function switch Selects whether pin P42/TXD31 functions as P42 or as TXD31. 0: Functions as P42 I/O pin 1: Functions as TXD31 output pin Set the TE bit in SCR3 after setting this bit to 1.

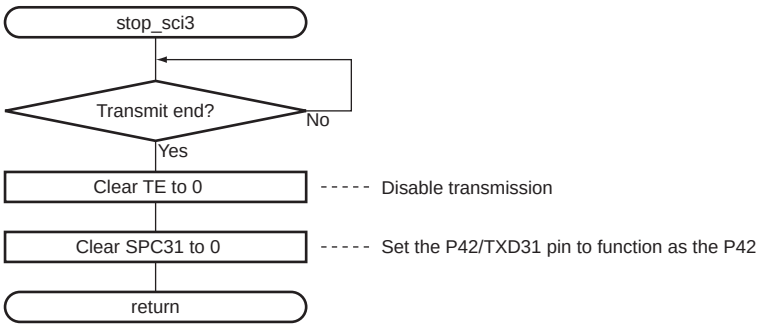
- SCR3 Serial control register 3 Address: H'FF9A

Bit	Bit Name	Set Value	R/W	Description
5	TE	0	R/W	Transmit enable Transmission is enabled when this bit is set to 1. When the TE bit is 0, the TDRE bit in SSR3 is fixed at 1. When transmit data is written to TDR3 while TE is 1, the TDRE bit in SSR3 is cleared to 0 and serial data transmission starts. Be sure to make SMR3 settings and set the SPC31 or SPC32 bit in SPCR to decide the transmission format before setting the TE bit to 1.

- SSR3 Serial status register 3 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
2	TEND	Undefined	R	Transmit end [Setting conditions] • When the TE bit in SCR3 is 0 • When TDRE is 1 at transmission of the last bit of a transmit character [Clearing conditions] • When 0 is written to the TDRE bit after it was read as 1 • When transmit data has been written in the TDR3 register

3. Flowchart



4.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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