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April 1st, 2010
Renesas Electronics Corporation

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H8/38076R

Measuring Number of Input Pulses Using 16-Bit Event Counter Function of Timer F

Introduction
The 16-bit event counter function of timer F is used to count the rising edges of pulses input to the timer F event input (TMIF) pin.

Target Device
H8/38076R

Contents

1. Specifications .................................................................................................................................. 2
2. Description of Functions .................................................................................................................. 2
3. Principles of Operation .................................................................................................................... 4
4. Description of Software .................................................................................................................. 5
5. Flowchart ....................................................................................................................................... 8
1. Specifications

In this sample task timer counter F (TCF) is set to count the rising edges of an external clock input to the timer F event input (TMIF) pin. Timer counter F continues counting up until the rising edge count reaches 1,024.

2. Description of Functions

2.1 Functions

When the rising edge count reaches 1,024 the external clock input to TCF is halted and the sample task ends. In this sample task the 16-bit event counter function of timer counter F is used to measure the number of pulses input to the TMIF pin. A block diagram of the 16-bit event counter function of timer F is shown in figure 1. The 16-bit event counter function of timer F is described below.

1. Timer F Functions

This 16-bit timer has an output compare function. It can be used for external event counting or as a multifunction timer for a variety of applications, including counter resetting, interrupt request, and toggle output using compare match signals. It can also be used as two independent 8-bit timers (timer FH and timer FL).

- Timer counter F (TCF)
  TCF is a 16-bit readable/writeable up-counter that is incremented by input of an internal or an external clock. Five input clock options are available: the system clock divided by 4, 16, or 32; the subclock divided by 4; or an external clock.
  In this sample task external clock is selected as the TCF input clock.
- Timer control register F (TCRF)
  TCRF is an 8-bit readable/writeable register used for switching between 16-bit mode and 8-bit mode and for selecting among the four internal clocks and an external event.
- Timer control/status register F (TCSRF)
  TCSRF is an 8-bit register used for counter clear selection, overflow flag and compare match flag settings, and controlling the enabling of overflow interrupt requests.

2. I/O Port Functions

The following port setting is performed.

- Port mode register 4 (PMR4)
  PMR4 is used to set the P40/SCK31/TMIF pin as a TMIF pin.

3. Interrupt Controller Functions

The following registers are used to control interrupts.

- Interrupt enable register 2 (IENR2)
  IENR2 controls timer F interrupts.
- Interrupt request register 2 (IRR2)
  IRR2 is the interrupt request status register for timer F interrupts.
2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. With functions assigned as shown in table 1 the 16-bit event counter function of timer F is used to measure the number of input pulses.

Table 1 Assignment of Functions

<table>
<thead>
<tr>
<th>Elements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCF</td>
<td>16-bit counter using external clock input</td>
</tr>
<tr>
<td>TCRF</td>
<td>Sets TCF to 16-bit mode, selects external clock as TCF input clock</td>
</tr>
<tr>
<td>TCSRF</td>
<td>Timer F status register, enables TCF overflow interrupts, disables clearing TCF by compare match</td>
</tr>
<tr>
<td>IENTFH</td>
<td>Enables interrupt requests at timer F overflow</td>
</tr>
<tr>
<td>IRRTFH</td>
<td>Interrupt flag set by timer F overflow</td>
</tr>
<tr>
<td>TMIF</td>
<td>Input pin for external event input to TCFL</td>
</tr>
</tbody>
</table>
3. **Principles of Operation**

The principles of operation of this sample task are illustrated in figure 2. Using the hardware and software processing shown in figure 2 the 16-bit event counter function of timer F is used to measure the number of input pulses.

![Figure 2 Principles of Operation](image-url)

**Figure 2 Principles of Operation**
4. Description of Software

4.1 Description of Modules

Table 2 shows the modules used in this sample task.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>Settings for timer F 16-bit event counter function, selects external clock the TCF input clock source, enables interrupts, ends when TCF input clock rising edge count reaches 1,024</td>
</tr>
<tr>
<td>tfint</td>
<td>During timer F overflow interrupt handling, sets 1 to ENDF and disables timer F interrupt requests</td>
</tr>
</tbody>
</table>

4.2 Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

The internal registers used in this sample task are shown below.

- **TCRF**  
  Timer Control Register F  
  Address: H'FFB6

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>CKSH2</td>
<td>0</td>
<td>W</td>
<td>Clock Select H</td>
</tr>
<tr>
<td>5</td>
<td>CKSH1</td>
<td>0</td>
<td>W</td>
<td>Selects the clock input to TCFH from among internal clock sources or TCFL overflow.</td>
</tr>
<tr>
<td>4</td>
<td>CKSH0</td>
<td>0</td>
<td>W</td>
<td>000: 16-bit mode, counting on TCFL overflow signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001: 16-bit mode, counting on TCFL overflow signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010: 16-bit mode, counting on TCFL overflow signal</td>
</tr>
<tr>
<td>2</td>
<td>CKSL2</td>
<td>0</td>
<td>W</td>
<td>Clock Select L</td>
</tr>
<tr>
<td>1</td>
<td>CKSL1</td>
<td>0</td>
<td>W</td>
<td>Select the clock input to TCFL from among internal clock sources or external event input.</td>
</tr>
<tr>
<td>0</td>
<td>CKSL0</td>
<td>0</td>
<td>W</td>
<td>000: Counting on rising or falling edge of an external event (TMIF pin)*</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001: Counting on rising or falling edge of an external event (TMIF pin)*</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010: Counting on rising or falling edge of an external event (TMIF pin)*</td>
</tr>
</tbody>
</table>

Note: * The TMIFEG bit in IEGR selects which edge of an external event is used for counting.
### Measuring Number of Input Pulses Using 16-Bit Event Counter Function of Timer F

**TCSRF**  
Timer Control/Status Register F  
Address: H'FFB7

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | OVFH     | Undefined | R/W | Timer Overflow Flag H  
[Setting condition]  
• When TCFH overflows from H'FF to H'00  
[Clearing condition]  
• When 0 is written to this bit after reading it as 1 |
| 5   | OVIEH    | 1         | R/W | Timer Overflow Interrupt Enable H  
Enables or disables interrupt generation when TCFH overflows.  
1: TCFH overflow interrupt requests enabled |
| 4   | CCLRH    | 0         | R/W | Counter Clear H  
In 16-bit mode this bit selects whether TCF is cleared when TCF and OCRF match.  
In 16-bit mode:  
0: TCF clearing by compare match disabled |

Note: * Only 0 can be written to clear the flag.

**TCF**  
Timer Counter F  
Address: H'FFB8

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Bit 15</td>
<td>Undefined</td>
<td>R/W</td>
<td>Output Compare Register F</td>
</tr>
<tr>
<td>14</td>
<td>Bit 14</td>
<td>Undefined</td>
<td>R/W</td>
<td>When CKSH2 in TCRF is set to 0 TCF operates as a 16-bit counter. The TCF input clock is selected by bits CKSL2 to CKSL0 in TCF.</td>
</tr>
<tr>
<td>13</td>
<td>Bit 13</td>
<td>Undefined</td>
<td>R/W</td>
<td>TCF can be cleared in the event of a compare match by CCLRH in TCSR F.</td>
</tr>
<tr>
<td>12</td>
<td>Bit 12</td>
<td>Undefined</td>
<td>R/W</td>
<td>When TCF overflows from H'FFFF to H'0000, OVFH in TCSR F is set to 1. If the value of OVIEH in TCSR F is 1 at this time, IRTF in IRR2 is set to 1, and if in addition the value of IENF in IENR2 is 1, an interrupt request is sent to the CPU.</td>
</tr>
<tr>
<td>9</td>
<td>Bit 9</td>
<td>Undefined</td>
<td>R/W</td>
<td>When TCF overflows from H'FFFF to H'0000, OVFH in TCSR F is set to 1. If the value of OVIEH in TCSR F is 1 at this time, IRTF in IRR2 is set to 1, and if in addition the value of IENF in IENR2 is 1, an interrupt request is sent to the CPU.</td>
</tr>
<tr>
<td>8</td>
<td>Bit 8</td>
<td>Undefined</td>
<td>R/W</td>
<td>TCF can be cleared in the event of a compare match by CCLRH in TCSR F.</td>
</tr>
<tr>
<td>7</td>
<td>Bit 7</td>
<td>Undefined</td>
<td>R/W</td>
<td>When TCF overflows from H'FFFF to H'0000, OVFH in TCSR F is set to 1. If the value of OVIEH in TCSR F is 1 at this time, IRTF in IRR2 is set to 1, and if in addition the value of IENF in IENR2 is 1, an interrupt request is sent to the CPU.</td>
</tr>
<tr>
<td>6</td>
<td>Bit 6</td>
<td>Undefined</td>
<td>R/W</td>
<td>TCF can be cleared in the event of a compare match by CCLRH in TCSR F.</td>
</tr>
<tr>
<td>5</td>
<td>Bit 5</td>
<td>Undefined</td>
<td>R/W</td>
<td>TCF can be cleared in the event of a compare match by CCLRH in TCSR F.</td>
</tr>
<tr>
<td>4</td>
<td>Bit 4</td>
<td>Undefined</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Bit 3</td>
<td>Undefined</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Bit 2</td>
<td>Undefined</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Bit 1</td>
<td>Undefined</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Bit 0</td>
<td>Undefined</td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

**PMR4**  
Port Mode Register 4  
Address: H'FFC3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0   | TMIF     | 1         | R/W | P40/SCK31/TMIF pin function switch  
Selects whether pin P40/SCK31/TMIF is used as P40/SCK31 or as TMIF.  
0: Functions as P40/SCK31 I/O pin  
1: Functions as TMIF input pin |
• **IEGR**  
  **Interrupt Edge Select Register**  
  Address: H'FFF2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 6   | TMIFEG   | 1         | R/W | TMIF Edge Select  
  0: Detects the falling edge of the TMIF pin input  
  1: Detects the rising edge of the TMIF pin input |

• **IENR2**  
  **Interrupt Enable Register 2**  
  Address: H'FFF4

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3   | IENTFH    | 1         | R/W | Timer FH Interrupt Enable  
  Timer FH interrupt requests are enabled when this bit is set to 1.  
  1: Timer FH interrupt requests enabled |

• **IRR2**  
  **Interrupt Request Register 2**  
  Address: H'FFF7

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3   | IRRTFH    | Undefined | R/W | Timer FH Interrupt Request Flag  
  [Setting condition]  
  • When timer FH compare match or overflow occurs  
  [Clearing condition]  
  • When 0 is written to this bit |

### 4.4 RAM Usage

The RAM usage in this sample task is shown in table 3.

**Table 3 RAM Usage**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Description</th>
<th>Amount of Memory Used</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ENDF</td>
<td>Flag indicating that rising edge of input pulse has been detected 1,024 times</td>
<td>1 bit</td>
<td>main tflint</td>
</tr>
</tbody>
</table>
5. Flowchart

5.1 main

```
main

   SP = H'FF80
   CCR I-bit = 1
   ENDF = 0
   TMIF = 1
   TMIFEG = 1
   TCRF = H'00
   tmp = TCSRFF
   TCSRFF = H'20
   TCF = H'FC00
   IRRTFH = 0
   IENTFH = 1
   CCR I-bit = 0
   ENDF != 1 ?
      Yes
      TCRF = H'06
      No

```

- Initialize stack pointer
- Set 1 to I bit in CCR, disable interrupts
- Initialize RAM area to be used
- Set as timer F event input pin (TMIF pin)
- Select rising edge detection of TMIF pin input
- Set TCF to 16-bit mode, count TCF on rising edge of external input (TMIF pin)
- Enable interrupt requests at TCF overflow, clear OVFH and CMFH, disable clearing of TCF at compare match of TCF and OCRF
- Initialize TCF
- Clear IRRTFH
- Enable TCFH interrupt requests (compare match, overflow)
- Set 1 to I bit in CCR, enable interrupts
- Event count finished?
- Disable external event clock input to TCF

5.2 tfint

```

```
## 5.3 Link Address Specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVECT</td>
<td>H'0000</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
<tr>
<td>B</td>
<td>H'F780</td>
</tr>
</tbody>
</table>
# Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.18.05</td>
<td></td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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