To our customers,

Old Company Name in Catalogs and Other Documents

On April 1\textsuperscript{st}, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: \url{http://www.renesas.com}

April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (\url{http://www.renesas.com})

Send any inquiries to \url{http://www.renesas.com/inquiry}. 
Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.

2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.

4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.

5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.

6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depend on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheet or data books, etc.

“Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

“High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

“Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.
H8/38076R
Asynchronous Serial Data Reception

Introduction
Serial data is received using the asynchronous mode of the serial communication interface 3 (SCI3).

Target Device
H8/38076R

Contents

1. Specifications .................................................................................................................. 2
2. Description of Functions .................................................................................................. 3
3. Principles of Operation ................................................................................................... 6
4. Description of Software ................................................................................................. 7
1. Specifications

- Asynchronous serial data transfer is employed to receive 4 bytes of 8-bit data using channel 1.
- The format of the receive data is set to 8-bit data length, odd parity, and 1 stop bit.
- The bit rate is 31,250 bps. The task finishes after 4 bytes of data have been received.
- Figure 1 shows a connection diagram for serial data reception in the asynchronous mode.
- Figure 2 shows the data format for serial data reception in the asynchronous mode.
2. Description of Functions

2.1 Functions Used

In this sample task serial data is transmitted using the asynchronous mode of the serial communication interface 3 (SCI3). A block diagram of the serial communication interface 3 is shown in figure 3, and the functions used in this sample task are described below.

1. System Clock (\( \phi \))
   This 10-MHz oscillation clock is the reference clock for operation of the CPU and peripheral functions.

2. SCI3 Asynchronous Mode
   Each character of transfer data consists of a start bit (low level), followed by transmit/receive data (in LSB-first order), a parity bit, and finally a stop bit (high level). In the asynchronous mode, synchronization is performed on the falling edge of the start bit during reception. The data is sampled on the 8th pulse of a clock with a frequency 16 times the bit period, so the transfer data is fetched at the center of each bit. The transmitter and receiver are independent units inside the SCI3, enabling full duplex operation. Both the transmitter and the receiver also have a double-buffered structure, so the next data can be written while transmission is in progress and the preceding data can be read while reception is in progress, enabling continuous data transfer.

- Receive shift register 3 (RSR3)
  RSR3 is a shift register that receives serial data input from the RXD31 or RXD32 pin and converts it into parallel data. When one frame of data has been received, it is transferred automatically to RDR3. RSR3 cannot be directly accessed by the CPU.

- Receive data register 3 (RDR3)
  RDR3 is an 8-bit register that stores receive data. When one frame of data has been received, it is transferred from RSR3 to RDR3, enabling RSR3 to receive the next frame of data. RSR3 and RDR3 have a double-buffered structure, so continuous reception is possible. Read RDR3 only once, after confirming that the RDRF bit in SSR3 is set to 1. RDR3 cannot be written by the CPU. The initial value of RDR3 is H'00. RDR3 is initialized to H'00 at a reset, in the standby mode, watch mode, or module standby mode.

- Serial mode register 3 (SMR3)
  SMR3 is a register for selecting the serial communication format and the clock source for the internal baud rate generator. In this sample task the asynchronous mode is selected and \( n = 0 \) is selected as the clock source.

- Serial control register 3 (SCR3)
  SCR3 is a register that controls transmission, reception, and interrupts, and selects the clock source.

- Serial status register 3 (SSR3)
  SSR3 consists of status flags and multiprocessor bits for transmission and reception. In this sample task the RDRF bit is polled and the receive data is read in after the preceding frame has been transferred from RSR3 to RDR3.

- Serial port control register (SPCR)
  SPCR switches the functions of the TXD32 and TXD31 pins and controls data inversion of the transmit and receive pins. In this sample task the TXD31 pin is selected and data is input unmodified (without inversion).
- **Bit rate register 3 (BRR3)**

  BRR3 sets the bit rate. In this sample task it is set to \( N = 9 \) (10 MHz, \( n = 0 \)) to obtain a bit rate of 250 Kbps. The equation used to calculate the setting is shown below.

  \[
  N \text{ (set value of BRR3)} = \frac{6}{32 \times 2^n \times \text{bit rate}} - 1
  \]

  \[
  = \frac{10 \text{ MHz}}{32 \times 2^2 \cdot 5 \times 31250} - 1
  \]

  \[
  = 9
  \]

![Figure 3 Block Diagram of SCI3](image-url)
2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Serial data reception in the asynchronous mode is performed using functions assigned as shown in table 1.

<table>
<thead>
<tr>
<th>Elements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDR3</td>
<td>8-bit register for storing receive data</td>
</tr>
<tr>
<td>SMR3</td>
<td>Sets the asynchronous mode and selects φ as clock source for baud rate generator</td>
</tr>
<tr>
<td>SCR3</td>
<td>Enables reception, sets internal clock as clock source</td>
</tr>
<tr>
<td>SSR3</td>
<td>Status flag showing the operating status of the SCI3</td>
</tr>
<tr>
<td>BRR3</td>
<td>Sets the bit rate (31,250 bps)</td>
</tr>
<tr>
<td>SPCR</td>
<td>Specifies the data is input to the RXD31 pin unmodified (without inversion)</td>
</tr>
<tr>
<td>RXD31</td>
<td>Receive data input pin of SCI3</td>
</tr>
</tbody>
</table>
3. Principles of Operation

The principles of operation for this sample task are illustrated in figure 4. Serial data reception in the asynchronous mode is implemented using the software and hardware processing shown below.

![Diagram](image-url)

**Figure 4  Principles of Operation for Serial Data Reception in the Asynchronous Mode**
4. Description of Software

In this sample task serial data is received in the asynchronous mode. The functions used are listed below.

4.1 Functions

Table 2 List of Functions

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>Controls serial data reception in the asynchronous mode, sets receive buffer</td>
</tr>
<tr>
<td>init_sci3</td>
<td>Initializes SCI3</td>
</tr>
<tr>
<td>recv_sci3</td>
<td>Receives serial data in the asynchronous mode</td>
</tr>
<tr>
<td>stop_sci3</td>
<td>Ends the asynchronous mode</td>
</tr>
</tbody>
</table>

4.2 Constants

The constants used in this sample task are listed in table 3.

Table 3 Constants

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Constant Value</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA_NUM</td>
<td>4</td>
<td>Receive data size</td>
<td>main</td>
</tr>
</tbody>
</table>

4.3 RAM Usage

No RAM is used in this sample task.
4.4 Modules

4.4.1 main() Function

1. Module Specifications
   - Controls serial data reception in the asynchronous mode, sets receive buffer

<table>
<thead>
<tr>
<th>Table 4 Module Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Item</strong></td>
</tr>
<tr>
<td>Arguments</td>
</tr>
</tbody>
</table>

2. Internal Registers Used
   None

3. Flowchart

```
main

SP = H'FF80
----- Initialize stack pointer

CCR l-bit = 1
----- Set 1 to CCR l-bit to disable interrupts

Receive buffer settings

init_sci3()
----- Initialize SCI3

err = recv_sci3(r_buf, DATA_NUM)
----- Reception processing

stop_sci3()
----- Disable communication

Error?

Yes

Error handling

No
```

No
4.4.2 init_sci3 Function

1. Module Specifications
   - Initializes the asynchronous mode

2. Internal Registers Used
   The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

   - SPCR  Serial Port Control Register
     Address: H'FF91

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SCINV0</td>
<td>0</td>
<td>R/W</td>
<td>RXD31 Pin Input Data Inversion Switch</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Specifies whether data input to the RXD31 pin is inverted or not.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: RXD31 input data not inverted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: RXD31 input data inverted</td>
</tr>
</tbody>
</table>

Table 5 Module Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Type</th>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arguments</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>
## SMR3 Serial Mode Register 3

**Address:** HFF98

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | COM      | 0         | R/W | Communication Mode  
|     |          |           |     | 0: Asynchronous mode  
|     |          |           |     | 1: Clock-synchronous mode |
| 6   | CHR      | 0         | R/W | Character Length (enabled only in the asynchronous mode)  
|     |          |           |     | 0: Data length of 8 or 5 bits used for transmission and reception  
|     |          |           |     | 1: Data length of 7 or 5 bits used for transmission and reception  
|     |          |           |     | When 7-bit data is selected, the MSB (bit 7) in TDR3 is not transmitted. To select 5 bits as the data length, set both the PE and MP bits to 1. In this case the three most significant bits (bits 7, 6, and 5) in TDR3 are not transmitted. |
| 5   | PE       | 1         | R/W | Parity Enable (enabled only in the asynchronous mode)  
|     |          |           |     | When this bit is set to 1, a parity bit is added to transmit data before transmission, and the parity bit is checked in reception. |
| 4   | PM       | 1         | R/W | Parity Mode  
|     |          |           |     | (enabled only when the PE bit is 1 in the asynchronous mode)  
|     |          |           |     | 0: Even parity used for transmission  
|     |          |           |     | 1: Odd parity used for transmission  
|     |          |           |     | When even parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an even number. During reception the data is checked to confirm that the number of 1 bits in the receive data plus the parity bit is an even number.  
|     |          |           |     | When odd parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an odd number. During reception the data is checked to confirm that the number of 1 bits in the receive data plus the parity bit is an odd number. Note that in the clock-synchronous mode, and in the asynchronous mode if parity bit addition and checking is disabled, the PM bit setting is invalid. |
| 3   | STOP     | 0         | R/W | Stop Bit Length (enabled only in the asynchronous mode)  
|     |          |           |     | Selects the stop bit length in transmission.  
|     |          |           |     | 0: 1 stop bit  
|     |          |           |     | 1: 2 stop bits  
|     |          |           |     | Only the first stop bit is checked during reception, regardless of the value of STOP. If the second stop bit is 0, it is treated as the start bit of the next transmit character. |
| 2   | MP       | 0         | R/W | Multiprocessor Mode  
|     |          |           |     | The multiprocessor communication function is enabled when this bit is set to 1. The PE and PM bit settings become invalid. |
| 1   | CKS1     | 0         | R/W | Clock Select 0 and 1  
|     |          |           |     | These bits select the clock source for the internal baud rate generator.  
|     |          |           |     | 00: φ clock (n = 0)  
|     |          |           |     | A set value of 0 is used for active (medium-speed/high-speed) mode. |
Asynchronous Serial Data Reception

**BRR3**  Bit Rate Register 3  Address: H'FF99

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>bit7</td>
<td>0</td>
<td>R/W</td>
<td>BRR3 is an 8-bit readable/writable register that selects the bit rate. The initial value is H'FF. The bit rate is determined by the setting of bits CKS1 and CKS0 in SMR3 in the asynchronous mode and combination with the N setting of BRR3. See the hardware manual for details.</td>
</tr>
<tr>
<td>6</td>
<td>bit6</td>
<td>0</td>
<td>R/W</td>
<td>In this sample task BRR3 is set to 9 to obtain a bit rate of 31,250 bps.</td>
</tr>
<tr>
<td>5</td>
<td>bit5</td>
<td>0</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>bit4</td>
<td>0</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>bit3</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>bit2</td>
<td>0</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>bit1</td>
<td>0</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>bit0</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

**SCR3**  Serial Control Register 3  Address: H'FF9A

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>TE</td>
<td>0</td>
<td>R/W</td>
<td>Transmit Enable Transmission is enabled when this bit is set to 1. When TE is 0, the TDRE bit in SSR3 is fixed at 1. When transmit data is written to TDR3 while TE is 1, the TDRE bit in SSR3 is cleared to 0 and serial data transmission starts. Be sure to carry out SMR3 settings and set the SPC31 or SPC32 bit in SPCR to determine the transmission format before setting the TE bit to 1.</td>
</tr>
<tr>
<td>4</td>
<td>RE</td>
<td>1</td>
<td>R/W</td>
<td>Receive Enable Reception is enabled when this bit is set to 1. In this state serial data reception is started when serial clock input is detected in the asynchronous mode. Be sure to carry out SMR3 settings to decide the reception format before setting the RE bit to 1. Note that the RDRF, FER, PER, and OER flags in SSR3 are not affected when the RE bit is cleared to 0, and retain their previous state.</td>
</tr>
<tr>
<td>1</td>
<td>CKE1</td>
<td>0</td>
<td>R/W</td>
<td>Clock Enable 0 and 1</td>
</tr>
<tr>
<td>0</td>
<td>CKE0</td>
<td>0</td>
<td>R/W</td>
<td>Selects the clock source. Asynchronous mode 00: Internal baud rate generator (SCK31 or SCK32 pin functions as an I/O port)</td>
</tr>
</tbody>
</table>
### SSR3
**Serial Status Register 3**

**Address:** H'FF9C

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 6   | RDRF     | 0         | R/(W) | Receive Data Register Full  
Indicates whether or not receive data is stored in RDR3.  
[Setting condition]  
• When reception ends normally and receive data is transferred from RSR3 to RDR3  
[Clearing conditions]  
• When 0 is written to RDRF after it was read as 1  
• When data is read from RDR3 |
| 5   | OER      | 0         | R/(W) | Overrun Error  
[Setting condition]  
• When an overrun error occurs during reception  
[Clearing condition]  
• When 0 is written to OER after it was read as 1  
When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1. |
| 4   | FER      | 0         | R/(W) | Framing Error  
[Setting condition]  
• When a framing error occurs during reception  
[Clearing condition]  
• When 0 is written to FER after it was read as 1  
When the RE bit in SCR3 is cleared to 0, the FER bit is not affected and retains its previous state. Note that, in 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR3 but the RDRF bit is not set. Reception cannot be continued with the FER bit set to 1. |
| 3   | PER      | 0         | R/(W) | Parity Error  
[Setting condition]  
• When a parity error is generated during reception  
[Clearing condition]  
• When 0 is written to PER after it was read as 1  
When the RE bit in SCR3 is cleared to 0, the PER bit is not affected and retains its previous state. Receive data in which a parity error has occurred is still transferred to RDR3, but the RDRF bit is not set. Reception cannot be continued with the PER bit set to 1. |

**Note:** * Only 0 can be written to clear the flag.
3. Flowchart

```
init_sci3

SCR3 = H'00
     Clear TE to 0 to disable transmission
     Clear RE to 0 to disable reception
     Select internal baud rate generator

SMR3 = H'30
     Set the asynchronous mode, enable parity bit,
     select odd parity for transmission and reception,
     internal baud rate generator as clock source

BRR3 = 9
     Set bit rate to 31,250 bps

1 bit duration elapsed?
   No
   Wait 1 bit duration in software
   Yes

Clear OER
Clear FER
Clear PER
Clear RDRF

RE = 1
     Enable reception

return
```
4.4.3  rcv_scl3() Function

1. Module Specifications
   • Receives serial data in the asynchronous mode

Table 6  Module Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Type</th>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arguments</td>
<td>unsigned char</td>
<td>r_ptr</td>
<td>Pointer to buffer for storing receive data</td>
</tr>
<tr>
<td></td>
<td>unsigned char</td>
<td>num</td>
<td>Number of bytes of receive data</td>
</tr>
<tr>
<td>Return value</td>
<td>unsigned char</td>
<td>err</td>
<td>Indicates whether or not an error has occurred</td>
</tr>
</tbody>
</table>

2. Internal Registers Used
   The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

   • RDR3  Receive Data Register 3  Address: H'FF9D

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Bit 7</td>
<td>Undefined</td>
<td>R</td>
<td>RDR3 is an 8-bit register that stores receive data. When one</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>frame of data has been received, it is transferred from RSR3</td>
</tr>
<tr>
<td>6</td>
<td>Bit 6</td>
<td>Undefined</td>
<td>R</td>
<td>to this register, enabling RSR3 to receive the next frame of</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>data. RSR3 and RDR3 have a double-buffered structure, so</td>
</tr>
<tr>
<td>5</td>
<td>Bit 5</td>
<td>Undefined</td>
<td>R</td>
<td>continuous reception is possible. Read RDR3 only once, after</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>confirming that the RDRF bit in SSR3 is set to 1. RDR3 cannot</td>
</tr>
<tr>
<td>4</td>
<td>Bit 4</td>
<td>Undefined</td>
<td>R</td>
<td>be written to by the CPU. The initial value of RDR3 is H'00.</td>
</tr>
<tr>
<td>3</td>
<td>Bit 3</td>
<td>Undefined</td>
<td>R</td>
<td>RDR3 is initialized to H'00 at a reset, in the standby mode,</td>
</tr>
<tr>
<td>2</td>
<td>Bit 2</td>
<td>Undefined</td>
<td>R</td>
<td>watch mode, or module standby mode.</td>
</tr>
<tr>
<td>1</td>
<td>Bit 1</td>
<td>Undefined</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Bit 0</td>
<td>Undefined</td>
<td>R</td>
<td></td>
</tr>
</tbody>
</table>
### SSR3 Serial Status Register 3
**Address:** H'FF9C

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 6   | RDRF     | Undefined | R/(W) | Receive Data Register Full  
Indicates whether or not receive data is stored in RDR3.  
**[Setting condition]**  
- When reception ends normally and receive data is transferred from RSR3 to RDR3  
**[Clearing conditions]**  
- When 0 is written to RDRF after it was read as 1  
- When data is read from RDR3  
If an error is detected during reception, or if the RE bit in SCR3 has been cleared to 0, RDR3 and the RDRF bit are not affected and retain their previous state. Note that if data reception is completed while bit RDRF is still set to 1, an overrun error (OER) will occur and the receive data will be lost. |
| 5   | OER      | Undefined | R/(W) | Overrun Error  
**[Setting condition]**  
- When an overrun error occurs during reception  
**[Clearing condition]**  
- When 0 is written to OER after it was read as 1  
When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1. |
| 4   | FER      | Undefined | R/(W) | Framing Error  
**[Setting condition]**  
- When a framing error occurs during reception  
**[Clearing condition]**  
- When 0 is written to FER after it was read as 1  
When the RE bit in SCR3 is cleared to 0, the FER bit is not affected and retains its previous state. Note that, in 2-stop-bit mode, only the first stop bit is checked for a value of 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR3 but the RDRF bit is not set. Reception cannot be continued with the FER bit set to 1. |
| 3   | PER      | Undefined | R/(W) | Parity Error  
**[Setting condition]**  
- When a parity error is generated during reception  
**[Clearing condition]**  
- When 0 is written to PER after it was read as 1  
When the RE bit in SCR3 is cleared to 0, the PER bit is not affected and retains its previous state. Receive data in which a parity error has occurred is still transferred to RDR3, but the RDRF bit is not set. Reception cannot be continued with the PER bit set to 1. |

**Note:** * Only 0 can be written to clear the flag.
3. Flowchart

```
recv_sci3
i = 0
err = 0
OER == 1?
Yes
Set err to 1
Clear OER to 0
No
FER == 1?
Yes
Set err to 1
Clear FER to 0
No
PER == 1?
Yes
Set err to 1
Clear PER to 0
No
Error?
Yes
RDRF == 1?
Yes
Error?
Yes
No
Read data from RDR3
No
i++
i < byte count?
Yes
No
return(err)
```

Variable showing whether or not an error has occurred
err = 0: No error
err = 1: Error
### 4.4.4 stop_sci3() Function

1. **Module Specifications**
   - Ends the asynchronous mode

<table>
<thead>
<tr>
<th>Table 7 Module Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Item</strong></td>
</tr>
<tr>
<td>Arguments</td>
</tr>
</tbody>
</table>

2. **Internal Registers Used**
   The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- **SCR3** Serial Control Register 3 Address: H'FF9A

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>RE</td>
<td>0</td>
<td>R/W</td>
<td>Receive Enable</td>
</tr>
</tbody>
</table>

Reception is enabled when this bit is set to 1. Serial data reception is started when a start bit is detected in the asynchronous mode. Be sure to carry out SMR3 settings to determine the reception format before setting the RE bit to 1. Note that the RDRF, FER, PER, and OER flags in SSR3 are not affected when the RE bit is cleared to 0, and retain their previous state.

3. **Flowchart**

- stop_sci3
- Clear RE to 0
- Disable reception
- return

### 4.5 Link Address Specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVECT</td>
<td>H'0000</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
</tbody>
</table>
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.18.05</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.

2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.

Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).

4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.

7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.

Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.