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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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Introduction
The timer W input capture function is used to trim the on-chip oscillator of the H8/36912.

Target Device
H8/36912

Contents
1. Specifications ............................................................................................................. 2
2. Functions Used............................................................................................................ 3
3. Principles of Operation.............................................................................................. 6
4. Description of Software............................................................................................ 8
5. Flowcharts ................................................................................................................. 14
1. Specifications

The timer W input capture function is used to trim the on-chip oscillator of the H8/36912. An illustration of procedure for trimming the on-chip oscillator used in this sample task is shown in figure 1.

Data to be set in the RC trimming data register (RCTRMDR) is calculated based on the external reference clock input to timer W input capture A (the FTIOA pin).

In this sample task the frequency of the reference clock input to the FTIOA pin is 100 kHz and the on-chip oscillation frequency is trimmed to 9 MHz. Furthermore, the clock generated by the on-chip oscillator is output from pin PC1 for operation checking. Note that the on-chip oscillation frequency is trimmed to within an error range of 5%.

---

**Figure 1  On-Chip Oscillator Trimming**
2. Functions Used

2.1 Functions

In this sample task, trimming of the on-chip oscillator is performed. A block diagram of the timer W input capture and trimming operation is shown in figure 2. A description of the functions used in the sample task is provided below.

- On-chip oscillator functions
  - Clock control/status register (CKCSR)
    Selects the port C function, controls switching the system clocks, and indicates the system clock state.
  - RC trimming data protect register (RCTRMDPR)
    Controls RCTRMDPR itself and writing to RCTRMDR. Use the MOV instruction to rewrite this register. Bit manipulation instructions cannot be used to change the settings.
  - RC trimming data register (RCTRMDR)
    Stores the trimming data for the on-chip oscillator frequency.

- Timer W functions
  - Timer mode register W (TMRW)
    Selects the general register functions and the timer output mode.
  - Timer control register W (TCRW)
    Selects the TCNT counter clock source, selects a clearing condition, and specifies the timer output levels.
  - Timer status register W (TSRW)
    Shows the status of interrupt requests.
  - Timer I/O control register 0 (TIOR0)
    Selects the functions of GRA and GRB, and specifies the functions of the FTIOA and FTIOB pins.
  - Timer counter (TCNT)
    A 16-bit readable/writable up-counter. TCNT must always be read or written to in 16-bit units; 8-bit access is not allowed. The initial value of TCNT is H'0000.
  - General registers A and C (GRA and CRC)
    Each general register is a 16-bit readable/writable register that can function as either an output compare register or an input capture register. Also, GRC can be used as a buffer register for GRA.
System clock \( (\phi = \phi_{RC}) \)

Input pulse

FTIOA

Prescaler S (PSS)

Select TCNT input clock

Timer counter (TCNT)

Set buffer operation

General register A (GRA)

Set input capture

Timer status register W (TSRW)

General register C (GRC)

Timer interrupt enable register W (TIERW)

Calculate data to be written to RCTRMDR to obtain desired frequency based on input pulse

Note: See section 3, Principles of Operation, for details of the calculation method.

Control writing to RCTRMDR

Control on-chip oscillation frequency

RC trimming data protect register (RCTRMDPR)

On-chip oscillator

Figure 2 Block Diagram of Timer W Input Capture and Trimming
2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, trimming of the on-chip oscillator is performed.

Table 1 Assignment of Functions

<table>
<thead>
<tr>
<th>Elements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CKCSR</td>
<td>Controls on-chip oscillator clock output</td>
</tr>
<tr>
<td>TMRW</td>
<td>Controls the timer counter, sets GRC as buffer register for GRA</td>
</tr>
<tr>
<td>TCRW</td>
<td>Sets $\phi$ as the TCNT counter clock source</td>
</tr>
<tr>
<td>TIERW</td>
<td>Enables input capture A interrupts</td>
</tr>
<tr>
<td>TSRW</td>
<td>Input capture A interrupt request flag</td>
</tr>
<tr>
<td>TIOR0</td>
<td>Specifies that input capture to GRA is performed at rising edge of FTIOA pin</td>
</tr>
<tr>
<td>TIOR1</td>
<td>Sets GRC to the GRA buffer function</td>
</tr>
<tr>
<td>TCNT</td>
<td>16-bit counter that counts rising edges of $\phi$</td>
</tr>
<tr>
<td>GRA</td>
<td>TCNT value is transferred at GRA input capture</td>
</tr>
<tr>
<td>GRC</td>
<td>GRA value is sent to buffer register GRC at GRA input capture</td>
</tr>
<tr>
<td>TCSRWD</td>
<td>Stops the watchdog timer operation</td>
</tr>
</tbody>
</table>
3. Principles of Operation

Trimming of the on-chip oscillator is performed by using the timer W input capture function to input an external reference pulse. Using the hardware and software processing shown in figures 3 and 4 the on-chip oscillator is trimmed.

The equation shown below can be used to obtain the oscillation frequency of the on-chip oscillator. Since the input capture input is sampled at $\phi_{RC}$ the calculated value has a sampling error of $\pm 1$ clock ($\phi_{RC}$).

$$\phi_{RC} = \frac{(M + \alpha) - M}{t_A} \quad [\text{MHz}]$$

$\phi_{RC}$: Oscillation frequency of on-chip oscillator [MHz]
$t_A$: Reference clock frequency [µs]
$M$: Timer W counter value (M < TCNT)

**Figure 3 Principles of Operation 1**
Set timer W
GRA: Input capture
GRC: GRA buffer

Set RCTRMDR to H'00

Input reference pulse to FTIOA pin

Capture 1

Capture 2

Calculate frequency

Within desired frequency range?

No

Yes

End

Start

Note: * Compare the measured frequency to the desired frequency to determine if it is higher or lower, then decide the value of RCTRMDR one bit at a time, starting from the MSB. This sample task uses the setting method shown below. However, trimming is not possible if $\phi_{RC}$ is higher than the desired frequency when the sign bit is set to 1, because the frequency is already at its minimum value (H'80). Also, trimming is not possible if the frequency is not within the desired range after setting all the valid bits to 1.

**Figure 4  Principles of Operation 2**
4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>Stops the watchdog timer operation, controls the RC trimming data register, outputs the on-chip oscillator clock, sets input capture, controls TCNT, and controls interrupts</td>
</tr>
<tr>
<td>twint</td>
<td>Handles input capture interrupts, clears IMFA, disable input capture interrupts, and increments cnt</td>
</tr>
<tr>
<td>trimming</td>
<td>Calculates the measured frequency, rewrites RCTRMDR, and increments tr_cnt</td>
</tr>
<tr>
<td>labs</td>
<td>Standard function included in stdlib.h. Calculates absolute values using long-type data as arguments, and returns the result as long-type data</td>
</tr>
</tbody>
</table>

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- CKCSR Clock control/status register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PMRC1</td>
<td>1</td>
<td>R/W</td>
<td>Port C function select bits 1 and 0</td>
</tr>
<tr>
<td>6</td>
<td>PMRC0</td>
<td>0</td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PMRC1</th>
<th>PMRC0</th>
<th>PC1</th>
<th>PC0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>CLKOUT</td>
<td>I/O</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>I/O</td>
<td>OSC1 (external clock input)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>OSC2</td>
<td>OSC1</td>
</tr>
</tbody>
</table>
### RCTRMDPR
RC trimming data protect register
Address: H'F736

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 WRI</td>
<td>Write inhibit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 PRWE</td>
<td>Protect information write enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 LOCKDW</td>
<td>Trimming data register lock down</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 TRMDRWE</td>
<td>Trimming data register write enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### RCTRMDR
RC trimming data register
Address: H'F737

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 TRMD7</td>
<td>Trimming data</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 TRMD6</td>
<td>In the flash memory version, trimming data is loaded from flash memory to this register immediately after a reset. These bits are always read as undefined values.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 TRMD5</td>
<td>The frequency changes as follows, using TRMD7 as the sign bit:</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Note:** * In the flash memory version, these bits are initialized using trimming data values from flash memory.
### TMRW  Timer mode register W  
Address: H'FF80

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | CTS      | 1         | R/W | Counter start  
TCNT counter operation is halted when this bit is 0, and the counter operates when this bit is 1. |
| 4   | BUFEA    | 1         | R/W | Buffer operation A  
Selects the GRC function.  
0: GRC operates as an input capture/output compare register  
1: GRC operates as the buffer register for GRA |

### TCRW  Timer control register W  
Address: H'FF81

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | CCLR     | 0         | R/W | Counter clear  
The TCNT value is cleared by compare match A when this bit is 1.  
When this bit is 0, TCNT operates as a free-running counter. |
| 6   | CKS2     | 0         | R/W | Clock select 2 to 0 |
| 5   | CKS1     | 0         | R/W | Selects the clock input to TCNT. |
| 4   | CKS0     | 0         | R/W | 000: Internal clock: counts on φ  
001: Internal clock: counts on φ/2  
010: Internal clock: counts on φ/4  
011: Internal clock: counts on φ/8  
1XX: Counts on rising edges of external event (FTCI) |

Note:  X: Don’t care

### TIERW  Timer interrupt enable register W  
Address: H'FF82

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0   | IMIEA    | 1         | R/W | Input capture/compare match interrupt enable A  
When this bit is set to 1, IMIA interrupt requests using IMFA in TSRW are enabled. |

### TSRW  Timer status register W  
Address: H'FF83

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | OVF      | 0         | R/W | Timer overflow flag  
[Setting condition]  
• When TCNT overflows from H'FFFF to H'0000  
[Clearing condition]  
• When this bit is read as 1 and then 0 is written to it |
| 0   | IMFA     | 0         | R/W | Input capture/compare match flag A  
[Setting condition]  
• When the TCNT value is transferred to GRA by an input capture signal when GRA is functioning as an input capture register  
[Clearing condition]  
• When this bit is read as 1 and then 0 is written to it |
### H8/36912, H8/36902 Groups
On-Chip Oscillator Trimming

- **TIOR0** Timer I/O control register 0 Address: H'FF84

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>IOA2</td>
<td>1</td>
<td>R/W</td>
<td>I/O control A2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Selects the GRA function.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: GRA functions as an output compare register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: GRA functions as an input capture register</td>
</tr>
</tbody>
</table>

- **TIOR1** Timer I/O control register 1 Address: H'FF85

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>IOC2</td>
<td>1</td>
<td>R/W</td>
<td>I/O control C2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Selects the GRC function.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Functions as an output compare register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Functions as an input capture register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If GRA buffer operation has been selected by BUFEA in TMRW, the same function as GRA should be selected.</td>
</tr>
</tbody>
</table>

- **TCNT** Timer counter Address: H'FF86

  Description: A 16-bit readable/writable up-counter. TCNT must always be read or written to in 16-bit units; 8-bit access is not allowed. The initial value of TCNT is H'0000.

  Set value: H'0000

- **GRA** General register A Address: H'FF88

  Description: A 16-bit readable/writable register to which TCNT values are transferred during input capture operation. GRA must always be read or written to in 16-bit units; 8-bit access is not allowed.

  Set value: —

  Note: —: Undefined
• GRC  General register C  Address: H'FF8C
  Description: A 16-bit readable/writable register. When GRC is set as the buffer of GRA, during input capture operation TCNT values are transferred to GRA and then from GRA to the buffer register GRC. TCNT values are transferred at the rising edge of the FTIOA. GRC must always be read or written to in 16-bit units; 8-bit access is not allowed.
  Set value: —
  Note: —: Undefined

• TCSRWD  Timer control/status register WD  Address: H'FFC0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 5   | B4WI     | 0             | R/W Bit 4 write inhibit  
  Bit 4 in this register can be written to only when 0 is written to this bit. This bit is always read as 1. |
| 4   | TCSRWE   | 1             | R/W Timer control/status register W write enable  
  Writing to bits 2 and 0 in this register is enabled when this bit is set to 1. When writing 0 to this bit, the value written to bit 5 must be 0 as well. |
| 3   | B2WI     | 0             | R/W Bit 2 write inhibit  
  Bit 2 in this register can be written to only when 0 is written to this bit. This bit is always read as 1. |
| 2   | WDON     | 0             | R/W Watchdog timer on  
  TCWD (timer counter WD) starts counting up when this bit is set to 1 and halts when the this bit is cleared to 0. The watchdog timer is enabled in the initial state. Clear this bit to 0 if the watchdog timer will not be used.  
  [Clearing conditions]  
  • Reset  
  • When 0 is written to the B2WI bit and 0 is written to the WDON bit while the TCSRWE bit is set to 1  
  [Setting condition]  
  • When 0 is written to the B2WI bit and 1 is written to the WDON bit while the TCSRWE bit is set to 1 |
4.4 Constants Used

The constants used in this sample task are shown in table 3.

<table>
<thead>
<tr>
<th>Label</th>
<th>Constant Value</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>ERROR</td>
<td>7</td>
<td>Error code</td>
<td>main trimming</td>
</tr>
<tr>
<td>HZ</td>
<td>9</td>
<td>Desired frequency [MHz]</td>
<td>trimming</td>
</tr>
<tr>
<td>IN_PERIOD</td>
<td>10</td>
<td>Pulse cycle input to FTIOA pin [10 µs]</td>
<td></td>
</tr>
<tr>
<td>MAX_FRE</td>
<td>105</td>
<td>105% of desired frequency (used to determine if frequency is in desired frequency range)</td>
<td></td>
</tr>
<tr>
<td>MIN_FRE</td>
<td>95</td>
<td>95% of desired frequency (used to determine if frequency is in desired frequency range)</td>
<td></td>
</tr>
<tr>
<td>OK</td>
<td>0</td>
<td>OK code</td>
<td></td>
</tr>
</tbody>
</table>

4.5 RAM Usage

The RAM usage in this sample task is shown in table 4.

<table>
<thead>
<tr>
<th>Constant</th>
<th>Description</th>
<th>Amount of Memory Used</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>cnt</td>
<td>Number of input captures</td>
<td>1 byte</td>
<td>main</td>
</tr>
<tr>
<td>tr_cnt</td>
<td>Number of times trimming data is rewritten</td>
<td>1 byte</td>
<td>main trimming</td>
</tr>
</tbody>
</table>
5. Flowcharts

5.1 main

```
main

set_ccr(H'80)  Disable interrupts

TCSRWD = H'9E
TCSRWD = H'92
TCSRWD = H'8A

tr_cnt = 0
tmp = 0

RCTRMDPR = H'4F
RCTRMDPR = H'5F
RCTRMDR = H'00
CKCSR = H'80

Enable writing to RCTRMDR
Initialize RCTRMDR
Clock output

TMRW = H'58
TCRW = H'00
tmp = TSRW
TSRW & = H'70
TIOR0 = H'8C
TIOR1 = H'8C

CTS = 1
Start timer counter

set_imask_ccr = 0
Enable interrupts

tmp = ERROR?
Yes

No

cnt = 0

IMIEA = 1

No

cnt = 2 ?
Yes

tmp = trimming()

No

tmp = 0 ?
Yes

set_imask_ccr = 1
Disable interrupts

Error handling
Note: In this sample task this is an infinite loop.
The user should provide appropriate error handling here.

Enable input capture

Input capture finished?

Enable interrupts

Stop WDT

Count internal clock φ
Clear flag
Use GRC as GRA buffer
Use GRA and GRC for input capture
```

Stop timer counter
5.2 twint

twint

tmp = TSRW
TSRW & H'7E

cnt > 0 ?

Yes

Clear flag

IMIEA = 0

Disable input capture interrupts

No

IMIEA = 0

Increment number of input capture interrupts

cnt++

cnt > 0 ?

end
5.3 trimming

```
5.3 trimming

tmp = H'80

fcnt = GRA - GRC

fcnt = (short)(labs((long)fcnt))

hz = fcnt * 100 / IN_PERIOD

hz > (HZ*MIN_FRE) ...
and ...
hz < (HZ*MAX_FRE)?

Yes

hz > (HZ*MAX_FRE)?

No

tr_cnt = 0 ?

Yes

tr_cnt = 1 ?

Yes

No

No

No

Yes

RCTRMDR = tmp

tmp >>= tr_cnt
RCTRMDR |= tmp
tmp <<= 1
RCTRMDR ^= tmp

return(0)

No

Yes

tr_cnt++

return(tr_cnt)
```

Input capture

Calculate current $\phi_{RC}$

Is $hz$ within the desired frequency range?

Yes

No

return(0)

Yes

No

No

return(ERROR)
5.4 Link Address Specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'0000</td>
</tr>
<tr>
<td>CV2</td>
<td>H'002A</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
<tr>
<td>B</td>
<td>H'FD80</td>
</tr>
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</table>
# Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Dec.20.04</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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