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April 1st, 2010
Renesas Electronics Corporation

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Introduction
An internal low-voltage detection circuit is used, and depending on the voltage level, transitions to standby mode or to the reset state are made.

Target Device
H8/3687G

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1. Specifications.......................................................................................................................... 2
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1. Specifications

1. An internal low-voltage detection circuit is used, and the operating state is changed.
2. While in active mode, when the voltage falls to 3.7 V or lower, a transition to standby mode is made.
3. If, while in standby mode, the voltage rises to 4.0 V or higher, the system is returned to active mode.
4. When the voltage falls to 2.3 V or below, an internal reset signal is generated.
5. In order to confirm the operating/reset state, connect an LED to pin P74. In the operating state, the LED is turned on (P74 = 0), and in the reset state the LED is turned off (P74 = 1).
6. If the IRQ1 switch is turned on, the low-voltage detection circuit is canceled.
7. A connection example for this task is shown in figure 1.1.

![Connection example for this task](image-url)

**Figure 1.1** Connection example for this task
2. Description of Functions

1. In this sample task, the optional internal low-voltage detection circuit is used to control the operating state at low voltages. A block diagram of the low-voltage detection circuit is shown in figure 2.1. Below, the block diagram of the low-voltage detection circuit is described.

- System clock (φ) is a 16 MHz clock which serves as the reference clock for operation of the CPU and peripheral functions.
- Prescaler S (PSS) is functions as a 13-bit counter with φ as an input, counting up one each cycle.
- Low-voltage detection control register (LVDCR) is controls the low-voltage detection circuit. In this sample task, the low-voltage detection circuit is used to generate an IRQ0 interrupt when the voltage rises or falls, and sets the reset detection voltage to 2.3 V.
- Low-voltage detection status register (LVDSR) is flags indicating whether the power supply voltage has risen or fallen from a constant voltage.

![Block diagram of the low-voltage detection circuit](image)

Figure 2.1   Block diagram of the low-voltage detection circuit

2. Function allocations in this sample task are shown in table 2.1. Functions are allocated as shown in table 2.1, and upon low voltage detection there is a transition to standby mode.

Table 2.1   Function allocations

<table>
<thead>
<tr>
<th>Function</th>
<th>Function allocation</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSS</td>
<td>A 13-bit counter with the system clock used as an input signal</td>
</tr>
<tr>
<td>LVDCR</td>
<td>Controls operation/cancellation of the low-voltage detection circuit</td>
</tr>
<tr>
<td>LVDSR</td>
<td>Flags indicating whether the power supply voltage has risen or fallen from a certain constant voltage</td>
</tr>
<tr>
<td>PDR7</td>
<td>In order to confirm the operating mode, an LED connected to pin P74 is lit</td>
</tr>
<tr>
<td>PCR7</td>
<td>Pin P74 is set to an output pin</td>
</tr>
<tr>
<td>SYSCR1</td>
<td>Controls low-power consumption modes</td>
</tr>
<tr>
<td>SYSCR2</td>
<td>Controls low-power consumption modes</td>
</tr>
<tr>
<td>IRQ1</td>
<td>Low-voltage detection circuit operation/cancellation switch</td>
</tr>
</tbody>
</table>
3. Description of Operation

1. Figure 3.1 shows the procedure for setting and canceling LVDI, and transitions to standby mode triggered by low-voltage detection interrupts.

![Diagram of Active mode and Standby mode transitions](image-url)

**Figure 3.1 Description of operation (1)**
2. Figure 3.2 illustrates a transition to standby mode triggered by a low-voltage detection interrupt, and reset operation on low voltage detection.

![Figure 3.2 Description of operation (2)]
4. Description of Software

4.1 Description of modules

Modules in this sample task are listed in table 4.1.

Table 4.1 Description of modules

<table>
<thead>
<tr>
<th>Module name</th>
<th>Label name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Set low-voltage detection circuit, enable interrupts, control LED (P74), and judge switch connected to IRQ0</td>
</tr>
<tr>
<td>Low-voltage detection</td>
<td>irq0int</td>
<td>IRQ0 interrupt processing Clear LVD flag, set lpcnt to 0 or 1</td>
</tr>
<tr>
<td>interrupt</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switch on</td>
<td>irq1int</td>
<td>IRQ01 interrupt processing Set lpcnt to 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4.2 Description of arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers Used

Internal registers used in this sample task are indicated below.

- LVDCR  Low-voltage detection control register Address: 0xF730

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 7   | LVDE     | 1       | LVD enable
LVDE = 0: Low-voltage detection circuit is not used (standby state)
LVDE = 1: Low-voltage detection circuit is used |
| 3   | LVDSEL   | 0       | LVDR detection level selection
LVDSEL = 0: Sets reset detection voltage to 2.3 V
LVDSEL = 1: Sets reset detection voltage to 3.6 V |
| 2   | LVDRE    | 1       | LVDR enable
LVDRE = 0: Disables reset by LVDR
LVDRE = 1: Enables reset by LVDR |
| 1   | LVDDE    | 1       | LVDR enable
LVDDE = 0: Disables interrupt requests when voltage falls
LVDDE = 1: Enables interrupt requests when voltage falls |
| 0   | LVDUE    | 1       | LVDR enable
LVDUE = 0: Disables interrupt requests when voltage rises
LVDUE = 1: Enables interrupt requests when voltage rises |
### LVDSR Low-voltage detection status register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 1   | LVDDF    | 0       | LVD power supply voltage drop flag  
LVDDF = 0: Cleared to 0 state  
LVDDF = 1: Power supply voltage has fallen to 3.7 V or below |
| 0   | LVDFU    | 0       | LVD power supply voltage rise flag  
LVDFU = 0: Cleared to 0 state  
LVDFU = 1: While the LVDUE flag of LVDCR is set to 1, the power supply voltage has fallen to 3.7 V or below, and risen again to 4.0 V or above before falling to V reset (2.3 V) or below |

### PDR7 Port data register 7

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 4   | P74      | 0       | Port data register 7  
P74 = 0: Pin P74 output level Low  
P74 = 1: Pin P74 output level High |

### PMR1 Port mode register 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 5   | IRQ1     | 1       | Selects function of pin P15/IRQ1  
IRQ1 = 0: Sets pin P15/IRQ1 to P15 I/O pin function  
IRQ1 = 1: Sets pin P15/IRQ1 to IRQ1 input pin function |

### PCR7 Port control register 7

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 4   | PCR74    | 0       | Port control register 7  
PCR74 = 0: Sets pin P74 to P74 input pin function  
PCR74 = 1: Sets pin P74 to P74 output pin function |

### SYSCR1 System control register 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 7   | SSBY     | 1       | Software standby  
DSYNO = 0, SSBY = 1:  
After executing SLEEP instruction in active mode, makes transition to standby mode |
| 6   | STS2     | STS2 = 1| Standby timer select 2 to 0 |
| 5   | STS1     | STS1 = 0| When STS2 = 1, STS1 = 0 and STS0 = 0, the number of wait states is set to 131,072 states |
| 4   | STS0     | STS0 = 0| |

### SYSCR2 System control register 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 5   | DTON     | 0       | Direct transfer on flag  
DSYNO = 0, SSBY = 1:  
After executing SLEEP instruction in active mode, makes transition to standby mode |
| 4   | MA2      | MA2 = 0 | Active mode clock select 2 to 0 |
| 3   | MA1      | MA1 = x | MA2 = 0, MA1 = x, MA0 = x: |
| 2   | MA0      | MA0 = x | Sets the operating clock in active mode/sleep mode to φosc  
(x: don't care) |
Transition to Standby Mode upon Detecting Low Voltage

- **IEGR1 Interrupt edge select register 1**
  Address: 0xFFF2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>IEG1</td>
<td>1</td>
<td>IRQ1 edge select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IEG1 = 0: Selects falling edge as IRQ1 pin input detection edge</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IEG1 = 1: Selects rising edge as IRQ1 pin input detection edge</td>
</tr>
</tbody>
</table>

- **IENR1 Interrupt enable register 1**
  Address: 0xFFF4

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IEN1</td>
<td>1</td>
<td>IRQ1 interrupt request enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IEN1 = 0: Disables interrupt requests at pin IRQ1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IEN1 = 1: Enables interrupt requests at pin IRQ1</td>
</tr>
</tbody>
</table>

- **IRR1 Interrupt flag register 1**
  Address: 0xFFF6

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IRR1</td>
<td>0</td>
<td>IRQ1 interrupt request flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IRR1 = 0: IRQ1 pin interrupt not requested</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IRR1 = 1: IRQ1 pin interrupt requested</td>
</tr>
<tr>
<td>0</td>
<td>IRR0</td>
<td>0</td>
<td>IRQ0 interrupt request flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IRR0 = 0: IRQ0 pin interrupt not requested</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IRR0 = 1: IRQ0 pin interrupt requested</td>
</tr>
</tbody>
</table>

### 4.4 Description of RAM Used

The RAM used in this sample task is described in table 4.2.

<table>
<thead>
<tr>
<th>Label name</th>
<th>Function</th>
<th>Size</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpcnt</td>
<td>Flag to discriminate low-voltage detection states</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>lpcnt = 0: Returned to normal mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>lpcnt = 1: Low power voltage, module standby</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>lpcnt = 2: IRQ1 interrupt, low-voltage detection circuit disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 byte</td>
<td>Main routine</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low-voltage detection interrupt</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Switch on</td>
<td></td>
</tr>
</tbody>
</table>
5. Flowcharts

1. Main routine

```
main*

I = 1
Disable interrupts.

IRRI0 = 0
Clear IRQ0 interrupt request flag.

IEG1 = 1
Set IRQT input pin detection edge to rising edge.

IRQT = 1
Set P15/IRQT pin to IRQT input pin function.

IEN1 = 1
Enable interrupt requests at IRQT pin.

IRRI1 = 0
Clear IRQ1 interrupt request flag.

LVDE = 1
Use low-voltage detection circuit.

tmp = LVDSR
LVDSR = 0xFC
Clear LVD flag.

LVDCR = 0xF7
Reset detection voltage = 2.3 V.
Enable reset by LVDR.
Enable voltage fall/rise interrupt requests.

PCR74 = 1
Set P74 to output pin function.

P74 = 0
Output 0 from P74.

ipcnt = 0
Clear switch judgment flag.

I = 0
Enable interrupts.

Ipcnt < 2

LVDCR = 0xF0
LVDE = 0
Cancel low-voltage detection circuit setting.

SYSCR1 = 0xC0
SYSCR2 = 0x0C
Set transition to standby mode.

sleep()
Transition to standby mode.

Ipcnt == 1

SYS

No

Yes

No

Yes

No

Yes

No

Yes

Note: * The stack pointer is set using INIT.SRC (assembly language).```
2. Low-voltage Detection Interrupts

![Flowchart for Low-voltage Detection Interrupts]

3. Switch-on

![Flowchart for Switch-on]
6. Program Listing

/routes------------------------------------------
/*
 * H8/300HN Series -H8/3687G-
 * Application Note
 * 'Reset by lowvoltage'
 */
/*
: Low-voltage detection circuit
*/
/*
External Clock : 16MHz
*/
/* Internal Clock : 16MHz
*/
/* Sub Clock : 32.768kHz
*/
/routes------------------------------------------

#include <machine.h>

/routes------------------------------------------
/* Symbol Definition */
/routes------------------------------------------

struct BIT {
    unsigned char b7:1; /* bit7 */
    unsigned char b6:1; /* bit6 */
    unsigned char b5:1; /* bit5 */
    unsigned char b4:1; /* bit4 */
    unsigned char b3:1; /* bit3 */
    unsigned char b2:1; /* bit2 */
    unsigned char b1:1; /* bit1 */
    unsigned char b0:1; /* bit0 */
};

#define LVDCR *(volatile unsigned char *)0xF730 /* Low-voltage-detection control register */
#define LVDCR_BIT *(struct BIT *)0xF730 /* Low-voltage-detection control register */
#define LVDE LVDCR_BIT.b7 /* LVD Enable */
#define LVDSEL LVDCR_BIT.b3 /* LVDI Detection Level Select */
#define LVDE LVDCR_BIT.b2 /* LVDR Enable */
#define PDR7_BIT *(struct BIT *)0xFFDA /* Port Data Register 7 */
#define P74 PDR7_BIT.b4 /* Port Data Register 7 bit4 */
#define PMR1_BIT *(struct BIT *)0xFFEO /* Port mode register 1 */
#define IRQ1 PMR1_BIT.b5 /* Port mode register 1 */
#define PCR7_BIT *(struct BIT *)0xFFEA /* Port Control Register 7 */
#define PCR74 PCR7_BIT.b4 /* Port Control Register 7 bit4 */
#define IEGR1_BIT *(struct BIT *)0xFFFF2 /* Interrupt Edge Select Register 1 */
#define IEQ1 IEGR1_BIT.b1 /* Interrupt Edge Select */
#define IENR1_BIT *(struct BIT *)0xFFFF4 /* Interrupt Enable Register 1 */
#define IEN1 IENR1_BIT.b1 /* Interrupt Enable */
#define IRR1_BIT *(struct BIT *)0xFFFF6 /* Interrupt Request Register 1 */
#define IRR1 IRR1_BIT.b1 /* Interrupt Request */

#pragma interrupt (irq1int)
extern void INIT ( void ); /* SP Set */
void main ( void );
void irq1int ( void );

extern void INIT ( void ); /* SP Set */
void main ( void );
void irq1int ( void );

void main ( void )
{
  unsigned short i;
  set_imask_ccr(1); /* Interrupt Disable */
  IEG1 = 1; /* IRQ1 pin input is Rising edge */
  IRQ1 = 1; /* Select IRQ1 pin */
  IEN1 = 1; /* IRQ1 Interrupt Enable */
  IRRI1 = 0; /* IRQ1 Flag Clear */
  LVDE = 1; /* LVD Enable */
  for(i=0; i<800; i++); /* 50us Wait */
  LVDCR = 0xFC; /* LVD = 3.6V LVD Reset Enable */
  PCR74 = 1; /* P74 Output Pin */
  P74 = 0; /* P74 is Low */
  swonf = 0; /* Initialize swonf */
  set_imask_ccr(0); /* Interrupt Enable */
  while(swonf == 0);

  LVDCR = 0xF0; /* clearing LVDRE, LVDE, LVDEUE to 0 */
  LVDE = 0; /* clear LVDE 0 */
  while(1);
}
void irq1int ( void )
{
    IRRI1 = 0;    /* Clear IRRI1 */
    swonf = 1;    /* Set swonf */
}

Link address specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>0x0000</td>
</tr>
<tr>
<td>CV2</td>
<td>0x001C</td>
</tr>
<tr>
<td>CV3</td>
<td>0x0100</td>
</tr>
<tr>
<td>P</td>
<td>0x0100</td>
</tr>
<tr>
<td>B</td>
<td>0xFB80</td>
</tr>
</tbody>
</table>
## Revision Record

<table>
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<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
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<tr>
<td>1.00</td>
<td>Sep.29.03</td>
<td>—</td>
<td>First edition issued</td>
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<tr>
<td>2.00</td>
<td>May.07.04</td>
<td>—</td>
<td>Clerical error correction</td>
</tr>
</tbody>
</table>
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