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April 1\(^{st}\), 2010  
Renesas Electronics Corporation

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H8/300H Tiny Series
Reset Operation upon Detecting Low Voltage

Introduction
An internal low-voltage detection circuit is used for setting/canceling internal reset operations at low voltages.

Target Device
H8/3687G

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1. Specifications

1. An internal low-voltage detection circuit is used, and when the voltage falls to 3.6 V or lower, an internal reset occurs.
2. While in low-voltage reset state, when the voltage rises to 3.6 V or higher, PSS starts counting upward, and the internal reset is cancelled after 131,072 states have passed.
3. In order to confirm the operating/reset state, connect an LED to pin P74. In the operating state, the LED is turned on (P74 = 0), and in the reset state the LED is turned off (P74 = 1).
4. If the IRQ switch is turned on, the low-voltage detection circuit is canceled.
5. A connection example for this task appears in figure 1.1.

![Connection example for this task](image-url)
2. Description of Functions

In this sample task, the optional internal low-voltage detection circuit is used to control the reset operation at low voltages. A block diagram of the low-voltage detection circuit appears in figure 2.1. Below, the block diagram of the low-voltage detection circuit is described.

- **System clock** ($\phi$) is a 16 MHz clock which serves as the reference clock for operation of the CPU and peripheral functions.
- **Prescaler S (PSS)** is functions as a 13-bit counter when $\phi$ is input, counting up one each cycle.
- **Low-voltage detection control register (LVDCR)** is controls the low-voltage detection circuit. In this sample task, the low-voltage detection circuit is used, and sets the reset detection voltage to 2.3 V.

![Figure 2.1 Block diagram of the low-voltage detection circuit](image-url)
3. Description of Operation

Figure 3.1 shows the procedure for setting and canceling low-voltage detection reset circuit, and reset operation on low voltage detection.

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**Figure 3.1 Description of operation**
4. Description of Software

4.1 Description of modules

Modules in this sample task are listed in table 4.1.

<table>
<thead>
<tr>
<th>Module name</th>
<th>Label name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Set low-voltage detection circuit, enable interrupts, control LED (P74), and judge switch connected to IRQ0</td>
</tr>
<tr>
<td>Switch on</td>
<td>irq1int</td>
<td>IRQ1 interrupt processing Set swonf to 1</td>
</tr>
</tbody>
</table>

4.2 Description of arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers Used

Internal registers used in this sample task are indicated below.

- LVDCR  Low-voltage detection control register Address: 0xF730

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>LVDE</td>
<td>1</td>
<td>LVD enable LVDE = 0: Low-voltage detection circuit is not used (standby state) LVDE = 1: Low-voltage detection circuit is used</td>
</tr>
<tr>
<td>3</td>
<td>LVDSEL</td>
<td>1</td>
<td>LVDR detection level selection LVDSEL = 0: Sets reset detection voltage to 2.3 V LVDSEL = 1: Sets reset detection voltage to 3.6 V</td>
</tr>
<tr>
<td>2</td>
<td>LVDRE</td>
<td>1</td>
<td>LVDR enable LVDRE = 0: disables reset by LVDR LVDRE = 1: Enables reset by LVDR</td>
</tr>
</tbody>
</table>

- PDR7  Port data register 7 Address: 0xFFDA

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>P74</td>
<td>0</td>
<td>Port data register 74 P74 = 0: Pin P74 output level Low P74 = 1: Pin P74 output level High</td>
</tr>
</tbody>
</table>

- PMR1  Port mode register 1 Address: 0xFFE0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>IRQ1</td>
<td>1</td>
<td>Selects function of pin P15/IRQ1/TMIB1 IRQ1 = 0: Sets pin P15/IRQ1/TMIB1 to P15 I/O pin function IRQ1 = 1: Sets pin P15/IRQ1/TMIB1 to /IRQ1/TMIB1 input pin</td>
</tr>
</tbody>
</table>
4.4 Description of RAM Used

The RAM used in this sample task is described in table 4.2.

Table 4.2 Description of RAM used

<table>
<thead>
<tr>
<th>Label name</th>
<th>Function</th>
<th>Size</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>swonf</td>
<td>Flag determining switch input on/off status</td>
<td>1 byte</td>
<td>Main routine</td>
</tr>
</tbody>
</table>
<pre><code>                                       |      | Switch on     |
</code></pre>

- **PCR7 Port control register 7**
  - **Address:** 0xFFEA
  - Bit 4: PCR74
    - Setting: 0
    - Function: Port control register 74
    - PCR74 = 0: Sets pin P74 to P74 input pin function
    - PCR74 = 1: Sets pin P74 to P74 output pin function

- **IEGR1 Interrupt edge select register 1**
  - **Address:** 0xFFF2
  - Bit 0: IEG1
    - Setting: 1
    - Function: IRQ1 edge select
    - IEG1 = 0: Selects falling edge as IRQ1 pin input detection edge
    - IEG1 = 1: Selects rising edge as IRQ1 pin input detection edge

- **IENR1 Interrupt enable register 1**
  - **Address:** 0xFFF4
  - Bit 1: IEN1
    - Setting: 1
    - Function: IRQ1 interrupt request enable
    - IEN1 = 0: Disables interrupt requests at pin IRQ1
    - IEN1 = 1: Enables interrupt requests at pin IRQ1

- **IRR1 Interrupt flag register 1**
  - **Address:** 0xFFF6
  - Bit 1: IRR1
    - Setting: 0
    - Function: IRQ1 interrupt request flag
    - IRR1 = 0: IRQ1 pin interrupt not requested
    - IRR1 = 1: IRQ1 pin interrupt requested
5. Flowcharts

1. Main routine

```
main*

I = 1
Disable interrupts.

IEG1 = 1
Set IRQ1 input pin detection
edge to rising edge.

IRQ1 = 1
Set P15/IRQ1 pin to IRQ1
input pin function.

IEN1 = 1
Enable interrupt requests
at IRQ1 pin.

IRR11 = 0
Clear IRQ1 interrupt request flag.

LVDE = 1
Use low-voltage detection circuit.

i = 0

i < 800

I = 0
Enable interrupts.

LVDCR = 0xF0
LVDE = 0
Cancel low-voltage detection circuit
setting.

Yes

swonf == 0

No

Note: * The stack pointer is set using INIT.SRC (assembly language).
```

2. Switch-on

```
irq1int

I = 0

irr11 = 0
Clear IRQ1 interrupt request flag.

swonf = 1
Set switch input judgment flag to on.

END
```

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6. Program Listing

/**************************************************************************
/*          */
/* H8/300HN Series -H8/3687G- */
/* Application Note */
/* 'Reset by lowvoltage' */
/* Function */
/* : Low-voltage detection circuit */
/* */
/* External Clock : 16MHz */
/* Internal Clock : 16MHz */
/* Sub Clock : 32.768kHz */
/* */
/**************************************************************************

#include    <machine.h>

/**************************************************************************
/* Symbol Definition */
/**************************************************************************

struct BIT {
    unsigned char   b7:1;  /* bit7 */
    unsigned char   b6:1;  /* bit6 */
    unsigned char   b5:1;  /* bit5 */
    unsigned char   b4:1;  /* bit4 */
    unsigned char   b3:1;  /* bit3 */
    unsigned char   b2:1;  /* bit2 */
    unsigned char   b1:1;  /* bit1 */
    unsigned char   b0:1;  /* bit0 */
};

#define     LVDCR  *(volatile unsigned char *)0xF730 /* Low-voltage-detection control register */
#define     LVDCR_BIT (*(struct BIT *)0xF730) /* Low-voltage-detection control register */
#define     LVDE   LVDCR_BIT.b7 /* LVD Enable */
#define     LVDESEL LVDCR_BIT.b3 /* LVDI Detection Level Select */
#define     LVDEOK  LVDCR_BIT.b2 /* LVDR Enable */
#define     PDR7_BIT (*(struct BIT *)0xFFDA) /* Port Data Register 7 */
#define     P74    PDR7_BIT.b4 /* Port Data Register 7 bit4 */
#define     PMR1_BIT (*(struct BIT *)0xFFE0) /* Port mode register 1 */
#define     PMR1_B5  PMR1_BIT.b5 /* P15/IRQ1 Pin Function Switch */
#define     PCR7_BIT (*(struct BIT *)0xFFF8) /* Port Control Register 7 */
#define     PCR74   PCR7_BIT.b4 /* Port Control Register 7 bit4 */
#define     IERG1_BIT (*(struct BIT *)0xFFF2) /* Interrupt Edge Select Register 1 */
#define     IERG1   IERG1_BIT.b1 /* IRQ1 Edge Select */
#define     IENR1_BIT (*(struct BIT *)0xFFF4) /* Interrupt Enable Register 1 */
#define     IENR1   IENR1_BIT.b1 /* IRQ1 Enable Register */
#define     IRR1_BIT (*(struct BIT *)0xFFF6) /* Interrupt Request Register 1 */
#define     IRR1    IRR1_BIT.b1 /* IRQ1 Interrupt Request Flag */

#pragma interrupt   (irq1int)
/** Function define */

extern void INIT ( void );

void main ( void );

void irqlnt ( void );

/** RAM define */

volatile unsigned char swonf;

/** Vector Address */

#pragma section     V1    /* VECTOR SECTION SET */
void (*const VEC_TBL1[])(void) = { /* 0x00 - 0x0f */
    INIT /* 00 Reset */
};
#pragma section     V2    /* VECTOR SECTION SET */
void (*const VEC_TBL2[])(void) = {
    irqlnt /* 1E IRQ1 Interrupt */
};

#pragma section     /* P */

/** Main Program */

void main ( void )
{
    unsigned short i;

    set_imask_ccr(1);    /* Interrupt Disable */
    
    IEG1 = 1;      /* IRQ1 pin input is Rising edge */
    IRQ1 = 1;      /* Select IRQ1 pin */
    IEN1 = 1;      /* IRQ1 Interrupt Enable */
    IRRI1 = 0;     /* IRQ1 Flag Clear */
    LVDE = 1;      /* LVD Enable */
    for(i=0; i<800; i++);
    LVDCR = 0xFC;  /* LVD = 3.6V LVD Reset Enable */
    PCR74 = 1;     /* P74 Output Pin */
    P74 = 0;      /* P74 is Low */
    swonf = 0;     /* Initialize swonf */
    set_imask_ccr(0);    /* Interrupt Enable */
    while(swonf == 0);
    LVDCR = 0xF0;  /* clearing LVDRE, LVDDE, LVDUE to 0 */
    LVDE = 0;     /* clear LVDE 0 */
    while(1);
}
/***/
/* IRQ1 Interrupt */
/***/

void irq1int ( void )
{
    IRRI1 = 0;    /* Clear IRRI1 */
    swonf = 1;    /* Set swonf */
}

Link address specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>0x0000</td>
</tr>
<tr>
<td>CV2</td>
<td>0x001E</td>
</tr>
<tr>
<td>P</td>
<td>0x0100</td>
</tr>
<tr>
<td>B</td>
<td>0xFB80</td>
</tr>
</tbody>
</table>
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
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<tr>
<td>1.00</td>
<td>Sep.29.03</td>
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<td>—</td>
<td>First edition issued</td>
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<td>2.00</td>
<td>May.07.04</td>
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<td>—</td>
<td>Clerical error correction</td>
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</table>
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