To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8/300H Tiny Series

WDT Function

Introduction

A watchdog operation is performed by using the watchdog timer (WDT).

Target Device

H8/36912

Contents

1. Specifications 2
2. Description of Functions 3
3. Description of Operation 5
4. Description of Software 6
5. Flowchart 10
6. Program Listing 13

1. Specifications

A watchdog operation is performed by using the watchdog timer.

The overflow period of the timer counter WD is set to 245.76 ms, and an internal reset signal is generated if the timer counter WD is not initialized within 245.76 ms.

During normal operation, the P20 output value is inverted at constant intervals to confirm the operation and the timer counter WD is initialized to H'10 before it overflows.

If the switch connected to the $\overline{\text{IRQ3}}$ input pin is turned on, the timer counter WD is not initialized and an internal reset is generated when the WD overflows.

The type of reset that has occurred (power-on, LVD, or WDT) is determined.

- In power-on reset, normal reset operation is performed.
- In LVD reset, the P20 output value is inverted.
- In WDT reset, WRST is cleared and the WDT reset counter is incremented.

After WDT reset has occurred three times, the WDT function is disabled, and normal operation is continued.

2. Description of Functions

2.1 Functions Used in This Application

In this sample task, a watchdog operation is implemented using the watchdog timer function. Figure 1 is a block diagram of the watchdog timer. The functions used in this sample task are described below.

- System clock (ϕ)
  This is a reference clock used to drive the CPU and peripheral functions. In this sample task, the internal operating frequency is 8MHz.
- Prescaler S (PSS)
  This is a 13-bit counter which takes ϕ as input, and counts up once each clock cycle.
- Timer control/status register WD (TCSRWD)
  This is an 8-bit readable/writable register that controls writing to TCSRWD and TCWD, controls watchdog timer operation, and indicates the status of watchdog timer operation. The watchdog timer is enabled in the initial state and starts operation after the reset state is released.
- Timer counter WD (TCWD)
  This is an 8-bit readable/writable upward counter that is incremented by internal clock input. In this sample task, ϕ/8192 is selected as the input clock.
- Timer mode register (TMWD)
  This register selects an input clock. In this sample task, ϕ/8192 is selected.
- Low-voltage detection control register (LVDCR)
  This register sets whether the low-voltage detection circuit is used, whether the BGR circuit is used, and sets the LVDR detection level, as well as enabling/disabling reset by the low-voltage detection reset circuit.
- Port mode register 1 (PMR1)
  PMR1 is set so that P17 functions as the $\overline{\text{IRQ3}}$ input pin.
- Interrupt edge select register 1 (IEGR1)
  IEGR1 selects the edge (rising or falling) for interrupt request generation by the $\overline{\text{IRQ3}}$ pin.
- Interrupt enable register 1 (IENR1)
  IENR1 is set to enable the $\overline{\text{IRQ3}}$ pin interrupt.
- Interrupt flag register 1 (IRR1)
  IRR1 contains the IRQ3 interrupt request status flag.
- Port control register 2 (PCR2)
  Each bit of PCR2 selects the input/output of the corresponding port 2 pin which is used as a general I/O port.
- Port data register 2 (PDR2)
  PDR2 is a general I/O port data register for port 2.

TCWD overflow period is calculated by the following equation:

TCWD overflow period = (1/(System clock/8192)) × (256 – (TCWD reload value setting))
= 1.024 [ms] × (256 – 16)
= 245.76 [ms]

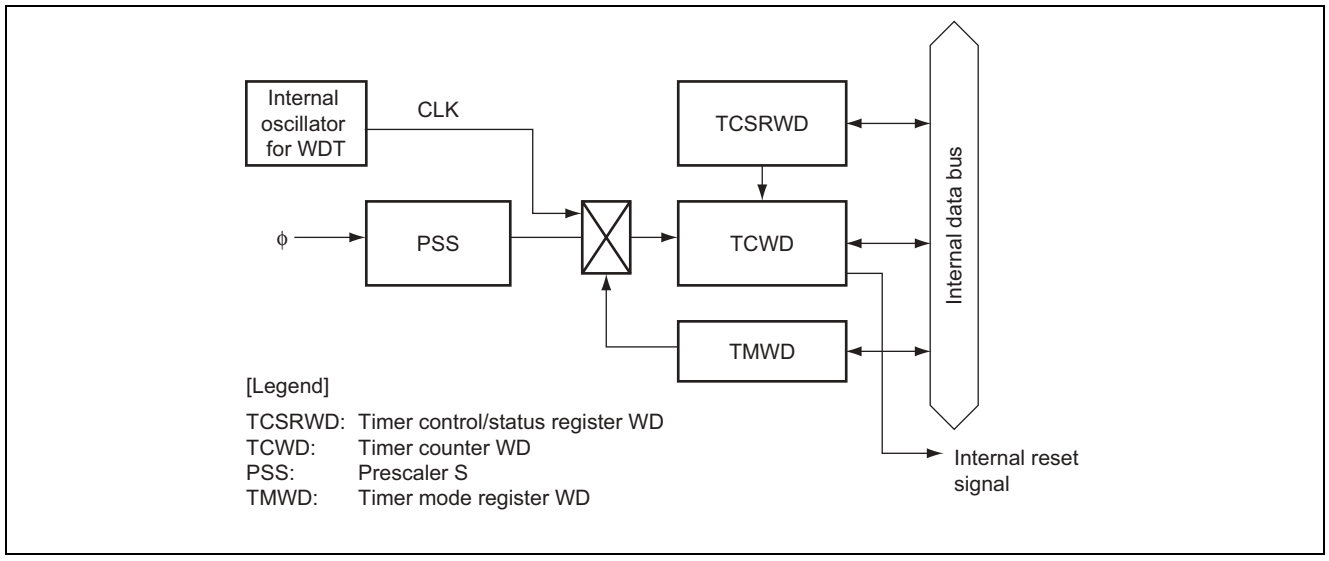


Figure 1 Block Diagram of Watchdog Timer

2.2 Function Assignment

Table 1 lists the assignment of functions used in this sample task. Functions are assigned as listed in this table to implement the watchdog operation.

Table 1 Assignment of Functions

Element	Description
TCSRWD	Sets up and stops the watchdog timer.
TCWD	Watchdog timer counter
TMWD	Sets the TCWD input clock to ϕ/8192.
LVDCR	Provides settings for the low-voltage detection circuit.
PMR1	Sets up P17 as the $\overline{\text{IRQ3}}$ input pin.
IEGR1	Selects falling edge detection for the $\overline{\text{IRQ3}}$ pin input.
IENR1	Enables interrupt requests by the $\overline{\text{IRQ3}}$ pin.
IRR1	Indicates the IRQ3 interrupt request status flag.
PCR2	Sets up P20 to function as an output pin, which is used to confirm the operation.
PDR2	Sets an output value for P20, which is used to confirm the operation.

3. Description of Operation

Figure 2 illustrates the operation of this sample task. Through the hardware and software processing shown in figure 2, watchdog operation is implemented using the watchdog timer function.

After WDT reset has occurred three times, the WDT is stopped.

If a LVD reset occurs while the program is running, the P20 output value is inverted.

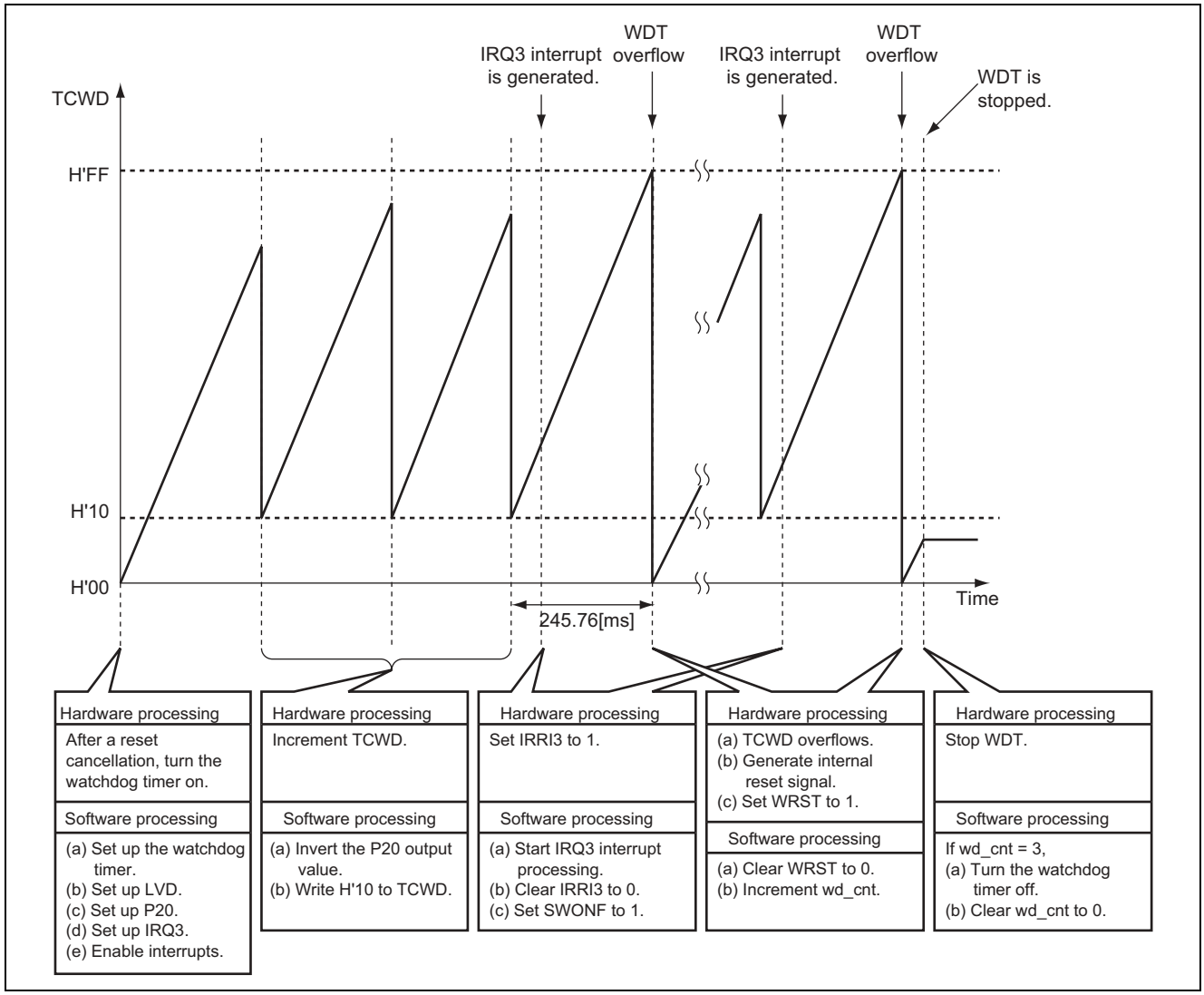


Figure 2 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Function Name	Function
main	Controls the watchdog timer function, sets up the LVD circuit, IRQ3 interrupt and P20 pin, enables interrupts, and determines the type of reset which has occurred.
irq3int	IRQ3 interrupt processing routine that clears IRRI3 and sets SWONF to 1.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- LVDCR: Low-voltage detection control register (Address: H'F730)

Bit	Bit Name	Setting	R/W	Function
7	LVDE	1	R/W	LVD Enable 0: The low-voltage detection circuit is not used. 1: The low-voltage detection circuit is used. When the BGRE bit in this register is cleared to 0, the low-voltage detection circuit is not used regardless of the LVDE bit setting.
6	BGRE	1	R/W	BGR Enable 0: The BGR circuit* is not used. 1: The BGR circuit* is used.
5	VDDII	0	R/W	External LVDI Comparison Voltage Input Disable 0: External voltage is used as LVDI comparison voltage. 1: Internal voltage is used as LVDI comparison voltage.
3	LVDSEL	1	R/W	LVDR Detection Level Selection 0: Reset detection voltage is 2.3 V (typ.) 1: Reset detection voltage is 3.6 V (typ.)
2	LVDRE	1	R/W	LVDR Enable 0: Disables a reset by LVDR. 1: Enables a reset by LVDR.

Note: * A circuit that outputs a stable reference voltage over the entire ranges of the operating voltage and operating temperature that are given in the "Electrical Characteristics".

- TCSRWD: Timer control status register WD (Address: H'FFC0)

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit-6 Write Disable Writing to bit 6 of this register is only enabled when a 0 is written to this bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable When this bit is set to 1, writing to TCWD is enabled. Note that bit 7 should be cleared to 0 to write data to this bit.
5	B4WI	1	R/W	Bit-4 Write Disable Writing to bit 4 of this register is only enabled when a 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD Write Disable When this bit is set to 1, writing to bits 0 and 2 of this register is enabled. Note that bit 5 should be cleared to 0 when writing to this bit.
3	B2WI	1	R/W	Bit-2 Write Disable Writing to bit 2 of this register is only enabled when a 0 is written to this bit. This bit is always read as 1.
2	WDON	1	R/W	Watchdog Timer On When this bit is set to 1, TCWD starts counting up. When cleared to 0, TCWD stops counting. The watchdog timer is ON with the initial value of this bit. When not using the watchdog timer, this bit should be cleared to 0. [Clearing conditions] • Reset • When B2WI and WDON are cleared to 0 while TCSRWE = 1. [Setting condition] • When B2WI is cleared to 0 and WDON is set to 1 while TCSRWE = 1.
1	B0WI	1	R/W	Bit-0 Write Disable Writing to bit 0 of this register is only enabled when a 0 is written to this bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing conditions] • Reset by the $\overline{\text{RES}}$ pin • When B0WI and WRST are cleared to 0 while TCSRWE = 1. [Setting condition] • When TCWD overflow has occurred and an internal reset signal is generated.

- TCWD: Timer counter WD (Address: H'FFC1)
  - Function: TCWD is an 8-bit readable/writable upward-counter. If TCWD overflows from H'FF to H'00, an internal reset signal is generated and WRST in TCSRWD is set to 1. The initial value of TCWD is H'00.
  - Setting value: H'10

- TMWD: Timer mode register WD (Address: H'FFC2)

Bit	Bit Name	Setting	R/W	Function
3	CKS3	1	R/W	Clock Select 3 to 0
2	CKS2	1	R/W	These bits select the input clock of TCWD.
1	CKS1	1	R/W	0xxx: Clock from the internal oscillator for WDT
0	CSK0	1	R/W	1000: Internal clock ϕ/64 1001: Internal clock ϕ/128 1010: Internal clock ϕ/256 1011: Internal clock ϕ/512 1100: Internal clock ϕ/1024 1101: Internal clock ϕ/2048 1110: Internal clock ϕ/4096 1111: Internal clock ϕ/8192 For details on the overflow period by the clock from the internal oscillator for WDT, refer to "Electrical Characteristics" in the hardware manual.

Note: x: Don't care

- PDR2: Port data register 2 (Address: H'FFD5)

Bit	Bit Name	Setting	R/W	Function
0	P20	0	R/W	Stores port 2 output value. When this register is read, the value of this register is read for a bit whose corresponding bit in PCR2 is set to 1; for a bit whose corresponding bit in PCR2 is clear, the pin state is read regardless of the value of this register.

- PMR1: Port mode register 1 (Address: H'FFE0)

Bit	Bit Name	Setting	R/W	Function
7	IRQ3	1	R/W	Selects the function of the P17/$\overline{\text{IRQ3}}$/TRGV pin. 0: The pin functions as general I/O port P17. 1: The pin functions as the $\overline{\text{IRQ3}}$ or TRGV input pin.

- PCR2: Port control register 2 (Address: H'FFE5)

Bit	Bit Name	Setting	R/W	Function
0	PCR20	1	W	When this bit is set to 1 while the general I/O port function is selected, the corresponding pin functions as an output port; and when cleared to 0, the pin functions as an input port.

- IEGR1: Interrupt edge select register 1 (Address: H'FFF2)

Bit	Bit Name	Setting	R/W	Function
3	IEG3	0	R/W	IRQ3 Edge Select 0: Detects the falling edge of the $\overline{\text{IRQ3}}$ pin input. 1: Detects the rising edge of the $\overline{\text{IRQ3}}$ pin input.

- IENR1: Interrupt enable register 1 (Address: H'FFF4)

Bit	Bit Name	Setting	R/W	Function
3	IEN3	1	R/W	IRQ3 Interrupt Request Enable When this bit is set to 1, interrupt requests of the $\overline{\text{IRQ3}}$ pin are enabled.

- IRR1: Interrupt flag register 1 (Address: H'FFF6)

Bit	Bit Name	Setting	R/W	Function
3	IRRI3	0	R/W	IRQ3 Interrupt Request Flag Setting condition: • When the $\overline{\text{IRQ3}}$ pin is enabled and the specified edge is detected. Clearing condition: • When a 0 is written to this bit.

4.4 RAM Usage

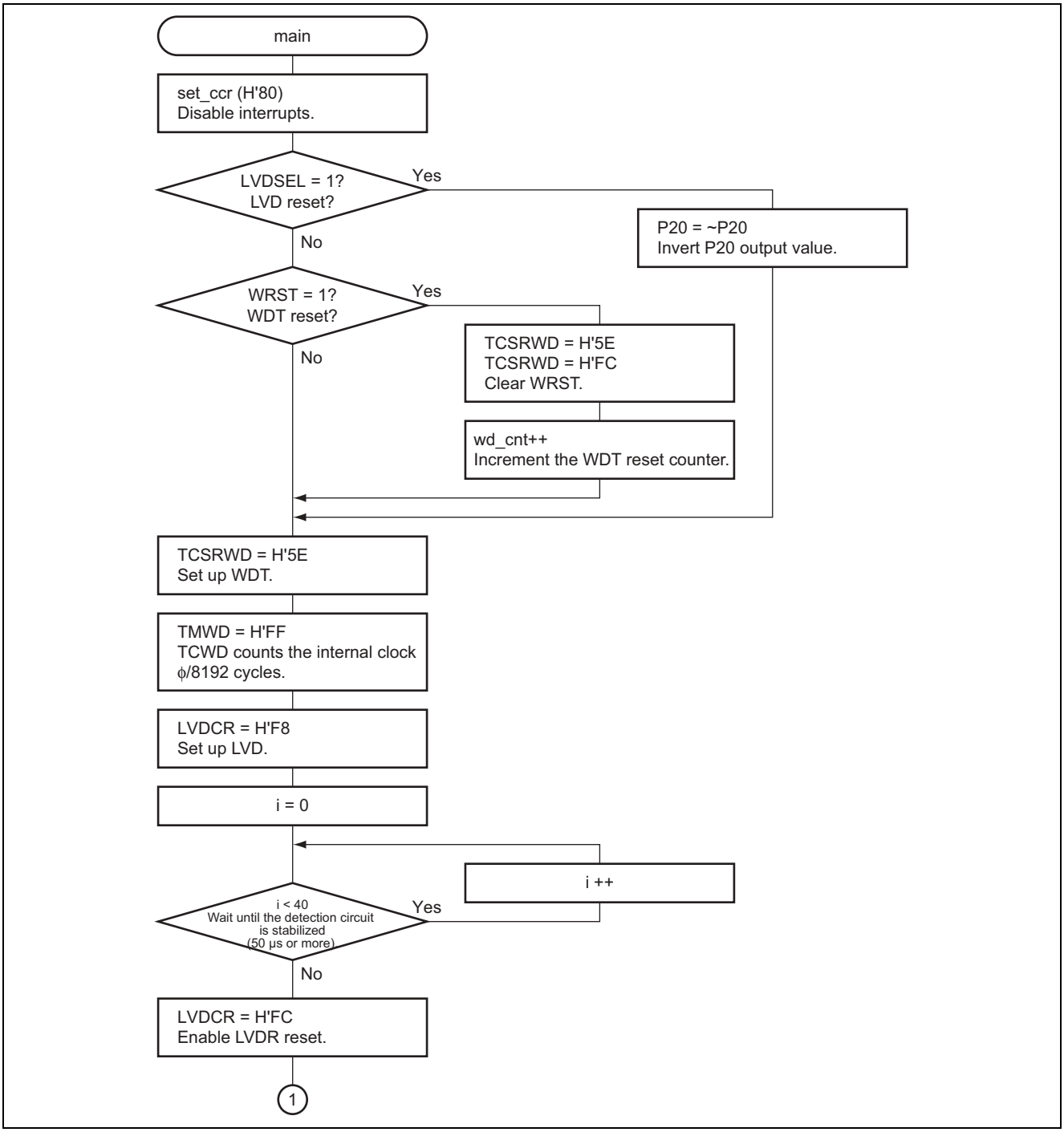
Table 3 describes the RAM usage in this sample task.

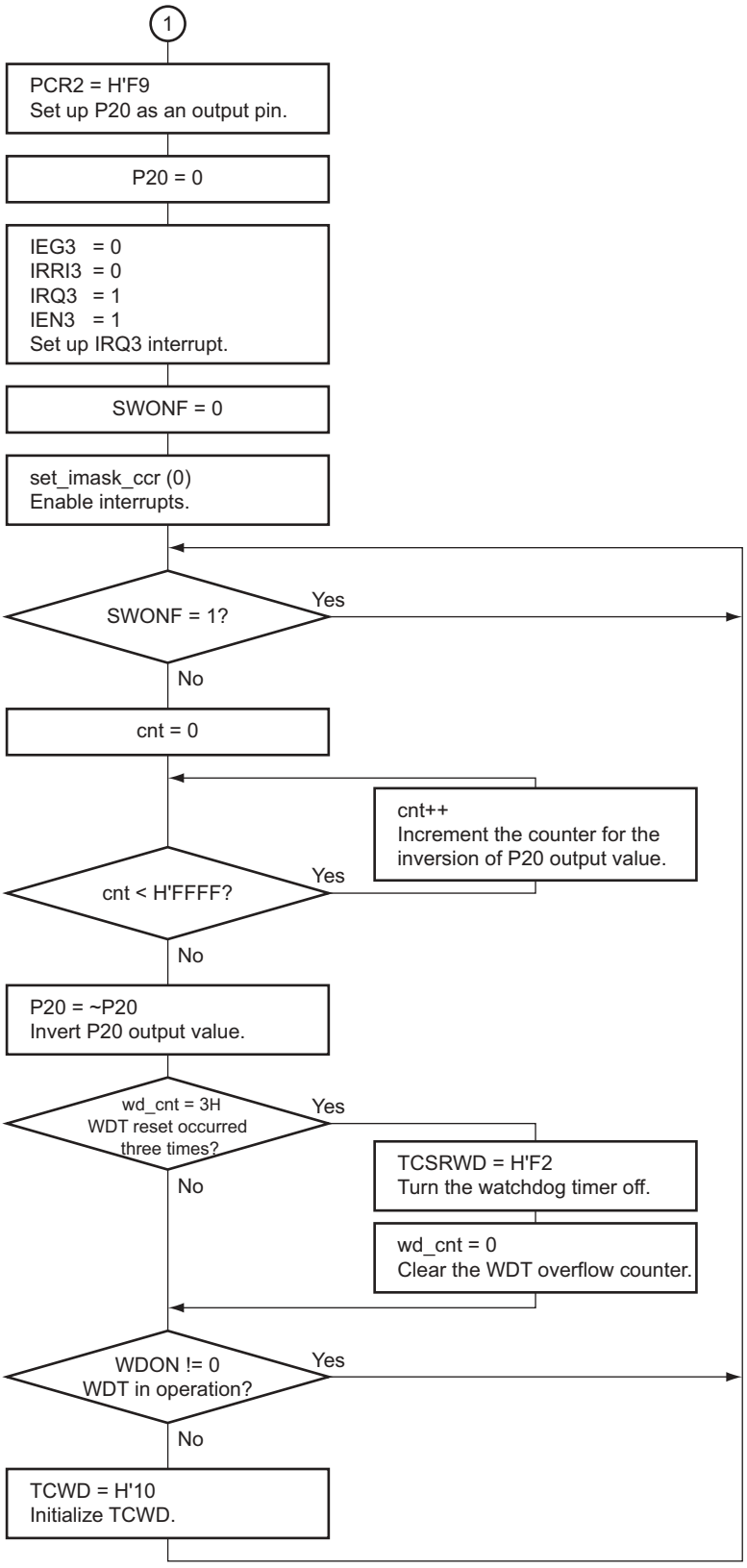
Table 3 Description of RAM

Constant Name	Function	Size	Used in
wd_cnt	Counts the number of watchdog counter overflows	1 byte	main
SWONF	Indicates whether an IRQ3 interrupt has occurred 0: No IRQ3 interrupt has occurred 1: An IRQ3 interrupt has occurred	1 byte	main IRQ3int

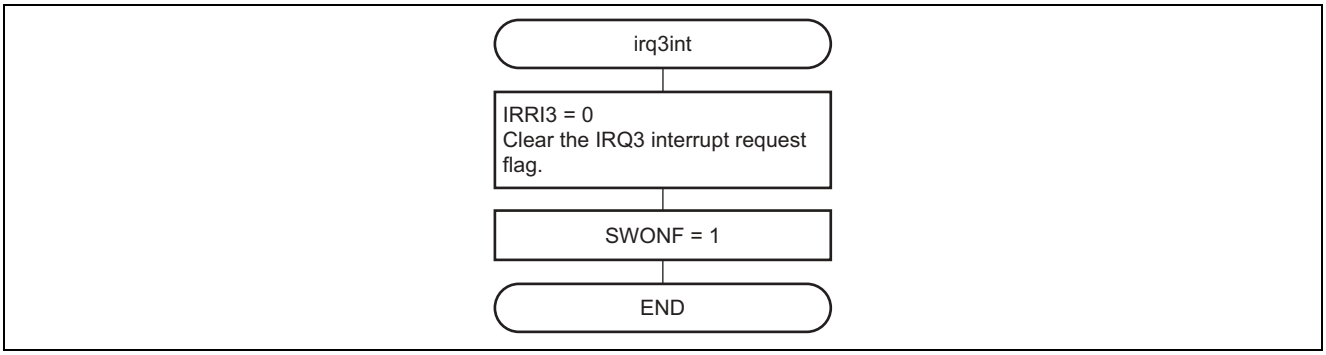
5. Flowchart

5.1 main




1
PCR2 = H'F9
Set up P20 as an output pin.
P20 = 0
IEG3 = 0
IRRI3 = 0
IRQ3 = 1
IEN3 = 1
Set up IRQ3 interrupt.
SWONF = 0
set_imask_ccr (0)
Enable interrupts.
SWONF = 1?
Yes
No
cnt = 0
cnt++
Increment the counter for the inversion of P20 output value.
cnt < H'FFFF?
Yes
No
P20 = ~P20
Invert P20 output value.
wd_cnt = 3H
WDT reset occurred three times?
Yes
No
TCSRWD = H'F2
Turn the watchdog timer off.
wd_cnt = 0
Clear the WDT overflow counter.
WDON != 0
WDT in operation?
Yes
No
TCWD = H'10
Initialize TCWD.

5.2 irq3int


irq3int
IRRI3 = 0
Clear the IRQ3 interrupt request flag.
SWONF = 1
END

6. Program Listing

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300H Series -H8/36912-                                                                   */
/*  Application Note                                                                            */
/*                                                                                              */
/*  'WDT'                                                                                       */
/*                                                                                              */
/*  Function                                                                                    */
/*  : WDT (Watch Dog Timer)                                                                     */
/*                                                                                              */
/*  External Clock : 8MHz                                                                       */
/*  Internal Clock : 8MHz                                                                       */
/*  Sub Clock      : 32.768kHz                                                                  */
/*                                                                                              */
/************************************************************************************************/

#include    <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define TCSRWD      *(volatile unsigned char *)0xFFC0   /* Timer Controller/Status Register WD */
#define TCSRWD_BIT  (*(volatile struct BIT *)0xFFC0)
#define B6WI        TCSRWD_BIT.b7                       /* Bit 6 Write Disable                 */
#define TCWE        TCSRWD_BIT.b6                       /* Timer Counter W Write Enable        */
#define B4WI        TCSRWD_BIT.b5                       /* Bit 4 Write Disable                 */
#define TCSRWE      TCSRWD_BIT.b4                       /* Timer Controller/                   */
                                                        /*            Status Register W Enable */
#define B2WI        TCSRWD_BIT.b3                       /* Bit 2 Write Disable                 */
#define WDON        TCSRWD_BIT.b2                       /* WD Timer ON                         */
#define B0WI        TCSRWD_BIT.b1                       /* Bit 0 Write Disable                 */
#define WRST        TCSRWD_BIT.b0                       /* WD Timer Reset                      */
#define TCWD        *(volatile unsigned char *)0xFFC1   /* Timer Counter WD                    */
#define TMWD        *(volatile unsigned char *)0xFFC2   /* Timer Mode WD                       */

#define LVDCR       *(volatile unsigned char *)0xF730   /* Low-Voltage-Detect control register */
#define LVDCR_BIT   (*(volatile struct BIT *)0xF730)
#define LVDE        LVDCR_BIT.b7                        /* LVD Enable                          */
#define BGRE        LVDCR_BIT.b6                        /* BGR Enable                          */
#define VDDII       LVDCR_BIT.b5                        /* Select LVDI comparative voltage     */
#define LVDSEL      LVDCR_BIT.b3                        /* LVDI Detection Level Select         */
```

```
#define LVDRE       LVDCR_BIT.b2                        /* LVDR Enable                          */
#define PMR1        *(volatile unsigned char *)0xFFE0   /* Port Mode Register 1                 */
#define PMR1_BIT    (*(volatile struct BIT *)0xFFE0)
#define IRQ3        PMR1_BIT.b7                         /* P17/IRQ3/TRGV Pin Function Switch    */
#define IEGR1       *(volatile unsigned char *)0xFFF2   /* Interrupt Edge Select Register       */
#define IEGR1_BIT   (*(volatile struct BIT *)0xFFF2)
#define IEG3        IEGR1_BIT.b3                        /* IRQ3 Edge Select                     */
#define IENR1       *(volatile unsigned char *)0xFFF4   /* Interrupt Enable Register 1          */
#define IENR1_BIT   (*(volatile struct BIT *)0xFFF4)
#define IEN3        IENR1_BIT.b3                        /* IRQ3 Interrupt Enable                */
#define IRR1        *(voltage unsigned char *)0xFFF6    /* Interrupt Request Register 1         */
#define IRR1_BIT    (*(volatile struct BIT *)0xFFF6)
#define IRRI3       IRR1_BIT.b3                         /* IRQ3 Interrupt Request Flag          */

#define PCR2        *(volatile unsigned char *)0xFFE5   /* Port Control Register 2              */
#define PCR2_BIT    (*(volatile struct BIT *)0xFFE5)
#define PCR20       PCR2_BIT.b0                         /* Port Control Register 2 bit 0        */
#define PDR2        *(volatile unsigned char *)0xFFD5   /* Port Data Register 2                 */
#define PDR2_BIT    (*(volatile struct BIT *)0xFFD5)
#define P20         PDR2_BIT.b0                         /* Port Data Register 2 bit 0           */

#pragma interrupt (irq3int)
/************************************************************************************************/
/*  Function define                                                                             */
/************************************************************************************************/
void main ( void );
void irq3int ( void );
/************************************************************************************************/
/*  RAM define                                                                                  */
/************************************************************************************************/
unsigned char SWONF;
unsigned char wd_cnt=0;                                 /* WDT reset counter                    */
/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section     V1                                  /* VECTOR SECTOIN SET                   */
void (*const VEC_TBL1[])(void) = {
    main
};

#pragma section     V2                                  /* VECTOR SECTOIN SET                   */
void (*const VEC_TBL2[])(void) = {
    irq3int                                             /* IRQ3 interrupt                       */
};

#pragma entry main(sp=0xFF80)
#pragma section                                         /* P                                    */
```

```
/*****************************************************************************************************/
/*  Main Program                                                                                     */
/*****************************************************************************************************/
void main ( void )
{
    unsigned short cnt;

    set_ccr(0x80);                                  /* Interrupt Disable                    */

    if(LVDSEL == 1)                                 /* LVD reset ?                          */
        P20 = ~P20;                                 /* The reversal of the output value     */
    else if(WRST == 1){                             /* WDT reset ?                          */
        TCSRWD = 0x5E;                              /* WRST                                 */
        TCSRWD = 0xFC;                              /* Clear                                */
        wd_cnt++;                                   /* Count up WDT reset                   */
    }

    TCSRWD = 0x5E;                                  /* Set up Watch Dog Timer               */
    TMWD = 0xFF;                                    /* TCWD -> input phi/8192 clock         */

    LVDCR = 0xF8;                                   /* Set up LVD                           */
    for(cnt=0; cnt<40; cnt++);                      /* wait Detection circuit stable time   */
                                                    /*                          (50us over) */

    LVDCR = 0xFC;                                   /* Set LVDRE                            */

    PCR2 = 0xF9;                                    /* P20 -> output                        */
    P20 = 0;                                        /* For the movement confirmation        */

    IEG3 = 0;                                       /* IRQ3 Interrupt Edge Select           */
    IRRI3 = 0;                                      /* Clear IRQ3 Interrupt Flag            */
    IRQ3 = 1;
    IEN3 = 1;                                       /* IRQ3 Interrupt Enable                */

    SWONF = 0;                                      /* Initialize SWONF                     */

    set_imask_ccr(0);                               /* Interrupt Enable                     */

    while(1){

        while(SWONF == 1);                          /* SWONF = 1 ?                          */

        for(cnt=0; cnt<0xFFFF; cnt++);              /* cnt Count up (P20 High, Low wait)    */

        P20 = ~P20;                                 /* The reversal of the output value     */

        if(wd_cnt == 3){                            /* WDT reset is three times ?           */
            TCSRWD = 0xF2;                          /* WDT STOP                             */
            wd_cnt = 0;                             /* Clear wd_cnt                         */
        }
        else if(WDON != 0)                          /* WDT move ?                           */
            TCWD = 0x10;                            /* Initialize TCWD                      */
    }
}
```

```
/*****************************************************************************************************/
/*  IRQ3 Interrupt                                                                                   */
/*****************************************************************************************************/
void irq3int ( void )
{
    IRRI3 = 0;                                          /* Clear IRQ3 Interrupt Flag           */

    SWONF = 1;                                          /* Set SWONF                           */
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0022
P	H'0100
B	H'FD80
D	

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.28.04	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.