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H8/300H Tiny Series

LCD Display by the External Driver

Introduction

This application note describes how to display characters on the LCD using the general I/O port.

Target Device

H8/3687

M1641 (LCD unit)

Contents

1. Specifications

An LCD is connected as shown in figure 1 and characters are displayed on the LCD through port operation.

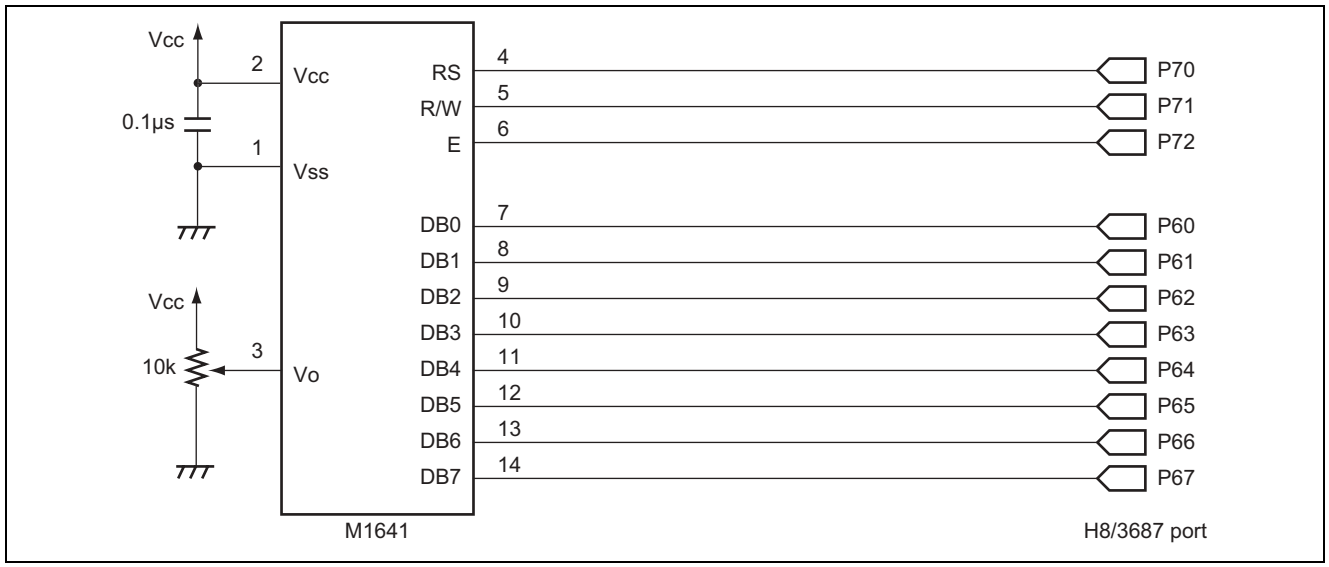


Figure 1 LCD Connections

Table 1 summarizes the LCD pin functions.

Table 1 LCD Interface Signals

Pin No.	Symbol	Function
1	Vss	Ground voltage
2	Vcc	Power supply voltage for the logic circuit
3	V_0	Power supply voltage for contrast adjustment
4	RS	Register select
5	R/W	Read/write
6	E	Enable
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)

Table 2 shows the correspondence between character codes and characters to be displayed.

Table 2 Correspondence between Character Codes and Display Characters

	Upper 4 Bits				
Lower 4 Bits	0000 CG RAM	0010	0011	0100	0101
0000	(1)		0	@	P
0001	(2)	!	1	A	Q
0010	(3)	"	2	B	R
0011	(4)	#	3	C	S
0100	(5)	$	4	D	T
0101	(6)	%	5	E	U
0110	(7)	&	6	F	V
0111	(8)	'	7	G	W
1000	(9)	(	8	H	X
1001	(10)	)	9	I	Y
1010	(11)	*	:	J	Z
1011	(12)	+	;	K	[
1100	(13)	,	<	L	\
1101	(14)	-	=	M	]
1110	(15)	.	>	N	^
1111	(16)	/	?	O	_

2. Description of Functions

2.1 Microcomputer Functions to be Used

In this sample task, characters are displayed on the LCD using the general I/O ports. Ports 6 and 7 are used as general I/O ports and their correspondig registers are summarized below.

- Port control register 6 (PCR6)
  Each bit in this register selects the input or output for each pin of port 6, which is used as a general I/O port.
- Port data register 6 (PDR6)
  This is a general I/O port data register for port 6.
- Port control register 7 (PCR7)
  Each bit in this register selects the input or output for each pin of port 7, which is used as a general I/O port.
- Port data register7 (PDR7)
  This is a general I/O port data register for port 7.

2.2 LCD Functions to be Used

The LCD module functions used in this application are described below. Instructions are listed in table 3. In table 3, DD RAM is a display data RAM that stores display data in 8-bit character codes, and CG RAM is a character generator RAM where the user can freely write and rewrite patterns by software.

Instructions are described below.

1. Clears all the display on the LCD and sets address 0 of DD RAM in the address counter.
2. Sets address 0 of DD RAM in the address counter and returns the shifted display to the home position. The DD RAM contents are not affected.
3. Sets the cursor move direction for data write/read and also sets whether the display is shifted or not.
4. Sets entire display on or off (D), cursor on or off (C), and blinking of the character at the cursor position (B).
5. Moves the cursor and shifts the display without changing the DDRAM contents.
6. Sets interface data length (DL), number of display lines (N), and character font (F).
7. Sets a CG RAM address. (CG RAM data is received or transmitted after a CG RAM address is set.)
8. Sets a DD RAM address. (DD RAM data is received or transmitted after a DD RAM address is set.)
9. Reads the busy flag (BF), which indicates the LCD unit is performing internal processing, and the address counter.
10. Writes data to DD RAM or CG RAM.
11. Reads data from DD RAM or CG RAM

Table 3 List of Instructions

		Codes									
	Instruction	**RS**	**R/W**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
1	Clear display	0	0	0	0	0	0	0	0	0	1
2	Return cursor to home position	0	0	0	0	0	0	0	0	1	*
3	Set entry mode	0	0	0	0	0	0	0	1	I/D	S
4	Display on/off control	0	0	0	0	0	0	1	D	C	B
5	Shift cursor/display	0	0	0	0	0	1	S/C	R/L	*	*
6	Set function	0	0	0	0	1	DL	N	F	*	*
7	Set CG RAM address	0	0	0	1	A_{CG}					
8	Set DD RAM address	0	0	1	A_{DD}						
9	Read busy flag and address	0	1	BF	AC						
10	Write data to CG RAM/DD RAM	1	0	Write Data							
11	Read data from CG RAM/DD RAM	1	1	Read Data							

Note: *: Don't care
I/D = 1: Increments.
I/D = 0: Decrements.
S = 1: Shifts the display
S = 0: Does not shift the display.
D = 1: Turns on entire display
D = 0: Turns off entire display
C = 1: Turns on the cursor
C = 0: Turns off the cursor
B = 1: The character blinks.
B = 0: The character does not blink.
S/C = 1: Shifts the display.
S/C = 0: Does not shift the display.
R/L = 1: Shifts to the right.
R/L = 0: Shifts to the left.
DL = 1: 8 bits
DL = 0: 4 bits
N = 1: Two lines
N = 0: One line
F = 1: 5 × 10 dots
F = 0: 5 × 7 dots
BF = 1: During internal operation
A_{CG}: CG RAM address
A_{DD}: DD RAM address corresponding to the cursor address
AC: Address counter value; used for both DD RAM and CG RAM.

The HD44780 has two 8-bit registers: the instruction register (IR) and data register (DR). These registers can be selected by the register select signal (RS). Table 4 shows the register selection.

- IR
  This register is used to store the instruction codes for display clear, cursor shift and other functions or address information of DD RAM and CG RAM. The IR register can be written by the MPU but cannot be read by the MPU.
- DR
  This register is used for temporal storage of the data to be written to DD RAM/CG RAM or the data read from DD RAM/CG RAM. The data written to DR by the MPU is automatically written to DD RAM/CC RAM through internal operation. The DR register is also used for data storage when data is read from DD RAM or CG RAM. When the address information is written to the IR register, data is read from DD RAM/CG RAM by internal operation. When the MPU reads the DR register at the next instruction, data transfer to the MPU is completed. After the reading, the address information is incremented automatically and the data at the next address in DD RAM/CG RAM is sent to DR to be ready for the next read from the MPU.

Table 4 Register Selection

RS	R/W	Operation
0	0	IR write and internal operation (display clear etc.)
0	1	Busy flag (DB7) and address counter (DB0 to DB6) read
1	0	DR write and internal operation (DR → DD RAM or CG RAM)
1	1	DR read and internal operation (DD RAM or CG RAM → DR)

3. Principles of Operation

The following figures illustrate the operation of this sample task. The port operation shown in figures 2 to 4 are performed to display characters on the LCD.

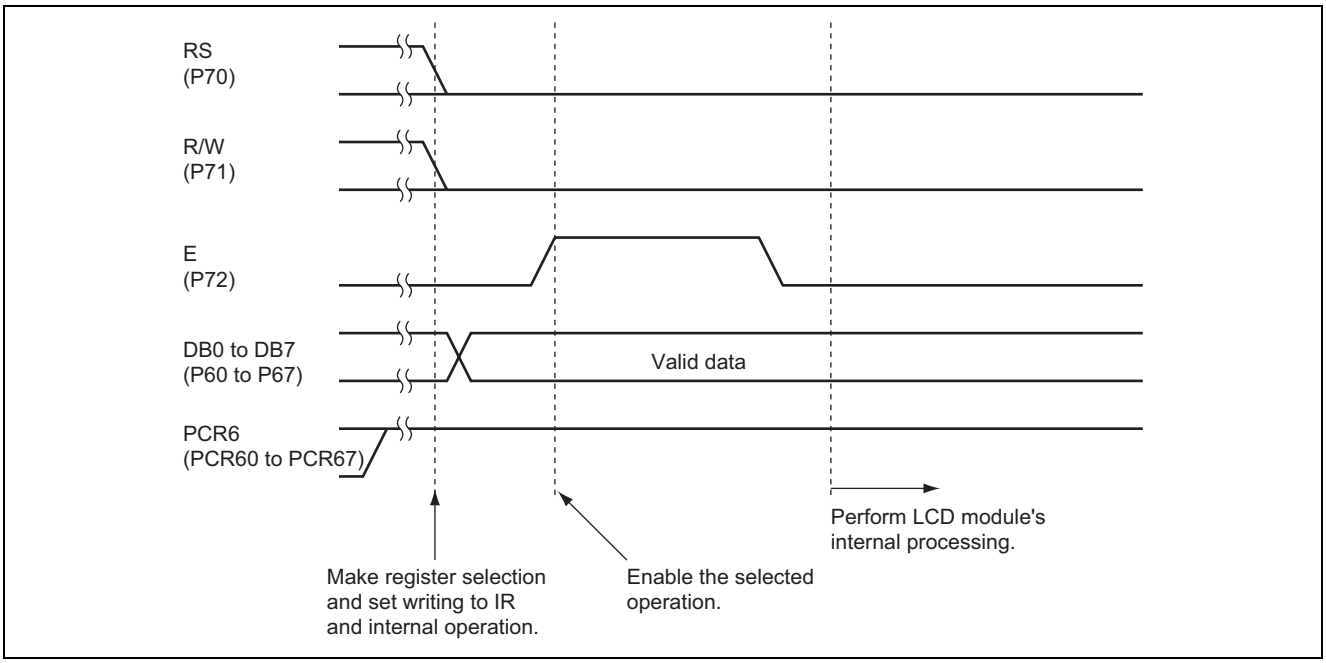


Figure 2 IR Write and Internal Operation (Display Clear and Others)

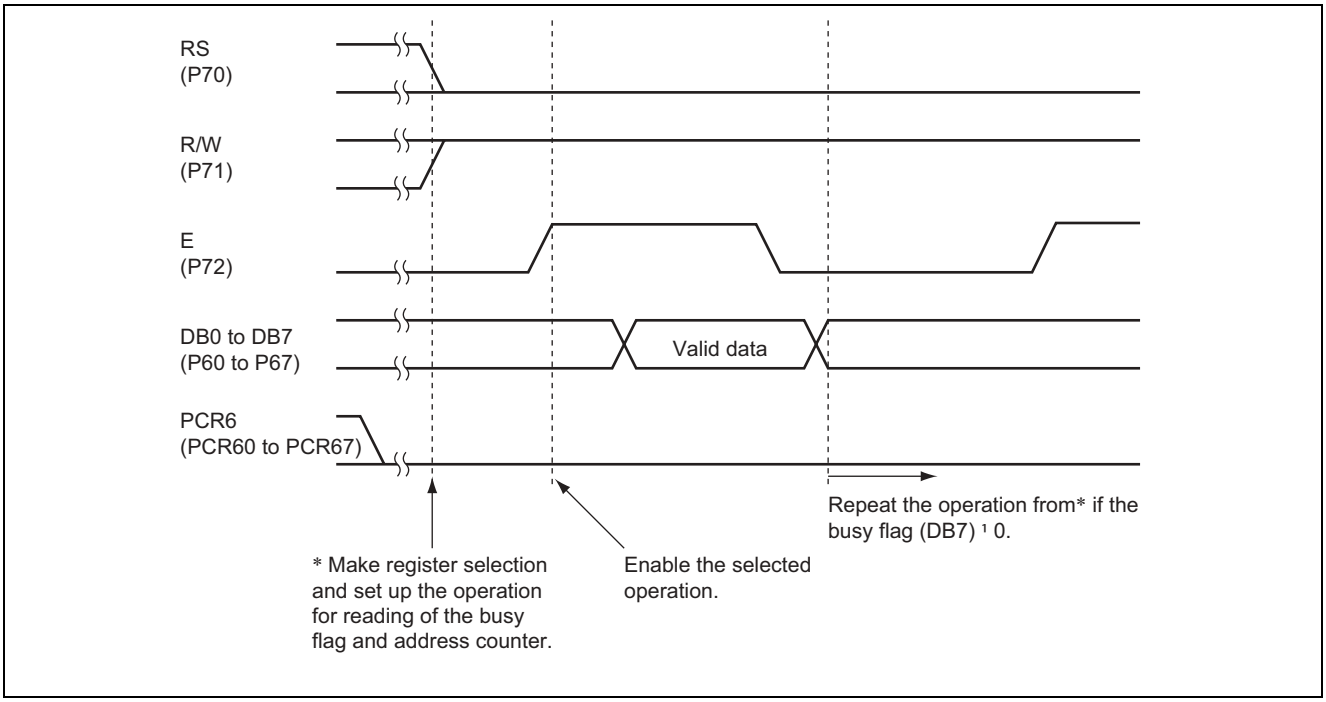


Figure 3 Reading of Busy Flag (DB7) and Address Counter (DB0 to DB6)

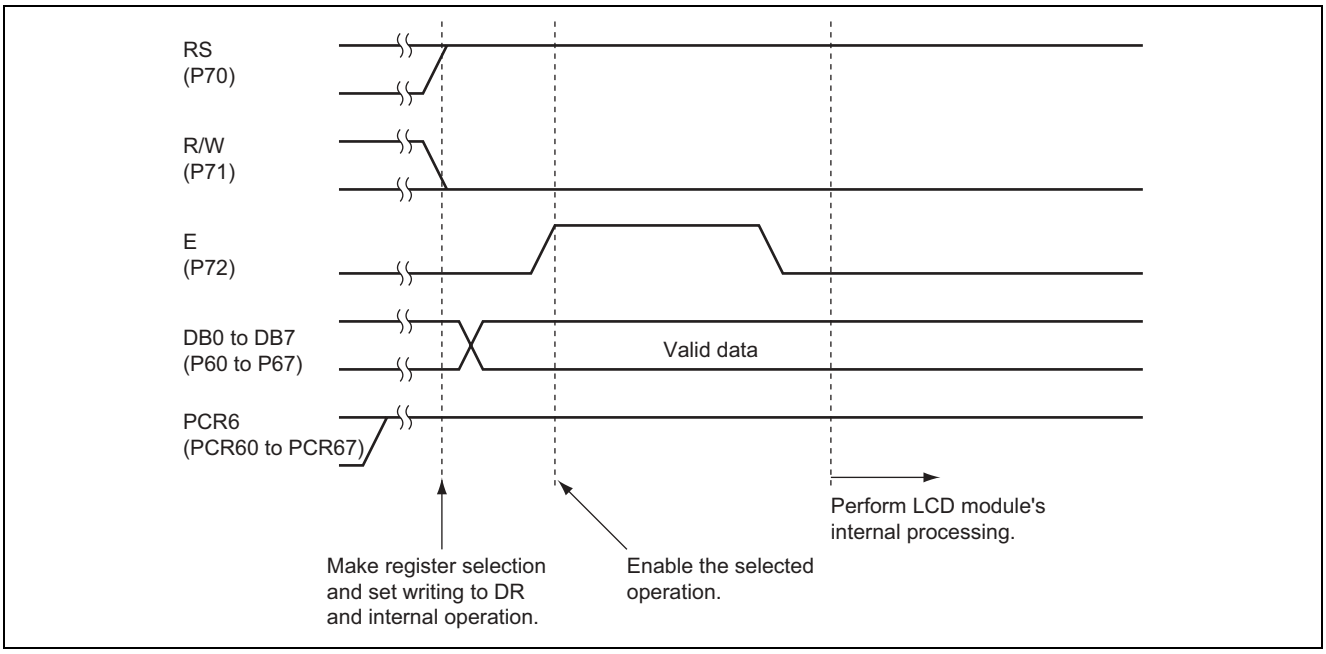


Figure 4 IR Write and Internal Operation (DR → DD RAM or CG RAM)

The HD44780 operation is described below. Figure 6 shows the display layout of LCD. Characters are displayed on the LCD using the instructions in table 3.

(1) Initialization
Set the interface data length as 8 bits, number of display lines as two, and character font as 5 × 7 dots.
Turn on the display, cursor, and blinking of the character at the cursor position.
Set the cursor shift direction in data reading/writing.
Set the DD RAM address to H'00.

(2) First line display
Display "H8/300H" in the first line.

(3) Set the DD RAM address
Set the DD RAM address at the beginning of the second line.

(4) Second line display
Display "3687" in the second line.

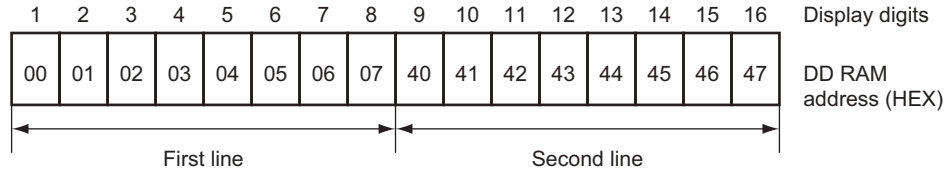


Figure 5 Display Layout

(1) Initialization

(2) Display the first line.

H 8 / 3 0 0 H

(3) Set the DDRAM address at the beginning of the second line

H 8 / 3 0 0 H

(4) Display the second line.

H 8 / 3 0 0 H 3 6 8 7

Figure 6 LCD Display

The bus write operation sequence is shown in figure 7 and table 5. The measurement conditions for the values in table 5 are as shown in figure 7.

In figure 7, V_H = 4.5 V and V_L = 0.2 V.

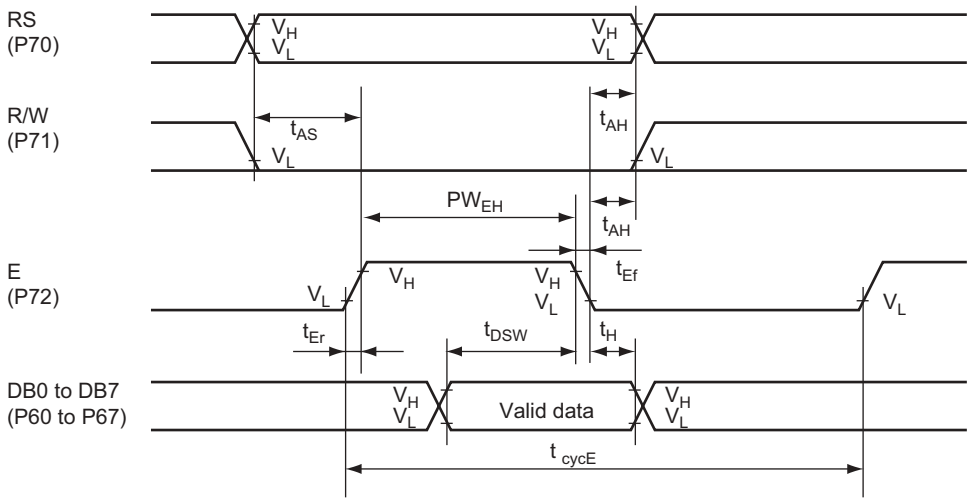


Figure 7 Bus Write Operation Sequence

Table 5 Bus Write Operation Sequence

Item	Symbol	Values		Unit
		Min.	Max.	
Enable cycle time	t_{cycE}	1000	—	ns
Enable pulse high-level width	PW_{EH}	450	—	ns
Enable rise or fall time	t_{Er}, t_{Ef}	—	25	ns
Set-up time for RS, R/W and E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data set-up time	t_{DSW}	195	—	ns
Data hold time	t_H	10	—	ns

The bus read sequence is shown in figure 8 and table 6. The measurement conditions for the values in table 6 are as shown in figure 8.

In figure 8, V_H = 4.5 V and V_L = 0.2 V.

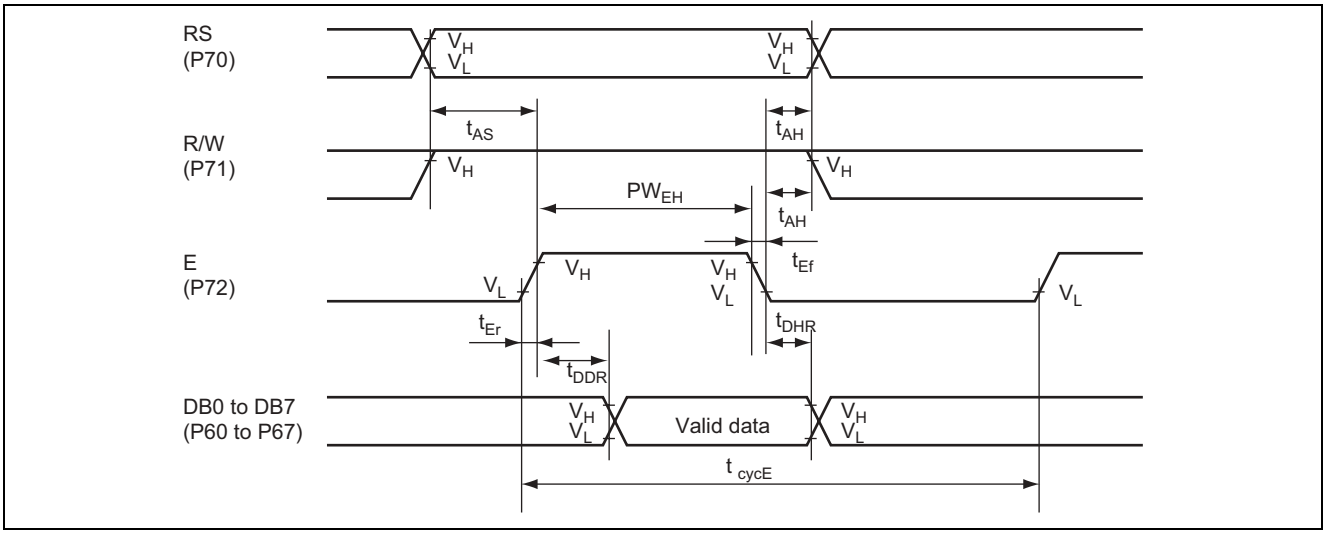


Figure 8 Bus Read Operation Sequence

Table 6 Bus Read Operation Sequence

Item	Symbol	Values		Unit
		Min.	Max.	
Enable cycle time	t_{cycE}	1000	—	ns
Enable pulse high-level width	PW_{EH}	450	—	ns
Enable rise or fall time	t_{Er}, t_{Ef}	—	25	ns
Set-up time for RS, R/W and E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	—	320	ns
Data hold time	t_{DHR}	20	—	ns

4. Description of Software

4.1 Modules

Table 7 shows the modules used in this sample task.

Table 7 Description of Modules

Label Name	Function
main	Controls the LCD.
Check_bf	Checks the busy flag.
Set_up	Writes to IR (instruction register).
Write_data	Writes to DR (data register).

4.2 Arguments

Table 8 shows the arguments used in this sample task.

Table 8 Description of Arguments

Label Name	Argument	Description
Set_up	unsigned char data	Data to be written to IR
Write_data	unsigned char data	Data to be written to DR

4.3 Constants

Table 9 shows the constants used in this sample task.

Table 9 Constants

Label Name	Buffer Name	Constant	Function
Set_up	Initialization[0]	H'38	Function setting
	Initialization[1]	H'0F	Display on/off control
	Initialization[2]	H'06	Entry mode setting
	Initialization[3]	H'80	Set the cursor at the start address of the first line.
Write_data	wr_data1[0]	H'48	"H"
	wr_data1[1]	H'38	"8"
	wr_data1[2]	H'2F	"/"
	wr_data1[3]	H'33	"3"
	wr_data1[4]	H'30	"0"
	wr_data1[5]	H'30	"0"
	wr_data1[6]	H'48	"H"
	wr_data2[0]	H'20	" "
	wr_data2[1]	H'33	"3"
	wr_data2[2]	H'36	"6"
	wr_data2[3]	H'38	"8"
	wr_data2[4]	H'37	"7"

4.4 Internal Registers

The internal registers used in this sample task are described below.

- PCR6: Port Control Register 6 (Address: H'FFE9)

Bit	Bit Name	Setting	R/W	Function
7	PCR67	1	W	If a bit in this register is set to 1 while a general I/O port function is selected, the corresponding pin functions as an output port; if a bit in this register is cleared to 0, the corresponding pin functions as an input port.
6	PCR66	1	W	
5	PCR65	1	W	
4	PCR64	1	W	
3	PCR63	1	W	
2	PCR62	1	W	
1	PCR61	1	W	
0	PCR60	1	W	

- PDR6: Port Data Register 6 (Address: H'FFD9)

Bit	Bit Name	Setting	R/W	Function
7	P67	—	R/W	Stores port 6 output values. When this register is read, the value in this register is read for the bits whose corresponding bits in PCR6 are set to 1; for the bits whose corresponding bits in PCR6 are clear, the pin states are read regardless of the value of this register.
6	P66	—	R/W	
5	P65	—	R/W	
4	P64	—	R/W	
3	P63	—	R/W	
2	P62	—	R/W	
1	P61	—	R/W	
0	P60	—	R/W	

- PCR7: Port Control Register 7 (Address: H'FFEA)

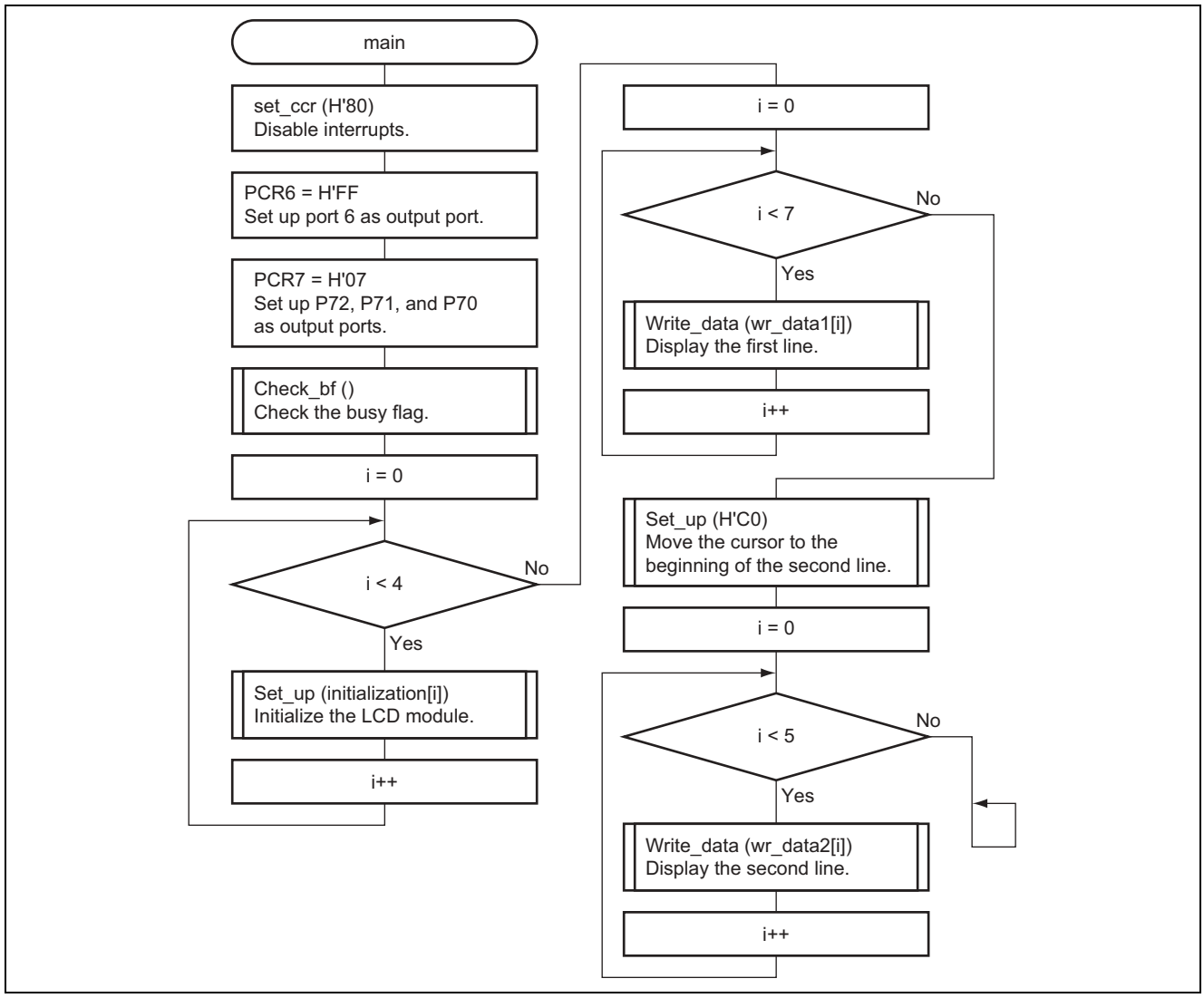
Bit	Bit Name	Setting	R/W	Function
2	PCR72	1	W	If a bit in this register is set to 1 while a general I/O port function is selected, the corresponding pin functions as an output port; if a bit in this register is cleared to 0, the corresponding pin functions as an input port.
1	PCR71	1	W	
0	PCR70	1	W	

- PDR7: Port Data Register 7 (Address: H'FFDA)

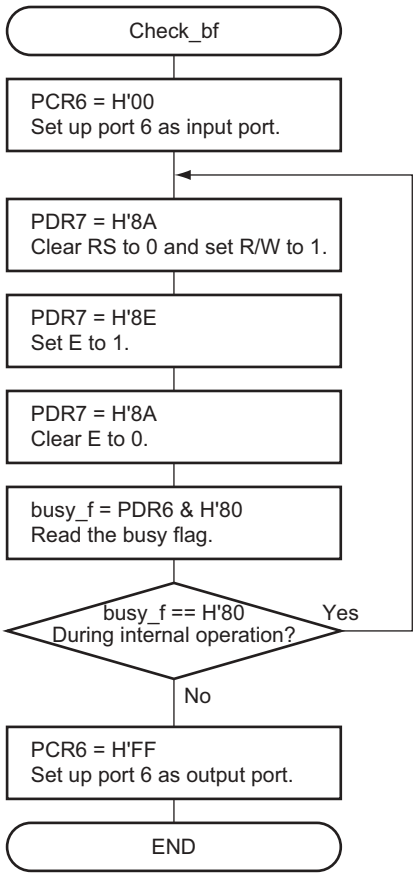
Bit	Bit Name	Setting	R/W	Function
2	PDR72	—	R/W	Stores port 7 output values. When this register is read, the value in this register is read for the bits whose corresponding bits in PCR7 are set to 1; for the bits whose corresponding bits in PCR7 are clear, the pin states are read regardless of the value of this register.
1	PDR71	—	R/W	
0	PDR70	—	R/W	

5. Flowchart

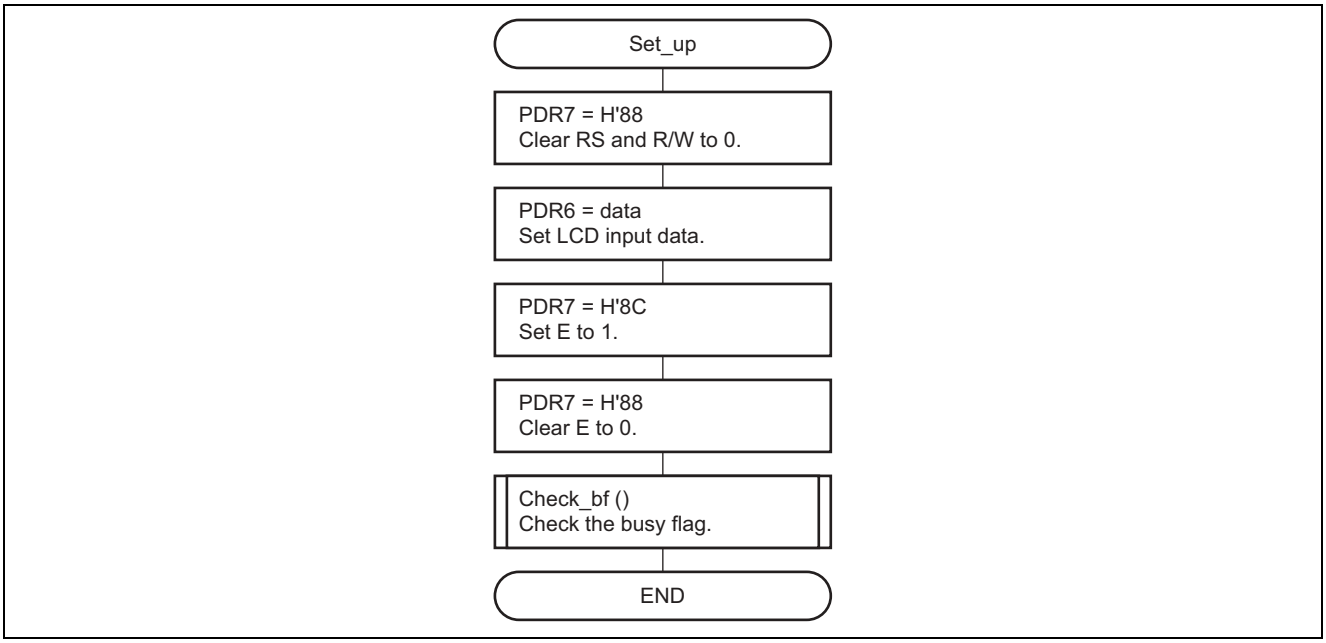
5.1 main



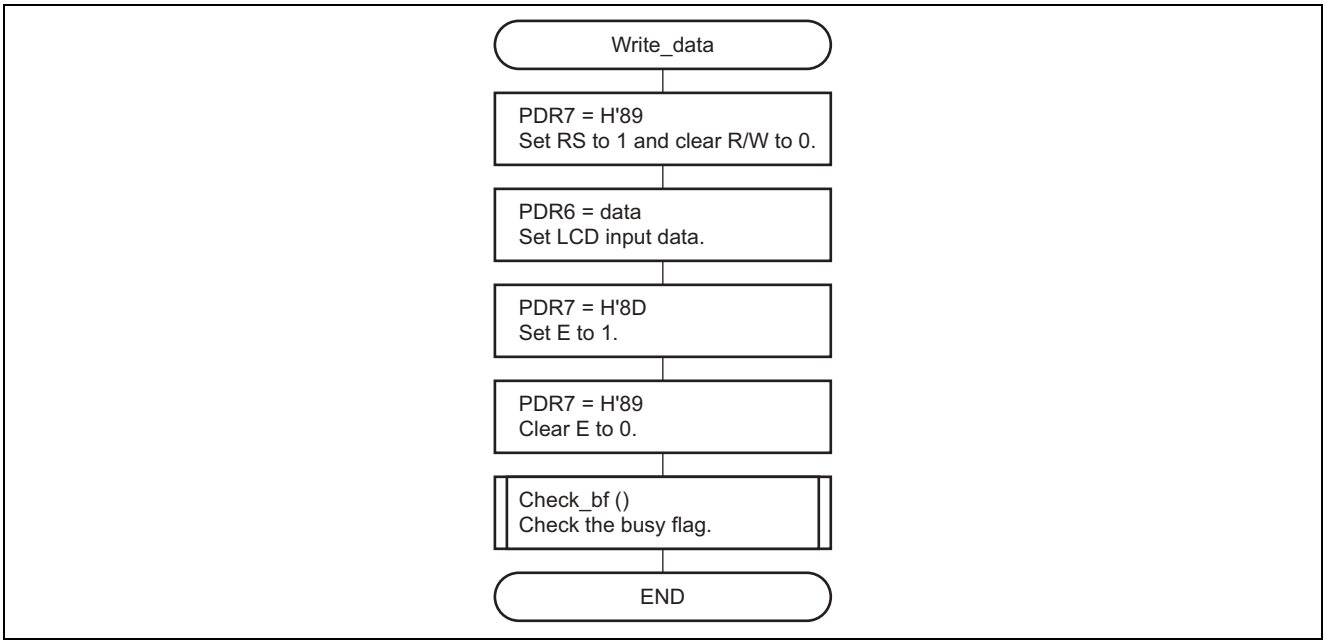
5.2 Check_bf


Check_bf
PCR6 = H'00
Set up port 6 as input port.
PDR7 = H'8A
Clear RS to 0 and set R/W to 1.
PDR7 = H'8E
Set E to 1.
PDR7 = H'8A
Clear E to 0.
busy_f = PDR6 & H'80
Read the busy flag.
busy_f == H'80
During internal operation?
Yes
No
PCR6 = H'FF
Set up port 6 as output port.
END

5.3 Set_up



5.4 Write_data



6. Program Listing

```
/************************************************************************************************/
/*                                                                                              */
/*  H8/300HN Series -H8/3687-                                                                   */
/*  Application Note                                                                            */
/*                                                                                              */
/*  'LCD'                                                                                       */
/*                                                                                              */
/*  External Clock : 16MHz                                                                      */
/*  Internal Clock : 16MHz                                                                      */
/*  Sub Clock      : 32.768kHz                                                                  */
/*                                                                                              */
/************************************************************************************************/

#include        <machine.h>

/************************************************************************************************/
/*  Symbol Definition                                                                           */
/************************************************************************************************/
struct BIT {
    unsigned char   b7:1;             /* bit7 */
    unsigned char   b6:1;             /* bit6 */
    unsigned char   b5:1;             /* bit5 */
    unsigned char   b4:1;             /* bit4 */
    unsigned char   b3:1;             /* bit3 */
    unsigned char   b2:1;             /* bit2 */
    unsigned char   b1:1;             /* bit1 */
    unsigned char   b0:1;             /* bit0 */
};

#define    PCR6       *(volatile unsigned char *)0xFFE9  /* Port Control Register 6            */
#define    PDR6       *(volatile unsigned char *)0xFFD9  /* Port Data Register 6               */
#define    PDR6_BIT   (*(struct BIT *)0cFFD9)            /* Port Data Register 6               */
#define    PCR7       *(volatile unsigned char *)0xFFEA  /* Port Control Register 7            */
#define    PDR7       *(volatile unsigned char *)0xFFDA  /* Port Data Register 7               */
#define    PDR7_BIT   (*(struct BIT *)0cFFDA)            /* Port Data Register 7               */

/************************************************************************************************/
/*  Function Define                                                                             */
/************************************************************************************************/
void       main(void);
void       Check_bf( void );
void       Set_up( unsigned char data );
void       Write_data( unsigned char data );

#pragma section     LCD
const unsigned char initialization[4] ={
    0x38,                                                 /* Function set                     */
    0x0F,                                                 /* Display ON/OFF Control           */
    0x06,                                                 /* Entry Mode Set                   */
    0x80
};

const unsigned char wr_data1[7] ={
    0x48,                                                 /* Data 'H'                         */
    0x38,                                                 /* Data '8'                         */
    0x2F,                                                 /* Data '/'                         */
```

```
    0x33,                                           /* Data '3'                 */
    0x30,                                           /* Data '0'                 */
    0x30,                                           /* Data '0'                 */
    0x48                                            /* Data 'H'                 */
};

const unsigned char wr_data2[5] ={
    0x20,                                           /* Data ' '                 */
    0x33,                                           /* Data '3'                 */
    0x36,                                           /* Data '6'                 */
    0x38,                                           /* Data '8'                 */
    0x37                                            /* Data '7'                 */
};

/************************************************************************************************/
/*  Vector Address                                                                              */
/************************************************************************************************/
#pragma section V1                                  /* Vector address           */
void(*const VEC_TBL1[])(void)={
    main
};

#pragma entry main(sp=0xFF80)
#pragma section
/************************************************************************************************/
/*  Main Program                                                                                */
/************************************************************************************************/
void main(void)                                     /* Main                     */
{
    unsigned char i;

    set_ccr(0x80);                                  /* Interrupt Disable        */

    PCR6 = 0xFF;                                    /* Port6 --> output         */
    PCR7 = 0x07;                                    /* P72, P72, P70 --> output */

    Check_bf();

    for(i=0; i<4; i++)
        Set_up( initialization[i] );                /* The initialization of LCD */

    for(i=0; i<7; i++)
        Write_data( wr_data1[i] );                  /* Indication of the first line */

    Set_up( 0xC0 );                                 /* Move on second line      */

    for(i=0; i<5; i++)
        Write_data( wr_data2[i] );                  /* Indication of the second line */

    while(1);
}
```

```
/*****************************************************************************************************/
/*  Check busy flag                                                                                  */
/*****************************************************************************************************/
void Check_bf( void )
{
    unsigned char busy_f;

    PCR6 = 0x00;                                        /* Port 6 --> input                  */

    do{
        PDR7 = 0x8A;                                    /* RS = 0, R/W = 1                   */
        PDR7 = 0x8E;                                    /* E = 1                             */
        PDR7 = 0x8A;                                    /* E = 0                             */

        busy_f = PDR6 & 0x80;                           /* Busy flag store                   */
    }while(busy_f == 0x80);                             /* During the inside movement        */

    PCR6 = 0xFF;                                        /* Port 6 --> output                 */
}

/*****************************************************************************************************/
/* Set up LCD                                                                                        */
/*****************************************************************************************************/
void Set_up( unsigned char data )
{
    PDR7 = 0x88;                                        /* RS = 0, R/W = 0                   */
    PDR6 = data;
    PDR7 = 0x8C;                                        /* E = 1                             */
    PDR7 = 0x88;                                        /* E = 0                             */

    Check_bf();                                         /* Check busy flag                   */
}

/*****************************************************************************************************/
/* Write data                                                                                        */
/*****************************************************************************************************/
void Write_data( unsigned char data )
{
    PDR7 = 0x89;                                        /* RS = 1, R/W = 0                   */
    PDR6 = data;
    PDR7 = 0x8D;                                        /* E = 1                             */
    PDR7 = 0x89;                                        /* E = 0                             */

    Check_bf();                                         /* Check busy flag                   */
}
```

Link Address Specification

Section Name	Address
CV1	H'0000
P, CLCD	H'0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.28.04	—	First edition issued

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