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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

Example of Reset Synchronous PWM Control Using Timer Z

Introduction

The reset synchronous PWM mode of timer Z is used in producing a PWM waveform in normal and inverse phases.

Target Device

H8/300H Tiny Series H8/36049

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1. Specifications

- The reset synchronous PWM mode of timer Z is used to produce a PWM waveform (normal and inverse phases) output.
- Pins FTI0B0 to FTI0D0 and FTI0A1 to FTI0D1 are set up as PWM output pins by default. TCNT_0 functions as an up-counter.
- By changing the value of GRB_0 on every interrupt generated by a match with GRA_0, the duty cycles of FTI0B0 and FTI0D0 can be changed.
- Buffered operation is not used.
- Output is toggled when TCNT_0 and GRC_0 match.
- TCNT_0 is cleared on a compare-match with GRA_0.
- TCNT_1 is independent of TCNT_0; its output is toggled when it matches GRC_1.
- TCNT_1 is used as a free-running counter.

2. Description of Functions

In this sample task, the reset-synchronous PWM mode of timer Z is used to output a pulse with a controlled duty cycle on the PWM output pin.

- System clock (\(\phi\))
  20-MHz reference clock that operates the CPU and peripheral functions
- Timer Start Register (TSTR)
  Selects operation or stoppage of the TCNT_0 and TCNT_1 counters. In this sample task, both counters are set to count.
- Timer Mode Register (TMDR)
  Selects timer synchronization/independence of counters TCNT_0 and TCNT_1. In this sample task, the two counters are set to operate independently. Normal rather than buffered operation is selected.
- Timer Function Control Register (TFCR)
  Selects settings and output levels for the various operating modes. In this sample task, reset-synchronous PWM mode operation is selected for channels 0 and 1. The initial output level is set to low, and the active level is set to high.
- Timer Output Master Enable Register (TOER)
  Enables/disables outputs on channels 0 and 1. In this sample task, all of the outputs are enabled.
- Timer Output Control Register (TOCR)
  Initial outputs, i.e. the outputs before the first occurrence of a compare-match, are set here. In this sample task, the initial outputs are all set to 0.
- Timer Control Register_0 (TCR_0)
  Selects the input clock and trigger for clearing of TCNT_0. In this sample task, TCNT_0 counts rising edges of \(\phi\) and is cleared on matches with GRA_0.
- Timer Control Register_1 (TCR_1)
  Selects the input clock and trigger for clearing of TCNT_1. In this sample task, TCNT_1 counts rising edges of \(\phi\) and clearing of TCNT_1 is disabled.
- Timer Counter_0 (TCNT_0)
  16-bit readable/writable up-counter which is incremented by cycles of an input internal/external clock signal. In this sample task, TCNT_0 counts rising edges of \(\phi\).
- Timer Counter_1 (TCNT_1)
  16-bit readable/writable up-counter which is incremented by cycles of an input internal/external clock signal. In this sample task, TCNT_1 counts rising edges of \(\phi\).
- General Registers (GRA_0, GRA_1, GRB_0, GRB_1, GRC_0, GRC_1)
  16-bit readable/writable registers, the contents of which are always compared with the counter of TCNT_0.
- Input Capture/Output Compare Pin C0 (FTI0C0)
  Toggled output that synchronizes the PWM cycle period.
- Input Capture/Output Compare Pin B0 (FTI0B0)
  PWM output 1
- Input Capture/Output Compare Pin D0 (FTI0D0)
  PWM output 1 (inverse of PWM output 1)
- Input Capture/Output Compare Pin A1 (FTI0A1)
  PWM output 2
- Input Capture/Output Compare Pin C1 (FTI0C1)
  PWM output 2 (inverse of PWM output 2)
- Input Capture/Output Compare Pin B1 (FTI0B1)
  PWM output 3
- Input Capture/Output Compare Pin D1 (FTI0D1)
  PWM output 3 (inverse of PWM output 3)
- Channel 0 Interrupt (ITMZ0)
  In this sample task, interrupts on matches between TCNT_0 and GRC_0 are used.
- Channel 1 Interrupt (ITMZ1)
  In this sample task, interrupts on matches between TCNT_1 and GRC_1 are used.
- P30 and P31 Terminals of I/O Port (P30, P31)
  Output toggling by GRC_0 interrupts is selected for P30, and output toggling by GRC_1 interrupts is selected for P31.
Figure 1  Block Diagram of Reset-Synchronous PWM Output Using Timer Z
The assignment of functions and operation of reset-synchronous PWM output in this sample task are as described in table 1.

### Table 1 Assignment of Functions

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSTR</td>
<td>Selects operation and stoppage of TCNT_0 and TCNT_1</td>
</tr>
<tr>
<td>TMDR</td>
<td>Sets independent operation of TCNT_0 and TCNT_1</td>
</tr>
<tr>
<td>TFCR</td>
<td>Sets reset-synchronous PWM mode operation for channels 0 and 1</td>
</tr>
<tr>
<td>TOER</td>
<td>Enables all outputs</td>
</tr>
<tr>
<td>TOCR</td>
<td>Sets 0 as the initial value for all outputs</td>
</tr>
<tr>
<td>TCR_0</td>
<td>Selects input clock and trigger for clearing of TCNT_0</td>
</tr>
<tr>
<td>TCR_1</td>
<td>Selects input clock and trigger for clearing of TCNT_1</td>
</tr>
<tr>
<td>TCNT_0</td>
<td>16-bit readable and writable counter that is incremented by cycles of the input clock</td>
</tr>
<tr>
<td>GRA_0</td>
<td>Constantly compared with TCNT_0</td>
</tr>
<tr>
<td>GRA_1</td>
<td>Constantly compared with TCNT_0</td>
</tr>
<tr>
<td>GRB_0</td>
<td>Constantly compared with TCNT_0</td>
</tr>
<tr>
<td>GRB_1</td>
<td>Constantly compared with TCNT_0</td>
</tr>
<tr>
<td>GRC_0</td>
<td>Constantly compared with TCNT_0</td>
</tr>
<tr>
<td>GRC_1</td>
<td>Constantly compared with TCNT_0</td>
</tr>
<tr>
<td>FTIOC0 pin</td>
<td>PWM cycle period in synchronization with the output toggled</td>
</tr>
<tr>
<td>FTIOB0 pin</td>
<td>PWM output 1</td>
</tr>
<tr>
<td>FTIOD0 pin</td>
<td>PWM output 1 (inverse of PWM output 1)</td>
</tr>
<tr>
<td>FTIOA1 pin</td>
<td>PWM output 2</td>
</tr>
<tr>
<td>FTIOC1 pin</td>
<td>PWM output 2 (inverse of PWM output 2)</td>
</tr>
<tr>
<td>FTIOB1 pin</td>
<td>PWM output 3</td>
</tr>
<tr>
<td>FTIOD1 pin</td>
<td>PWM output 3 (inverse of PWM output 3)</td>
</tr>
<tr>
<td>ITMZ0</td>
<td>Channel 0 interrupt generated by matches with GRC_0</td>
</tr>
<tr>
<td>ITMZ1</td>
<td>Channel 1 interrupt generated by matches with GRC_1</td>
</tr>
<tr>
<td>Port 3</td>
<td>Operation as interrupt-toggled outputs</td>
</tr>
</tbody>
</table>
3. Principles of Operation

Figure 2 shows the principles of operation for this task. The figure describes how reset-synchronous PWM output operation is obtained through a combination of hardware and software processing.

Figure 2 Using Timer Z to Produce a Reset-Synchronous PWM Output
4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2  Description of Modules

<table>
<thead>
<tr>
<th>Module</th>
<th>Label Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Selects the compare-match function of Timer Z, starts the counters, and selects the compare-match output pins.</td>
</tr>
<tr>
<td>Timer Z0 interrupt</td>
<td>tmrz0</td>
<td>On interrupts generated by matches with GRC_0: Sets the point where the next Timer Z0 interrupt will be triggered and drives output toggling. On interrupts generated by matches GRA_0: Sets the next interrupt point.</td>
</tr>
<tr>
<td>Timer Z1 interrupt</td>
<td>tmrz1</td>
<td>Sets the point where the next Timer Z1 interrupt will be triggered.</td>
</tr>
</tbody>
</table>

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers

The following describes the internal registers used in this sample task.

- TSTR  Timer Start Register  Address: 0xFFF720

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STR1</td>
<td>0/1</td>
<td>Channel 1 Counter Start 0: TCNT_1 is stopped. 1: TCNT_1 counts.</td>
</tr>
<tr>
<td>0</td>
<td>STR0</td>
<td>0/1</td>
<td>Channel 0 Counter Start 0: TCNT_0 is stopped. 1: TCNT_0 counts.</td>
</tr>
</tbody>
</table>
### Example of Reset Synchronous PWM Control Using Timer Z

#### TMDR Timer Mode Register Address: 0xFFF721

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>BFD1</td>
<td>0</td>
<td>Buffer Operation D1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: GRD_1 operates normally.</td>
</tr>
<tr>
<td>6</td>
<td>BFC1</td>
<td>0</td>
<td>Buffer Operation C1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: GRC_1 operates normally.</td>
</tr>
<tr>
<td>5</td>
<td>BFD0</td>
<td>0</td>
<td>Buffer Operation D0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: GRD_0 operates normally.</td>
</tr>
<tr>
<td>4</td>
<td>BFC0</td>
<td>0</td>
<td>Buffer Operation C0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: GRC_0 operates normally.</td>
</tr>
<tr>
<td>0</td>
<td>SYNC</td>
<td>0</td>
<td>Timer Synchronization</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: TCNT_1 and TCNT_0 operate independently.</td>
</tr>
</tbody>
</table>

#### TFCR Timer Function Control Register Address: 0xFFF723

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>OLS1</td>
<td>1</td>
<td>Output Level Select 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Initial output is low, and the active level is high.</td>
</tr>
<tr>
<td>2</td>
<td>OLS0</td>
<td>1</td>
<td>Output Level Select 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Initial output is low, and the active level is high.</td>
</tr>
<tr>
<td>1</td>
<td>CMD1</td>
<td>CMD1 = 0</td>
<td>Combination Mode 1 and 0</td>
</tr>
<tr>
<td>0</td>
<td>CMD0</td>
<td>CMD0 = 1</td>
<td>CMD1 = 0, CMD0 = 1: Channels 1 and 0 are used together in reset-synchronous PWM mode operation.</td>
</tr>
</tbody>
</table>

#### TOER Timer Output Master Enable Register Address: 0xFFF724

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ED1</td>
<td>0</td>
<td>Master Enable D1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOD1 is enabled.</td>
</tr>
<tr>
<td>6</td>
<td>EC1</td>
<td>0</td>
<td>Master Enable C1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOC1 is enabled.</td>
</tr>
<tr>
<td>5</td>
<td>EB1</td>
<td>0</td>
<td>Master Enable B1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOB1 is enabled.</td>
</tr>
<tr>
<td>4</td>
<td>EA1</td>
<td>0</td>
<td>Master Enable A1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOA1 is enabled.</td>
</tr>
<tr>
<td>3</td>
<td>ED0</td>
<td>0</td>
<td>Master Enable D0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOD0 is enabled.</td>
</tr>
<tr>
<td>2</td>
<td>EC0</td>
<td>0</td>
<td>Master Enable C0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOC0 is enabled.</td>
</tr>
<tr>
<td>1</td>
<td>EB0</td>
<td>0</td>
<td>Master Enable B0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOB0 is enabled.</td>
</tr>
<tr>
<td>0</td>
<td>EA0</td>
<td>0</td>
<td>Master Enable A0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Output on pin FTIOA0 is enabled.</td>
</tr>
</tbody>
</table>
### TOCR Timer Output Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TOD1</td>
<td>0</td>
<td>Output Level Select D1&lt;br&gt;TOD1 = 0: Sets 0 as the initial output of pin FTIOD1.</td>
</tr>
<tr>
<td>6</td>
<td>TOC1</td>
<td>0</td>
<td>Output Level Select C1&lt;br&gt;TOC1 = 0: Sets 0 as the initial output of pin FTIOC1.</td>
</tr>
<tr>
<td>5</td>
<td>TOB1</td>
<td>0</td>
<td>Output Level Select B1&lt;br&gt;TOB1 = 0: Sets 0 as the initial output of pin FTIOB1.</td>
</tr>
<tr>
<td>4</td>
<td>TOA1</td>
<td>0</td>
<td>Output Level Select A1&lt;br&gt;TOA1 = 0: Sets 0 as the initial output of pin FTIOA1.</td>
</tr>
<tr>
<td>3</td>
<td>TOD0</td>
<td>0</td>
<td>Output Level Select D0&lt;br&gt;TOD0 = 0: Sets 0 as the initial output of pin FTIOD0.</td>
</tr>
<tr>
<td>2</td>
<td>TOC0</td>
<td>0</td>
<td>Output Level Select C0&lt;br&gt;TOC0 = 0: Sets 0 as the initial output of pin FTIOC0.</td>
</tr>
<tr>
<td>1</td>
<td>TOB0</td>
<td>0</td>
<td>Output Level Select B0&lt;br&gt;TOB0 = 0: Sets 0 as the initial output of pin FTIOB0.</td>
</tr>
<tr>
<td>0</td>
<td>TOA0</td>
<td>0</td>
<td>Output Level Select A0&lt;br&gt;TOA0 = 0: Sets 0 as the initial output of pin FTIOA0.</td>
</tr>
</tbody>
</table>

### TCR_0 Timer Control Register_0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CCLR2</td>
<td>CCLR2 = 0</td>
<td>Counter Clear 2 to 0</td>
</tr>
<tr>
<td>6</td>
<td>CCLR1</td>
<td>CCLR1 = 0</td>
<td>CCLR2 = 0, CCLR1 = 0, CCLR0 = 1:</td>
</tr>
<tr>
<td>5</td>
<td>CCLR0</td>
<td>CCLR0 = 1</td>
<td>Clears TCNT0 on compare-matches with GRA0.</td>
</tr>
<tr>
<td>4</td>
<td>CKEG1</td>
<td>CKEG1 = 0</td>
<td>Clock Edge 1 to 0</td>
</tr>
<tr>
<td>3</td>
<td>CKEG0</td>
<td>CKEG0 = 0</td>
<td>CKEG1 = 0, CKEG0 = 0: Rising edges are counted.</td>
</tr>
<tr>
<td>2</td>
<td>TPSC2</td>
<td>TPSC2 = 0</td>
<td>Timer Prescaler 2 to 0</td>
</tr>
<tr>
<td>1</td>
<td>TPSC1</td>
<td>TPSC1 = 0</td>
<td>TPSC2 = 0, TPSC1 = 0, TPSC0 = 0:</td>
</tr>
<tr>
<td>0</td>
<td>TPSC0</td>
<td>TPSC0 = 0</td>
<td>Counting is driven by φ.</td>
</tr>
</tbody>
</table>

### TCR_1 Timer Control Register_1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CCLR2</td>
<td>CCLR2 = 0</td>
<td>Counter Clear 2 to 0</td>
</tr>
<tr>
<td>6</td>
<td>CCLR1</td>
<td>CCLR1 = 0</td>
<td>CCLR2 = 0, CCLR1 = 0, CCLR0 = 0:</td>
</tr>
<tr>
<td>5</td>
<td>CCLR0</td>
<td>CCLR0 = 1</td>
<td>Disable Clearing TCNT1.</td>
</tr>
<tr>
<td>4</td>
<td>CKEG1</td>
<td>CKEG1 = 0</td>
<td>Clock Edge 1 to 0</td>
</tr>
<tr>
<td>3</td>
<td>CKEG0</td>
<td>CKEG0 = 0</td>
<td>CKEG1 = 0, CKEG0 = 0: Rising edges are counted.</td>
</tr>
<tr>
<td>2</td>
<td>TPSC2</td>
<td>TPSC2 = 0</td>
<td>Timer Prescaler 2 to 0</td>
</tr>
<tr>
<td>1</td>
<td>TPSC1</td>
<td>TPSC1 = 0</td>
<td>TPSC2 = 0, TPSC1 = 0, TPSC0 = 0:</td>
</tr>
<tr>
<td>0</td>
<td>TPSC0</td>
<td>TPSC0 = 0</td>
<td>Counting is driven by φ.</td>
</tr>
</tbody>
</table>
Example of Reset Synchronous PWM Control Using Timer Z

- TCNT_0 Timer Counter _0 Address: 0xFFF706
  Function: 16-bit up-counter that counts rising edges of φ.
  Set value: 0
- TCNT_1 Timer Counter _1 Address: 0xFFF716
  Function: 16-bit up-counter that counts rising edges of φ.
  Set value: 0
- GRA_0 General Register A _0 Address: 0xFFF708
  Function: When the value set in GRA_0 matches the value counted by TCNT_0, a compare-match occurs.
  Set value: 12000
- GRA_1 General Register A _1 Address: 0xFFF718
  Function: When the value set in GRA_1 matches the value counted by TCNT_0, a compare-match occurs.
  Set value: 4000
- GRB_0 General Register B _0 Address: 0xFFF70A
  Function: When the value set in GRB_0 matches the value counted by TCNT_0, a compare-match occurs.
  Set value: Sets one data in GRB_DATA alignment at every GRA_0 interrupt
  (In this sample task, four data are repeatedly set.)
- GRB_1 General Register B _1 Address: 0xFFF71A
  Function: When the value set in GRB_1 matches the value counted by TCNT_0, a compare-match occurs.
  Set value: 2000
- GRC_0 General Register C _0 Address: 0xFFF70C
  Function: When the value set in GRC_0 matches the value counted by TCNT_0, a compare-match occurs.
  Set value: 2800
- GRC_1 General Register C _1 Address: 0xFFF71C
  Function: When the value set in GRC_1 matches the value counted by TCNT_1, a compare-match occurs.
  Set value: 20000
### 4.4 RAM Usage

Table 3 describes the RAM usage in this sample task.

**Table 3 Description of RAM Used**

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function</th>
<th>Address</th>
<th>Label Name of Module Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSR_SV</td>
<td>Saves the value of TSR_0</td>
<td>H'FFE812</td>
<td>tmrz0</td>
</tr>
<tr>
<td>GRB_count</td>
<td>Index counter for data to be placed in GRB_0</td>
<td>H'FFE800</td>
<td>main, tmrz0</td>
</tr>
<tr>
<td>GRA0_BUF</td>
<td>Saves the initially set data for GRA_0</td>
<td>H'FFE802</td>
<td>main, tmrz0</td>
</tr>
<tr>
<td>GRC0_BUF</td>
<td>Holds the data for output driven by matches with GRC_0</td>
<td>H'FFE806</td>
<td>main, tmrz0</td>
</tr>
<tr>
<td>GRC1_BUF</td>
<td>Saves the data for output driven by matches with GRC_1</td>
<td>H'FFE80A</td>
<td>main, tmrz1</td>
</tr>
<tr>
<td>GRC0_SW</td>
<td>Switch for toggling output driven by GRC_0</td>
<td>H'FFE80E</td>
<td>main, tmrz0</td>
</tr>
<tr>
<td>GRC1_SW</td>
<td>Switch for toggling output driven by GRC_1</td>
<td>H'FFE810</td>
<td>main, tmrz1</td>
</tr>
</tbody>
</table>
5. Flowcharts

5.1 Main Routine (main)

```
main

  *1 Mask interrupt requests by setting the CCR's interrupt mask bit (I) to 1.

  CCR I bit 1

  GRC0_SW 0
  Initialize the output switch for GRC_0.

  GRC1_SW 0
  Initialize the output switch for GRC_1.

  PCR3 H'03
  Initial setting of port 3
  P30: P30 output pin (output data = 0)
  P31: P31 output pin (output data = 0)

  TSTR 0
  Stop the timer Z.

  TCR_0 H'20
  Internal clock (count cycles of φ)
  Clear TCNT.

  TCR_1 H'00
  Internal clock (count cycles of φ)
  Disable clearing of TCNT.

  TFCR H'0D
  Initial setting of the timer function control register
  Operate in the reset-synchronous PWM mode.
  Initial output level is low, and active level is high.

  TOCR 0
  Output 0 as the initial output, i.e. until the first compare match.

  TCNT_0 0
  Initialize timer counter 0.

  TCNT_1 0
  Initialize timer counter 1.

Note *1: In this sample task, the stack pointer is set by INT.SRC (assembly language)
```
Example of Reset Synchronous PWM Control Using Timer Z

1. **GRA_0** ← SET_A0
   - Set the cycle period of GRA_0.

2. **GRA0_BUF** ← SET_A0
   - Save the cycle period of GRA_0.

3. **GRA_1** ← SET_A1
   - Set the cycle period of GRA_1.

4. **GRB_count** ← 0
   - Initialize the GRB data table counter.

5. **GRB_0** ← GRB_DATA [GRB_count]
   - Set the cycle period of GRB_0.

6. **GRB_1** ← SET_B1
   - Set the cycle period of GRB_1.

7. **GRC_0** ← SET_C0
   - Set the cycle period of GRC_0.

8. **GRC0_BUF** ← SET_C0
   - Save the cycle period of GRC_0.

9. **TIER_0** ← H'05
   - Enable interrupts on matches with GRA_0 and GRC_0.
TOER ← 0

Enable output on all pins for channels 0 and 1.

GRC_1 ← SET_C1

Set the cycle period of GRC_1.

GRC1_BUF ← SET_C1

Save the cycle period of GRC_1.

TIER_1 ← H'04

Enable interrupts on matches with GRC_1.

TSTR ← H'03

Start counting by both TCNT0 and TCNT1.

CCR I bit ← 0

Clear the interrupt mask bit (I) of the CCR.
5.2 Timer Z0 Interrupt Processing Routine (tmrz0)

```
 tmrz0

 TSR_SV <- TSR_0                  Save status.

 No

 TSR_SV & IMFC?                   Is GRC_0 the source of the interrupt request?

 Yes

 GRC0_BUF <- GRC0_BUF + SET_C0    Obtain the next interrupt point.

 GRC0_BUF > GRA0_BUF?             Next interrupt point > GRA_0 cycle period?

 No

 GRC0_BUF <- GRC0_BUF - GRA0_BUF  Subtract GRA_0 cycle period from the next interrupt point.

 GRC_0 <- GRC0_BUF                Set the next interrupt point.

 Invert GRC0_SW bit               Turn the internal switch on/off.

 GRC0_OUT <- GRC0_SW              Output.

 No

 TSR_SV & IMFA?                   Is GRA_0 the source of the interrupt request?

 Yes

 GRB_count < GRB_MAX - 1?         Is GRB_count within the size of GRB table?

 No

 GRB_count -> GRB_count + 1       Set GRB_count to the next index in GRB table.

 Yes

 GRB_0 <- GRB_DATA[GRB_count]     Set the next interrupt point.

 TSR_0 <- 0                      Initialize the status.

 rti
```
5.3 Timer Z1 Interrupt Processing Routine (tmrz1)

```
1. **tmrz1**

2. **TSR_1 & IMFC?**
   - Yes: Obtain the next interrupt point.
     - **GRC1_BUF**
     - **GRC1_BUF + SET_C1**
   - No: Next interrupt point > Maximum value?
     - Yes: Subtract maximum value from the next interrupt point.
       - **GRC1_BUF**
       - **GRC1_BUF - MAX_INT**
     - No: Is GRC_1 the source of the interrupt request?
       - Yes: **GRC1_BUF**
       - **GRC1_BUF + SET_C1**
       - No: Set the next interrupt point.
         - **GRC_1**
         - **GRC1_BUF**

3. Invert GRC1_SW bit

4. Output.

5. Initialize the status.

6. **TSR_1**

7. **rte**
```
6. Program Listing

INIT.SRC (Program listing)

```assembly
.export _INIT
.import _main
;
.section P,CODE
_INIT:
    mov.l #h'fff000,sp
    ldc.b #b'10000000,ccr
    jmp&_main
;
.end
```

/* H8/300H Tiny Series -H8/36049- Application Note */
/* Application Version */
/* Usage Example of Internal Timer Z */

#include <machine.h>

/* Symbol definitions */
struct BIT {
    unsigned char b7:1;        /* bit 7 */
    unsigned char b6:1;        /* bit 6 */
    unsigned char b5:1;        /* bit 5 */
    unsigned char b4:1;        /* bit 4 */
    unsigned char b3:1;        /* bit 3 */
    unsigned char b2:1;        /* bit 2 */
    unsigned char b1:1;        /* bit 1 */
    unsigned char b0:1;        /* bit 0 */
};

#define PDR3      *(volatile unsigned char *)0xFFFFD6        /* Port Data Register 3 */
#define PDR3_BIT  (*(struct BIT *)0xFFFFD6)                   /* Port Data Register 3 */
#define GRC0_OUT  PDR3_BIT.b0
/* Output it by interrupt from GRC0 */
#define GRC1_OUT  PDR3_BIT.b1
/* Output it by interrupt from GRC1 */
#define PCR3      *(volatile unsigned char *)0xFFFFE6     /* Port Control Register 3 */
/* COMMON */
#define TSTR    *(volatile unsigned char *)0xFFF720          /* Timer Start Register */
#define TMDR    *(volatile unsigned char *)0xFFF721           /* Timer Mode Register */
#define TPMR    *(volatile unsigned char *)0xFFF722       /* Timer PWM Mode Register */
#define TFCR    *(volatile unsigned char *)0xFFF723
/* Timer Function Control Register */
#define TOER    *(volatile unsigned char *)0xFFF724
/* Timer Output Master Enable Register */
#define TOCR    *(volatile unsigned char *)0xFFF725
```
/* Timer Output Control Register */

#define TCR_0 *(volatile unsigned char *)0xFFF700 /* CHANNEL 0 */
#define TIORA_0 *(volatile unsigned char *)0xFFF701 /* Timer Control Register_0 */
#define TIORC_0 *(volatile unsigned char *)0xFFF702 /* Timer I/O Control RegisterA_0 */
#define TSR_0 *(volatile unsigned char *)0xFFF703 /* Timer Status Register_0 */
#define TIER_0 *(volatile unsigned char *)0xFFF704 /* Timer Interrupt Enable Register_0 */
#define POCR_0 *(volatile unsigned char *)0xFFF705 /* PWM Mode Output Level Control Register_0 */
#define TCNT_0 *(volatile unsigned int *)0xFFF706 /* Timer Counter_0 */
#define GRA_0 *(volatile unsigned int *)0xFFF708 /* General Register A_0 */
#define GRB_0 *(volatile unsigned int *)0xFFF70A /* General Register B_0 */
#define GRC_0 *(volatile unsigned int *)0xFFF70C /* General Register C_0 */
#define GRD_0 *(volatile unsigned int *)0xFFF70E /* General Register D_0 */

/* CHANNEL 1 */

#define TCR_1 *(volatile unsigned char *)0xFFF710 /* Timer Control Register_1 */
#define TIORA_1 *(volatile unsigned char *)0xFFF711 /* Timer I/O Control RegisterA_1 */
#define TIORC_1 *(volatile unsigned char *)0xFFF712 /* Timer I/O Control RegisterC_1 */
#define TSR_1 *(volatile unsigned char *)0xFFF713 /* Timer Status Register_1 */
#define TIER_1 *(volatile unsigned char *)0xFFF714 /* Timer Interrupt Enable Register_1 */
#define POCR_1 *(volatile unsigned char *)0xFFF715 /* PWM Mode Output Level Control Register_1 */
#define TCNT_1 *(volatile unsigned int *)0xFFF716 /* Timer Counter_1 */
#define GRA_1 *(volatile unsigned int *)0xFFF718 /* General Register A_1 */
#define GRB_1 *(volatile unsigned int *)0xFFF71A /* General Register B_1 */
#define GRC_1 *(volatile unsigned int *)0xFFF71C /* General Register C_1 */
#define GRD_1 *(volatile unsigned int *)0xFFF71E /* General Register D_1 */

#define IMFA 0x01 /* bit position of IMFA */
#define IMFC 0x04 /* bit position of IMFC */
#define GRB_MAX 4 /* GRB table size */
#define SET_A0 12000 /* setting value for GRA_0 */
#define SET_A1 4000 /* setting value for GRA_1 */
#define SET_B1 2000 /* setting value for GRB_1 */
#define SET_C0 2800 /* setting value for GRC_0 */
#define SET_C1 20000 /* setting value for GRC_1 */
#define MAX_INT 65535 /* integer max value */

#pragma interrupt (tmrz0)
#pragma interrupt (tmrz1)
/* function definition */
extern void INIT(void);                                         /* Stack pointer set */

void main(void);                                                     /* main routine */
void tmrz0(void);                                                     /* Timer Z0 interrupt routine */
void tmrz1(void);                                                     /* Timer Z1 interrupt routine */

/* Data table */
const unsigned int GRB_DATA[GRB_MAX] =                                  /* GRB table */
{  
    7000,
    3000,
    9000,
    5000
};

/* RAM definition */
unsigned char TSR_SV;                                                    /* Save TSR */
int GRB_count;                                                        /* GRB counter */
unsigned long GRA0_BUF;                                          /* Buffer for GRA_0 */
unsigned long GRC0_BUF;                                          /* Buffer for GRC_0 */
unsigned long GRC1_BUF;                                          /* Buffer for GRC_1 */
int GRC0_SW;                                             /* Inverse switch for GRC_0 */
int GRC1_SW;                                             /* Inverse switch for GRC_1 */

/* Vector address */
#pragma section V1                                             /* Vector section set */
void (*const VEC_TBL1[])(void) = {
    INIT                                                      /* H'0000 Reset vector */
};

#pragma section V2                                             /* Vector section set */
void (*const VEC_TBL2[])(void) = {
    tmrz0
    /* H'0068 Timer Z0 interrupt vector */
};

#pragma section V3                                             /* Vector section set */
void (*const VEC_TBL3[])(void) = {
    tmrz1
    /* H'006C Timer Z1 interrupt vector */
};

#pragma section                                                                 /* P */

 PHX*********************************************************************
PHX Main program                                                 */
 PHX*********************************************************************

void main(void)
{
    set_imask_ccr(1);                                               /* CCR I-bit = 1 */
    GRC0_SW = 0;                                          /* initialize GRC_0 switch */
GRC1_SW = 0;          /* initialize GRC_1 switch */
PCR3 = 0x03;          /* initialize Port 3 */
TSTR = 0;            /* stop timer */
TCR_0 = 0x20;        /* select Internal clock(φ), Clears TCNT by GRA */
TCR_1 = 0x00;        /* select Internal clock(φ), Disables TCNT clearing */
TFCR = 0x0D;         /* operate in reset synchronous PWM mode */
                        /* initial output is low */
TOCR = 0;            /* selects the initial outputs */
TCNT_0 = 0;          /* clear timer counter */
TCNT_1 = 0;          /* clear timer counter */
GRA_0 = SET_A0;      /* set period */
GRA0_BUF = SET_A0;   /* keep period */
GRA_1 = SET_A1;      /* set period */
GRB_count = 0;       /* init counter */
GRB_0 = GRB_DATA[GRB_count]; /* set period */
GRB_1 = SET_B1;      /* set period */
GRC_0 = SET_C0;      /* set period */
GRC0_BUF = SET_C0;   /* keep period */
TIER_0 = 0x05;       /* enable GRA_0,GRC_0 interrupt */
TOER = 0;            /* enable output */
GRC_1 = SET_C1;      /* set period */
GRC1_BUF = SET_C1;   /* keep period */
TIER_1 = 0x04;       /* enable GRC_1 interrupt */
TSTR = 0x03;         /* start timer */
set_imask_ccr(0);    /* CCR I-bit = 0 */
                        
while(1);
}

/***********************************************************/
/* Timer Z0 Interrupt */
/***********************************************************/
void tmrz0(void)
{
    TSR_SV = TSR_0;       /* save status */
                        
    /* interrupt by GRC_0 */
    if(TSR_SV & IMFC) {

}}
Example of Reset Synchronous PWM Control Using Timer Z

```c
GRC0_BUF += SET_C0; /* get next period */
if(GRC0_BUF > GRA0_BUF) {
    GRC0_BUF -= GRA0_BUF;
}
GRC_0 = GRC0_BUF; /* set next period */

GRC0_SW ^= 1; /* reverse switch */
GRC0_OUT = GRC0_SW; /* output signal */
}

/* interrupt by GRA_0 */
if(TSR_SV & IMFA) {
    if(GRB_count < (GRB_MAX - 1)) /* get next index */
        GRB_count++;
    else
        GRB_count = 0;
    GRB_0 = GRB_DATA[GRB_count]; /* set next period from table */
}
TSR_0 = 0; /* clear status */
}

/* Timer Z1 Interrupt */
void tmrz1(void)
{

    /* interrupt by GRC_1 */
    if(TSR_1 & IMFC) {
        GRC1_BUF += SET_C1; /* get next period */
        if(GRC1_BUF > MAX_INT) {
            GRC1_BUF -= MAX_INT;
        }
        GRC_1 = GRC1_BUF; /* set next period */

        GRC1_SW ^= 1; /* reverse switch */
        GRC1_OUT = GRC1_SW; /* output signal */
    }
    TSR_1 = 0; /* clear status */
}
```
## Revision Record

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Example of Reset Synchronous PWM Control Using Timer Z

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