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April 1st, 2010
Renesas Electronics Corporation

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Introduction
The input capture function of the 16-bit timer pulse unit (TPU) is used to measure the time (cycle) from the rising edge of a pulse input from an input capture input pin (TIOCA1) to the next rising edge.

Target Device
H8/38076R

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2. Functions Used ......................................................................................................... 2
3. Principles of Operation ............................................................................................ 5
4. Description of Software ........................................................................................ 6
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1. **Specifications**

- The input capture function of the 16-bit timer pulse unit (TPU) is used to measure the cycle of a pulse input from an input capture input pin (TIOCA1).
- In this sample task, internal clock $\phi/256$ is set as the timer counter _1 (TCNT _1) input clock. At $\phi = 10$ MHz operation, the resolution is $25.6 \, \mu$s and the measurable cycle is $1.67 \, \text{s}$. The TCNT _1 count value from the rising edge of a TIOCA1 input pulse to the next rising edge is stored in RAM.
- An example of pulse cycle measurement by means of the input capture function is shown in figure 1.

![Figure 1: Example of Pulse Cycle Measurement Using TPU Input Capture Function](image)

2. **Functions Used**

2.1 **TPU Input Capture Function**

In this sample task, the input capture function of the TPU is used to measure the cycle of a pulse input to an input capture input pin (TIOCA1). A block diagram of the input capture function of the TPU is shown in figure 2. The block diagram of the input capture function of the TPU is explained below.

- Timer control register _1 (TCR _1)
  Selects timer counter _1 (TCNT _1) counter clearing source, the input clock edge, and the clock source.
- Timer mode register _1 (TMDR _1)
  Sets the operating mode of channel 1.
- Timer I/O control register _1 (TIOR _1)
  Controls timer general register A _1 (TGRA _1).
- Timer interrupt enable register _1 (TIER _1)
  Enables or disables TPU _1 interrupt requests.
- Timer status register _1 (TSR _1)
  Indicates the state of TPU _1.
- Timer counter _1 (TCNT _1)
  A 16-bit readable/writable counter that counts using the rising edge of internal clock $\phi/256$
- Timer general register A _1 (TGRA _1)
  A 16-bit readable/writable input capture register
• Timer start register (TSTR)
  Controls operation/stopping of timer counter_1 (TCNT_1).

• An example of input capture input cycle calculation is shown below. (In this sample task, the TCNT_1 count value is stored in RAM.)
  \[(\phi = 10 \text{ MHz}, \text{TCNT}_1 \text{ input clock} = \phi/256)\]
  \[\text{TIOCA1 pin input pulse cycle} = \text{TCNT}_1 \text{ count value} \times \text{TCNT}_1 \text{ input clock cycle}\]
  \[= \text{TCNT}_1 \text{ count value} \times 25.6 \mu\text{s}\]

---

**Figure 2** Block Diagram of TPU Input Capture Function
2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, the cycle of a pulse input from an input capture input pin (TIOCA1) is measured by means of the TPU input capture function.

### Table 1 Assignment of Functions

<table>
<thead>
<tr>
<th>Elements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCR_1</td>
<td>Sets TGRA_1 compare match as TCNT_1 counter clearing source, rising edge as input clock edge, and internal clock $\phi/256$ as clock source</td>
</tr>
<tr>
<td>TMDR_1</td>
<td>Sets normal operation mode as TPU channel 1 operating mode</td>
</tr>
<tr>
<td>TIOR_1</td>
<td>Sets input capture register as TGRA_1 function, and input capture at the rising edge as TIOCA1 pin function</td>
</tr>
<tr>
<td>TIER_1</td>
<td>Enables TCFV and TGFA interrupts</td>
</tr>
<tr>
<td>TSR_1</td>
<td>TCFV, TGFA interrupt request flags</td>
</tr>
<tr>
<td>TCNT_1</td>
<td>16-bit counter using internal clock $\phi/256$ as clock source</td>
</tr>
<tr>
<td>TGRA_1</td>
<td>16-bit input capture register</td>
</tr>
<tr>
<td>TSTR</td>
<td>Sets TCNT_1 count operation</td>
</tr>
<tr>
<td>TIOCA1</td>
<td>TGRA_1 input capture input pin</td>
</tr>
</tbody>
</table>
3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, pulse cycles are measured using the input capture function of the TPU.

![Figure 3 Principles of Operation](image-url)
4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>TPU initial settings, TCNT_1 count operation start, interrupt enabling, storing TCNT_1 value in RAM at end of measurement, end processing</td>
</tr>
<tr>
<td>int_tgi1a</td>
<td>TGRA_1 input capture A interrupt processing, measurement starting point/end point identification</td>
</tr>
<tr>
<td>int_tci1v</td>
<td>TCNT_1 overflow interrupt processing</td>
</tr>
</tbody>
</table>

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- **TSTR**  Timer start register  Address: H'F030

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1   | CST1     | 1         | R/W | Counter start 1  
Selects TCNT_1 operation or stopping.  
CST1 = 1: TCNT_1 performs count operation |

- **TCR_1**  Timer control register_1  Address: H'F040

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>CCLR1</td>
<td>0</td>
<td>R/W</td>
<td>Counter clear 1, 0</td>
</tr>
</tbody>
</table>
| 5   | CCLR0    | 1         | R/W | Select the TCNT_1 counter clearing source.  
CCLR1 = 0, CCLR0 = 1: TCNT_1 cleared by TGRA_1 input capture |
| 4   | CKEG1    | 0         | R/W | Clock edge 1, 0 |
| 3   | CKEG0    | 0         | R/W | Select the TCNT_1 input clock edge.  
CKEG1 = 0, CKEG0 = 0: Counts at the rising edge |
| 2   | TPSC2    | 1         | R/W | Timer prescaler 2, 1, 0 |
| 1   | TPSC1    | 1         | R/W | Select the TCNT_1 clock source. |
| 0   | TPSC0    | 0         | R/W | TPSC2 = 1, TPSC1 = 1, TPSC0 = 0: Counts on internal clock φ/256 |
- **TMDR_1** Timer mode register_1  
  Address: H'F041

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MD1</td>
<td>0</td>
<td>R/W</td>
<td>Mode 1, 0</td>
</tr>
<tr>
<td>0</td>
<td>MD0</td>
<td>0</td>
<td>R/W</td>
<td>Select the TPU_1 operating mode. MD1 = 0, MD0 = 0: TPU_1 set to normal operation mode</td>
</tr>
</tbody>
</table>

- **TIOR_1** Timer I/O control register_1  
  Address: H'F042

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>IOA3</td>
<td>1</td>
<td>R/W</td>
<td>I/O control A3 to A0</td>
</tr>
<tr>
<td>2</td>
<td>IOA2</td>
<td>0</td>
<td>R/W</td>
<td>Select the function of TGRA_1. IOA3 = 1, IOA2 = 0, IOA1 = 0, IOA0 = 0: TGRA_1 function is input capture register, TIOCA1 pin function is input capture at the rising edge</td>
</tr>
<tr>
<td>1</td>
<td>IOA1</td>
<td>0</td>
<td>R/W</td>
<td>IOA3 = 1, IOA2 = 0, IOA1 = 0, IOA0 = 0: TGRA_1 function is input capture register, TIOCA1 pin function is input capture at the rising edge</td>
</tr>
<tr>
<td>0</td>
<td>IOA0</td>
<td>0</td>
<td>R/W</td>
<td>IOA3 = 1, IOA2 = 0, IOA1 = 0, IOA0 = 0: TGRA_1 function is input capture register, TIOCA1 pin function is input capture at the rising edge</td>
</tr>
</tbody>
</table>

- **TIER_1** Timer interrupt enable register_1  
  Address: H'F044

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>TCIEV</td>
<td>1</td>
<td>R/W</td>
<td>Overflow interrupt enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Enables or disables TCFV flag interrupt request (TCI1V) when TCFV flag is set to 1 in TSR_1. TCIEV = 1: TCFV flag interrupt request (TCI1V) enabled</td>
</tr>
<tr>
<td>0</td>
<td>TGIEA</td>
<td>1</td>
<td>R/W</td>
<td>TGR interrupt enable A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Enables or disables TGFA flag interrupt request (TGI1A) when TGFA flag is set to 1 in TSR. TGIEA = 1: TGFA flag interrupt request (TGI1A) enabled</td>
</tr>
</tbody>
</table>
### TSR_1  Timer status register_1  Address: H'F045

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 4   | TCFV      | 0         | R/(W)* | Overflow flag  
    |           |           |      | Status flag indicating occurrence of TCNT_1 overflow  
    |           |           |      | [Setting condition]  
    |           |           |      | When TCNT_1 value overflows (H'FFFF → H'0000)  
    |           |           |      | [Clearing condition]  
    |           |           |      | When 0 is written to TCFV after TCFV is read while set to 1 |
| 0   | TGFA      | 0         | R/(W)* | Input capture/output compare flag A  
    |           |           |      | Status flag indicating occurrence of TGRA_1 input capture or compare match  
    |           |           |      | [Setting conditions]  
    |           |           |      | • When TCNT_1 = TGRA_1 while TGRA_1 is functioning as output compare register  
    |           |           |      | • When TCNT_1 value is transferred to TGRA_1 in response to input capture signal when TGRA_1 is functioning as input capture register  
    |           |           |      | [Clearing condition]  
    |           |           |      | • When 0 is written to TGFA after TGFA is read while set to 1 |

Note: * Only 0 can be written to clear the flag.

### TCNT_1  Timer counter_1  Address: H'F046

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15  | Bit 15   | 0         | R/W | Timer counter_1  
| 14  | Bit 14   | 0         | R/W | 16-bit readable/writable counter. TCNT_1 is initialized to H'0000 at a reset. TCNT_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.  
| 13  | Bit 13   | 0         | R/W |  
| 12  | Bit 12   | 0         | R/W |  
| 11  | Bit 11   | 0         | R/W |  
| 10  | Bit 10   | 0         | R/W |  
| 9   | Bit 9    | 0         | R/W |  
| 8   | Bit 8    | 0         | R/W |  
| 7   | Bit 7    | 0         | R/W |  
| 6   | Bit 6    | 0         | R/W |  
| 5   | Bit 5    | 0         | R/W |  
| 4   | Bit 4    | 0         | R/W |  
| 3   | Bit 3    | 0         | R/W |  
| 2   | Bit 2    | 0         | R/W |  
| 1   | Bit 1    | 0         | R/W |  
| 0   | Bit 0    | 0         | R/W |  

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4.4 Constants Used

No constants are used in this sample task.

4.5 RAM Usage

Table 3 describes RAM usage in this sample task.

### Table 3  RAM Usage

<table>
<thead>
<tr>
<th>Label</th>
<th>Description</th>
<th>Amount of Memory Used</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>period</td>
<td>Stores TCNT_1 value from rising edge of TIOCA1 pin input pulse to next rising edge.</td>
<td>1 word</td>
<td>main</td>
</tr>
<tr>
<td>flag</td>
<td>endf Flag indicating end of measurement</td>
<td>1 bit</td>
<td>main, int_tgi1a</td>
</tr>
<tr>
<td></td>
<td>strf Flag indicating start of measurement</td>
<td>1 bit</td>
<td>int_tci1v</td>
</tr>
<tr>
<td></td>
<td>errf Flag indicating that TCNT_1 has overflowed</td>
<td>1 bit</td>
<td>main, int_tci1v</td>
</tr>
</tbody>
</table>
5. Flowcharts

5.1 main

```
SP = H'FF80  ----------------- Initialize stack pointer
set_ccr(H'80)  ----------------- CCR I-bit = 1 (interrupts disabled)
period = H'0000  ----------------- Initialize RAM area used
flag = H'00
TCR_1 = H'26
TMDR_1 = H'C0
TIOR_1 = H'08
TCNT_1 = H'0000
TCFV, TGFA = 0  ----------------- Enable TGI1A and TCI1V interrupts
TCIEV, TGIEA = 1
TSTR = H'02  ----------------- Set CST1 to 1 and start TCNT_1 counter
set_imask_ccr(0)  ----------------- CCR I-bit = 0 (interrupts enabled)

endf?

= 0

= 1

period = TGRA_1

errf?

= 0

= 1

TSTR = H'00  ----------------- Store TCNT_1 count value
TIER_1 = H'40

TSTR = H'00  ----------------- End processing
TIER_1 = H'40

Normal termination

Error termination
```

TPU_1 initialization
- TCNT_1 counter clearing source: TGRA_1 input capture
- TCNT_1 input clock edge: Rising edge
- TCNT_1 input clock: Internal clock φ/256
- TPU_1 operating mode: Normal operation
- TGRA_1 function: Input capture register
- TIOCA1 pin function: Input capture at the rising edge
5.2 int_tgi1a

- TGFA = 0
- strf?
  - strf = 1
- endf = 1

5.3 int_tci1v

- TCFV = 0
- strf?
  - strf = 1
- errf = 1

- Link Address Specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'0000</td>
</tr>
<tr>
<td>CV2</td>
<td>H'003A</td>
</tr>
<tr>
<td>CV3</td>
<td>H'003E</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
<tr>
<td>B</td>
<td>H'F780</td>
</tr>
</tbody>
</table>
Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
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<tr>
<td>1.00</td>
<td>Sep.16.04</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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