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April 1st, 2010
Renesas Electronics Corporation

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H8/300H SLP Series

Multiple Interrupt Operation Using Interrupt Priority Function

Introduction

The interrupt priority function is used to generate TPU compare match interrupt processing during IRQ0 interrupt processing.

Target Device

H8/38076R

Contents

1. Specifications

1. An LED connected to P93 of port 9 is made to blink at 0.05 second intervals by means of compare match interrupt processing using the cycle counting function of the TPU.
2. An IRQ0 interrupt is generated by the on-state of switch input connected to the $\overline{\text{IRQ0}}$ pin, and within the interrupt processing function priority level 0 interrupt requests are masked and multiple interrupts are enabled. In this sample task, the IRQ0 interrupt processing period is set to one second or more.
3. Normally, a TPU interrupt has a priority level of 0, and therefore a TPU interrupt is not generated during IRQ0 interrupt processing, and LED blinking is suspended for approximately one second until IRQ0 interrupt processing ends. (This applies when PB1 of port B is 1.)
4. When PB1 of port B is 0, on the other hand, the interrupt level of the TPU is set to 1 using the interrupt priority function.
5. In this case, the TPU interrupt priority level is higher than the mask level, and therefore multiple interrupts are generated and LED blinking can be performed at 0.05 second intervals.
6. A sample connection diagram is shown in figure 1.

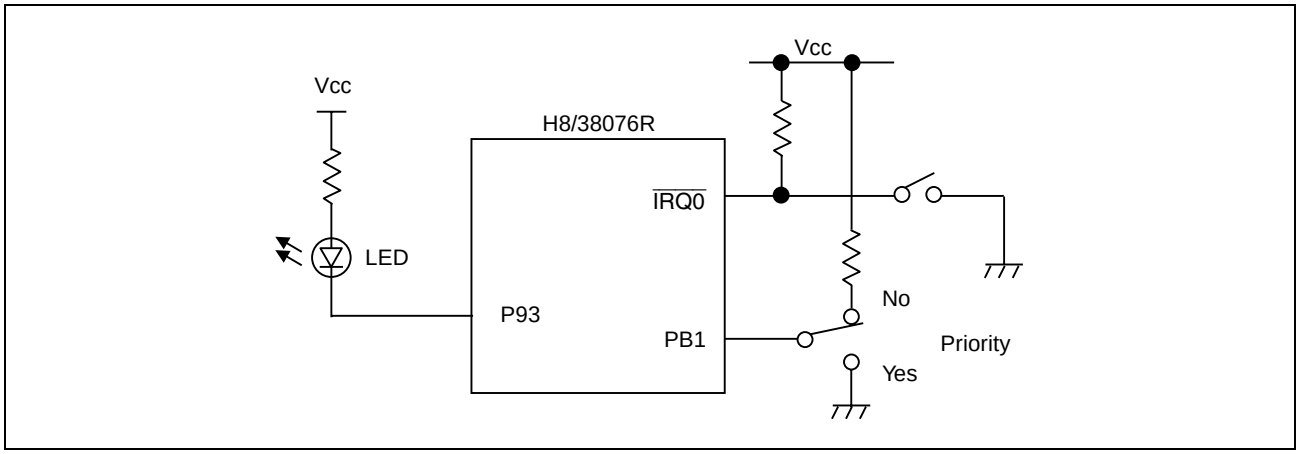


Figure 1 Example of Connections for This Sample Task

2. Functions Used

2.1 Functions

In this sample task, the interrupt priority function is used to generate TPU compare match interrupt processing during IRQ0 interrupt processing. A block diagram of the interrupt controller is shown in figure 2.

- Interrupt priority registers (IPRA to IPRE)

  The interrupt priority registers set interrupt priorities (level 2 to 0) for interrupts other than an address break. Priority level 0 is the lowest, and priority level 2 the highest.

- Interrupt mask register (INTM)

  INTM is an 8-bit readable/writable register that controls masking of the three interrupt levels set by the interrupt priority registers.

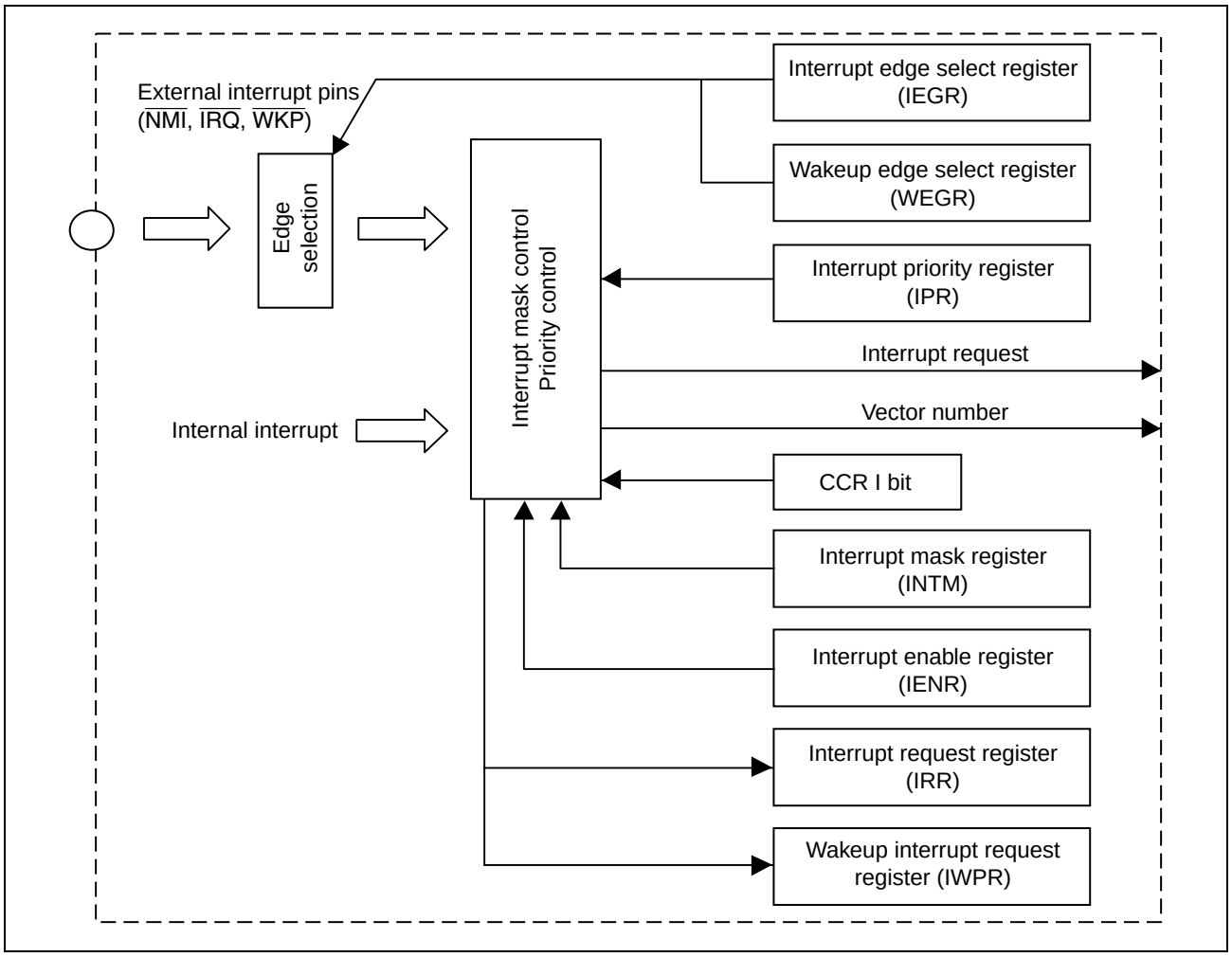


Figure 2 Block Diagram of Interrupt Controller

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, TPU compare match interrupt processing is performed during IRQ0 interrupt processing by means of the interrupt priority function.

Table 1 Assignment of Functions

Elements	Description
IERG0	$\overline{\text{IRQ0}}$ pin input edge selection
IENR1	Enables $\overline{\text{IRQ0}}$ pin interrupt request
IRR1	IRQ0 interrupt request flag
IPRA	IRQ0 interrupt priority selection
PMRB	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$ pin/port selection
PDRB	Register that stores port B data
INTM	3-level interrupt mask control
IPRC	TPU interrupt priority selection
TCR_1	Sets TGRA_1 compare match as TCNT_1 counter clearing source, rising edge as input clock edge, and internal clock ϕ/256 as clock source
TMDR_1	Sets normal operation mode as TPU channel 1 operating mode
TIER_1	Enables or disables interrupt request
TSR_1	Indicates timer status
TCNT_1	16-bit counter using internal clock ϕ/256 as clock source
TGRA_1	16-bit compare match register
TSTR	Sets TCNT_1 count operation

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, interrupt priority based multiple interrupts is performed. (A TPU interrupt has priority when PBI is 0, and an IRQ0 interrupt when PBI is 1.)

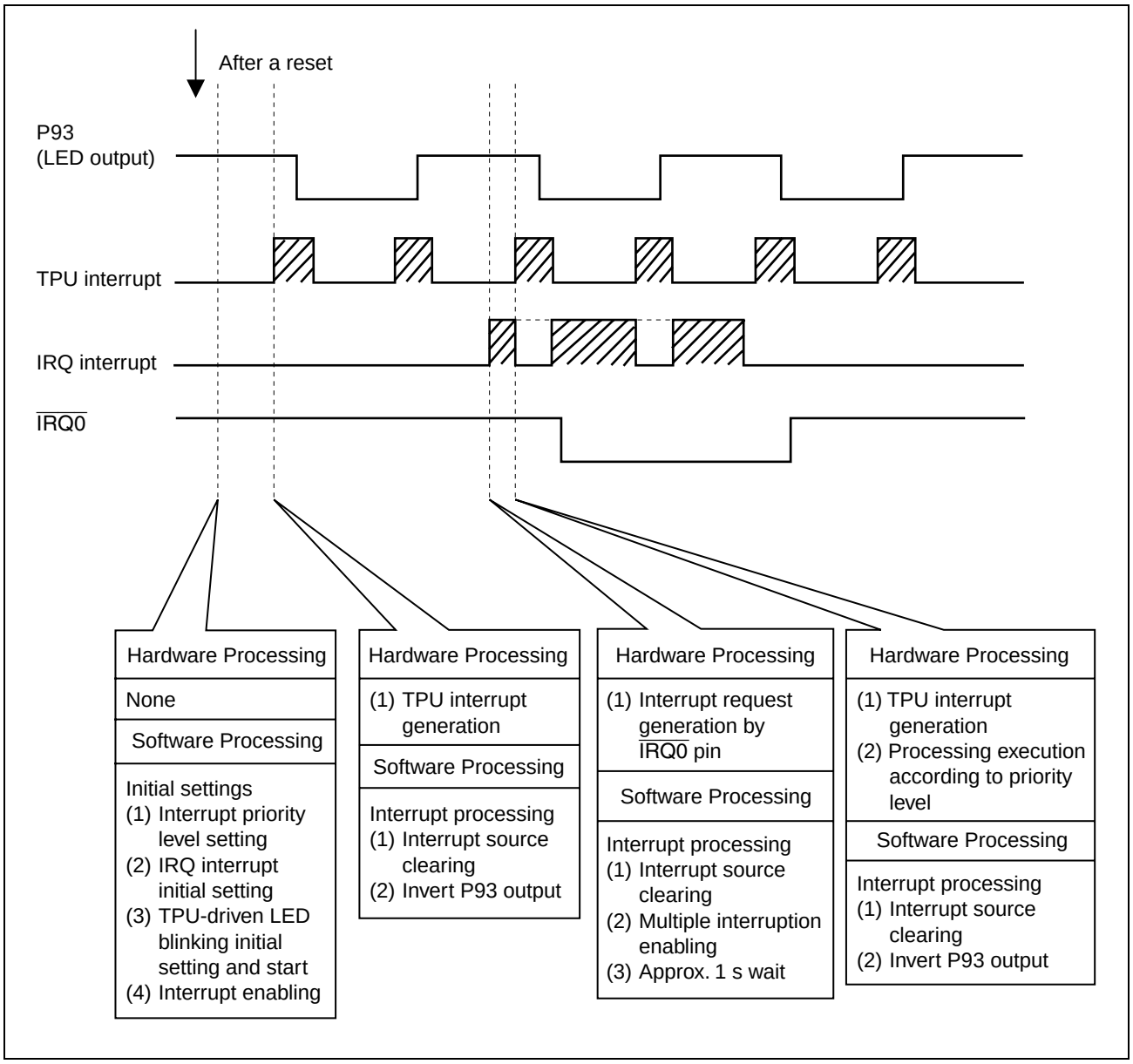


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	IRQ0 interrupt setting, sets P93 as output pin, outputs 0 (LED on)
Irq0_int	IRQ0 interrupt request flag clearing, sets masking of interrupts of interrupt priority level 0, clears I bit to 0 in CCR to enable multiple interrupts
tgia1int	Status flag clearing, inverts P93 output
init_tpu	TPU interrupt setting, interrupt priority level setting

4.2 Arguments

The arguments used in this sample task are shown in table 3.

Table 3 Arguments Used

Label	Description	Used in
unsigned short cycle	Specifies compare match generation cycle.	init_tpu
unsigned char level	Specifies interrupt priority level.	init_tpu

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- TSTR Timer start register Address: H'F030

Bit	Bit Name	Set Value	R/W	Description
1	CST1	1	R/W	Counter start 1 Selects TCNT_1 operation or stopping. CST1 = 1: TCNT_1 performs count operation

- TCR_1 Timer control register Address: H'F040

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	0	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_1 counter clearing source. CCLR1 = 0, CCLR0 = 1: TCNT_1 cleared by TGRA_1 compare match
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_1 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	1	R/W	Timer prescaler 2, 1, 0
1	TPSC1	1	R/W	Select the TCNT_1 clock source.
0	TPSC0	0	R/W	TPSC2 = 1, TPSC1 = 1, TPSC0 = 0: Counts on internal clock ϕ/256

- TMDR_1 Timer mode register Address: H'F041

Bit	Bit Name	Set Value	R/W	Description
1	MD1	0	R/W	Mode 1, 0
0	MD0	0	R/W	Select the TPU_1 operating mode. MD1 = 0, MD0 = 0: TPU_1 set to normal operation mode

- TIER_1 Timer interrupt enable register_1 Address: H'F044

Bit	Bit Name	Set Value	R/W	Description
0	TGIEA	1	R/W	TGR interrupt enable A Enables or disables TGFA flag interrupt request (TGI1A) when TGFA flag is set to 1 in TSR. TGIEA = 1: TGFA flag interrupt request (TGI1A) enabled

- TSR_1 Timer status register_1 Address: H'F045

Bit	Bit Name	Set Value	R/W	Description
0	TGFA	0	R/(W)*	Input capture/output compare flag A Status flag indicating generation of TGRA_1 input capture or compare match [Setting conditions] • When TCNT_1 = TGRA_1 while TGRA_1 is functioning as output compare register • When TCNT_1 value is transferred to TGRA_1 in response to input capture signal when TGRA_1 is functioning as input capture register [Clearing condition] When 0 is written to TGFA after TGFA is read while set to 1

Note: * Only 0 can be written to clear the flag.

- TGRA_1 Timer general register A_1 Address: H'F048

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	—	R/W	Timer general register A_1
14	Bit 14	—	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_1 is initialized to H'FFFF at a reset. TGRA_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	—	R/W	
12	Bit 12	—	R/W	
11	Bit 11	—	R/W	
10	Bit 10	—	R/W	
9	Bit 9	—	R/W	
8	Bit 8	—	R/W	
7	Bit 7	—	R/W	
6	Bit 6	—	R/W	
5	Bit 5	—	R/W	
4	Bit 4	—	R/W	
3	Bit 3	—	R/W	
2	Bit 2	—	R/W	
1	Bit 1	—	R/W	
0	Bit 0	—	R/W	

- IPRA Interrupt priority register A Address: H'F080

Bit	Bit Name	Set Value	R/W	Description
7	IPRA7	0	R/W	Interrupt source priority setting
6	IPRA6	0		00: Priority level 0 (lowest)
				01: Priority level 1
				1*: Priority level 2 (highest)

- IPRC Interrupt priority register C Address: H'F082

Bit	Bit Name	Set Value	R/W	Description
7	IPRC7	0	R/W	Interrupt source priority setting
6	IPRC6	—		00: Priority level 0 (lowest)
		(Argument)		01: Priority level 1
				1*: Priority level 2 (highest)

- PMRB Port mode register B Address: H'FFCA

Bit	Bit Name	Set Value	R/W	Description
0	IRQ0	1	R/W	PB0/AN0/$\overline{\text{IRQ0}}$ pin switching
				Sets whether PB0/AN0/$\overline{\text{IRQ0}}$ pin is to be used as PB0/AN0 pin or as $\overline{\text{IRQ0}}$ pin.
				1: Functions as $\overline{\text{IRQ0}}$ input pin

- PDR9 Port data register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	0	R/W	P93 data register Register that stores P93 data. If P93 is read while PCR93 bit is set to 1, the value stored in P93 is read, regardless of the actual pin state. If P93 is read while PCR93 bit is cleared to 0, the pin state are read.

- PDRB Port data register B Address: H'FFDE

Bit	Bit Name	Set Value	R/W	Description
1	PB1	0	R	When PDRB is read the pin states are always returned. However, when a pin for which an analog input channel is selected by CH3 to CH0 in AMR of the A/D converter is read, 0 is returned regardless of the input voltage.

- PCR9 Port control register 9 Address: H'FFEC

Bit	Bit Name	Set Value	R/W	Description
3	PCR93	1	W	P93 control register Controls P93 input/output. P93 is an output pin when PCR93 is set to 1, and an input pin when PCR93 is cleared to 0. This is a write-only register, and will always return a value of 1 if read.

- IEGR Interrupt edge select register Address: H'FFF2

Bit	Bit Name	Set Value	R/W	Description
0	IEG0	0	R/W	IRQ0 edge select 0: $\overline{\text{IRQ0}}$ pin input falling edge detected

- IENR1 Interrupt enable register 1 Address: H'FFF3

Bit	Bit Name	Set Value	R/W	Description
0	IEN0	1	R/W	IRQ0 interrupt request enable 1: IRQ0 interrupt requests enabled

- INTM Interrupt mask register Address: H'FFF5

Bit	Bit Name	Set Value	R/W	Description
0	INTM0	1	R/W	Sets the interrupt mask level. 1: Priority level 0 interrupts are masked

- IRR1 Interrupt flag register Address: H'FFF6

Bit	Bit Name	Set Value	R/W	Description
0	IRRI0	0	R/W	IRQ0 interrupt request flag 0: When the specified edge has not been detected 1: When the specified edge is detected

4.4 Constants Used

The constants used in this sample task are shown in table 4.

Table 4 Constants Used

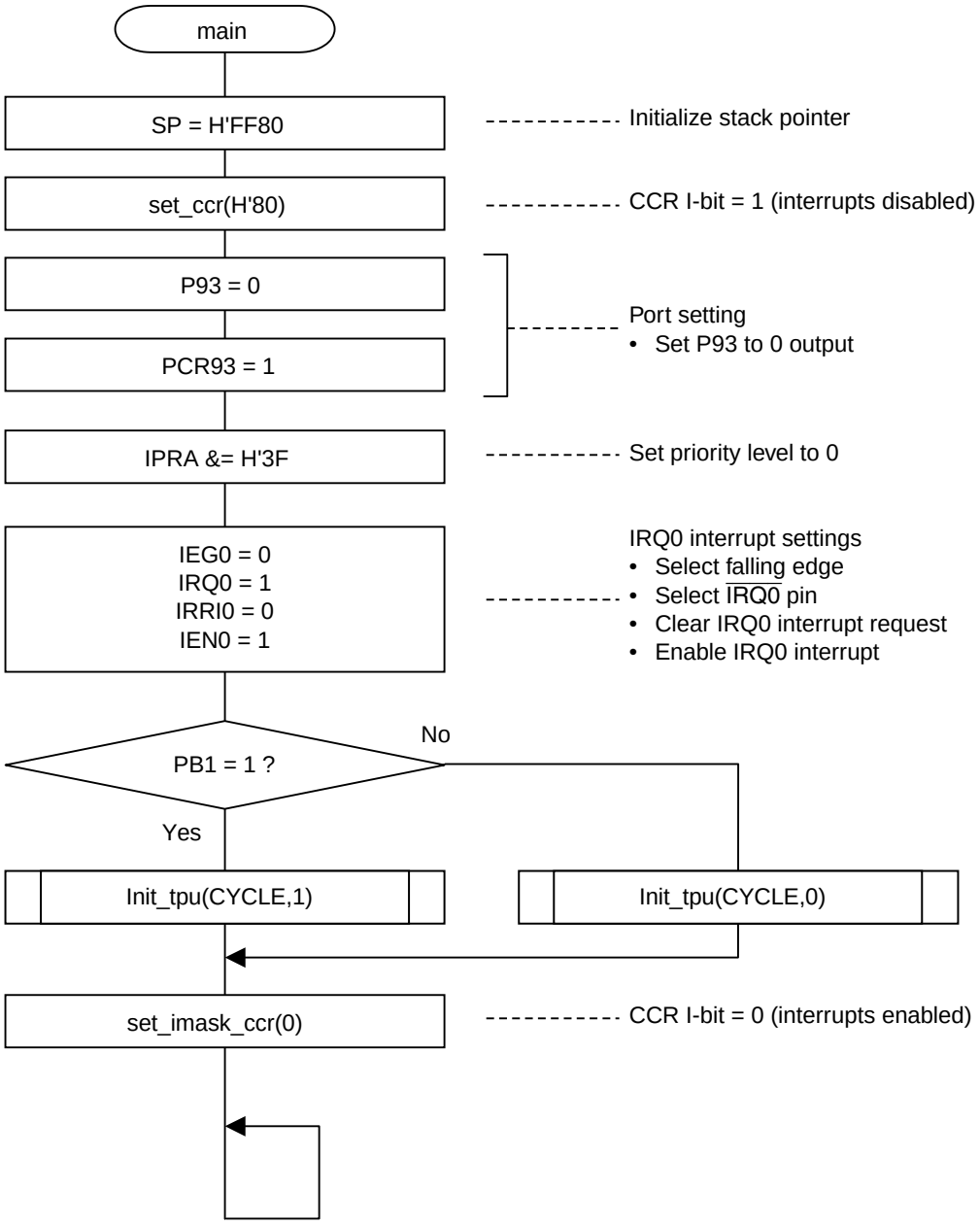
Label	Description	Used in
CYCLE	Specifies compare match generation cycle.	main, int_wkp0

4.5 RAM Usage

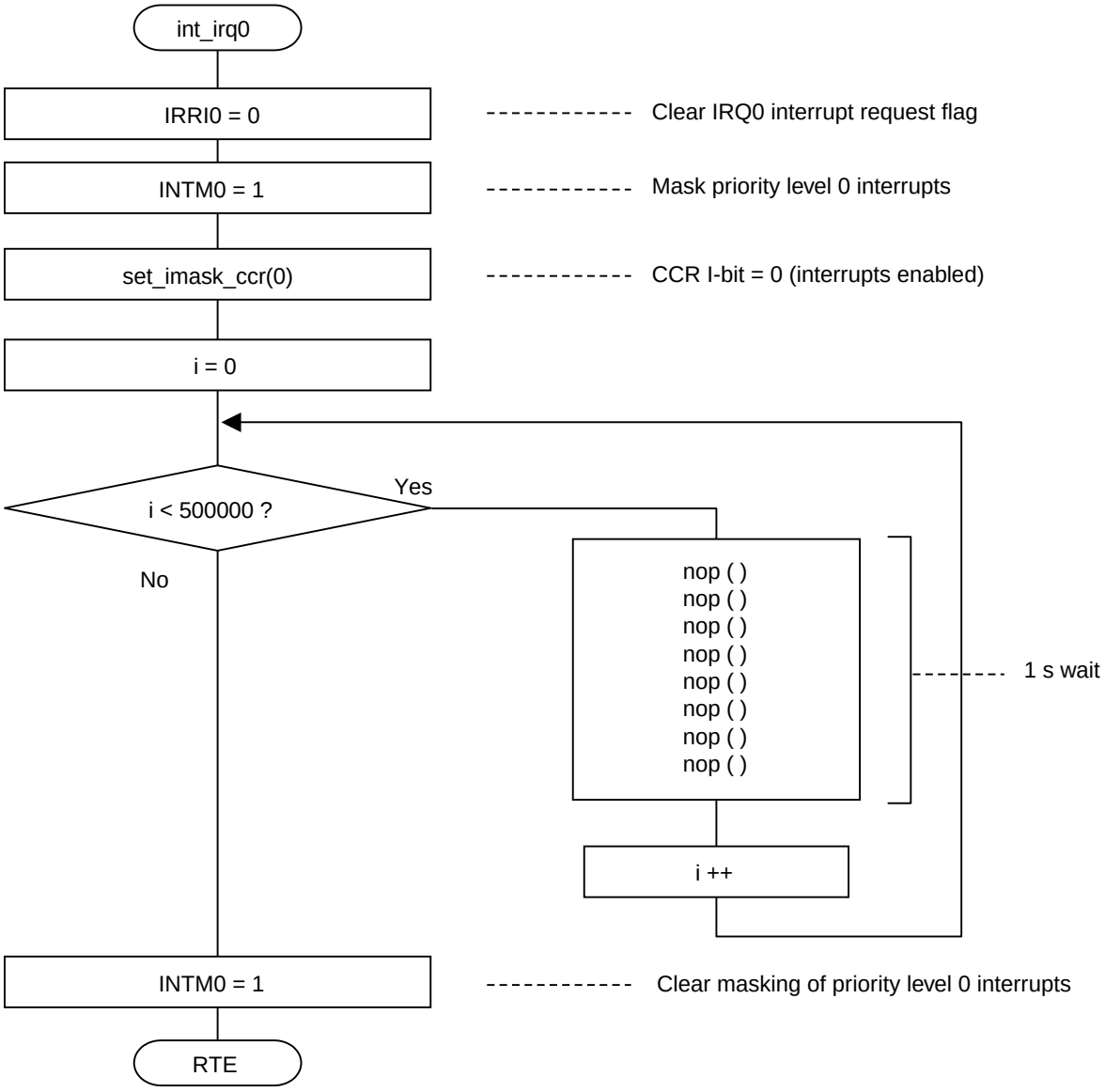
No RAM is used in this sample task.

5. Flowcharts

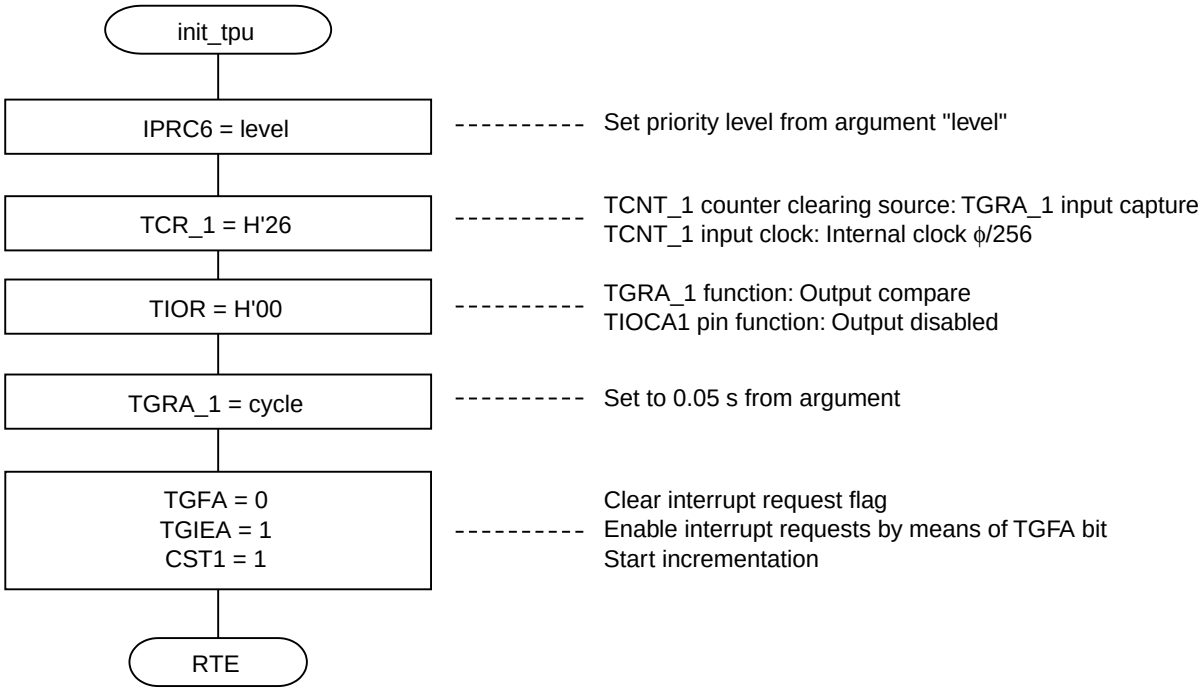
5.1 main



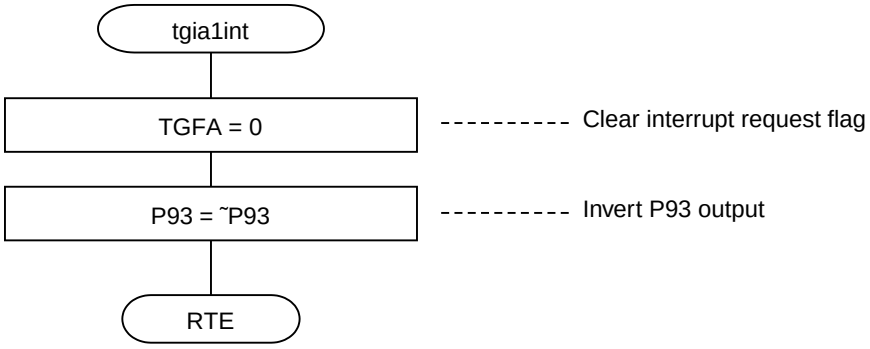
5.2 int_irq0


int_irq0
IRRI0 = 0
Clear IRQ0 interrupt request flag
INTM0 = 1
Mask priority level 0 interrupts
set_imask_ccr(0)
CCR I-bit = 0 (interrupts enabled)
i = 0
i < 500000 ?
Yes
No
nop ( )
nop ( )
nop ( )
nop ( )
nop ( )
nop ( )
nop ( )
nop ( )
1 s wait
i ++
INTM0 = 1
Clear masking of priority level 0 interrupts
RTE

5.3 init_tpu



5.4 tgia1int



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'000C
CV3	H'003A
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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