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April 1st, 2010
Renesas Electronics Corporation

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H8/300H SLP Series

Infrared Communication Using IrDA

Introduction

IrDA communication is performed using the encoding and decoding functions of serial communication interface 3 channel 1 (SCI3_1).

Target Device

H8/38076R

Contents

1. Specifications

1. Four bytes of data are transmitted and received using the IrDA communication function.
2. Communication data format settings are an 8-bit data length and a 1-bit stop bit length.
3. The bit rate is set to 9600 (bits/s).
4. Transmit data is output from the IrTxD pin as an encoded waveform compliant with IrDA Standard Version 1.0.
5. Receive data is input to the IrRxD pin as a decoded waveform compliant with IrDA Standard Version 1.0.

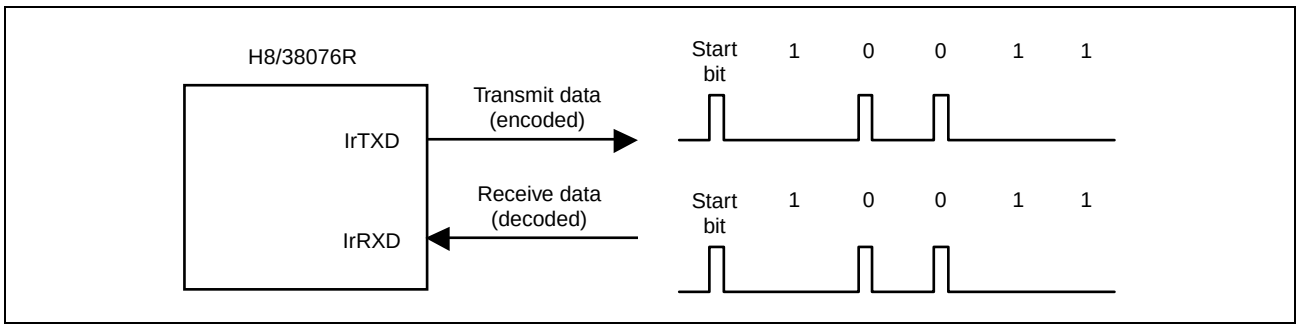


Figure 1 IrDA Communication

2. Functions Used

2.1 IrDA Function

In this sample task, the encoding and decoding functions of serial communication interface 3 channel 1 (SCI3_1) is used to output a transmit waveform and input a receive waveform compliant with IrDA Standard Version 1.0. A block diagram of serial communication interface 3 is shown in figure 1. The functions used are explained below.

- IrDA communication is performed in the asynchronous mode. In the asynchronous mode, serial data communication is carried out with synchronization performed on a character-by-character basis.
- Independent transmitting and receiving units are provided, enabling transmission and reception to be performed simultaneously. Both the transmitting unit and the receiving unit have a double-buffer structure, allowing continuous transmission and continuous reception.
- Any bit rate can be selected with an internal baud rate generator.
- An internal clock or external clock can be selected as the transmit/receive clock.
- There are six interrupt sources: transmit end, transmit data empty, receive data full, overflow error, framing error, and parity error.

- Receive shift register (RSR)

  The register for receiving serial data. Serial data input from the IrRxD pin is decoded as a UART frame, set in RSR in the order of reception, starting with the LSB (bit 0), and converted to parallel data. When one byte of data has been received, the data is automatically transferred to RDR. The CPU cannot read or write to RSR directly.

- Receive data register (RDR)

  An 8-bit register that stores received serial data. When reception of one byte of data ends, the received data is transferred from RSR to RDR and the receive operation is completed. RSR is then able to receive. As RSR and RDR have a double-buffer configuration, continuous reception can be carried out. RDR is a receive-only register, and cannot be written to by the CPU.

- Transmit shift register (TSR)

  The register for transmitting serial data. Serial data transmission is performed by first transferring transmit data from TDR to TSR, outputting it in order starting with the LSB (bit 0), and encoding it as an IR frame that is output from the IrTxD pin. When one byte of data is transmitted, the next transmit data is automatically transferred from TDR to TSR, and transmission is started. However, data transfer from TDR to TSR is not performed if data has not been written to TDR (if 1 is set in TDRE). The CPU cannot read or write to TSR directly.

- Transmit data register (TDR)

  An 8-bit register that stores transmit data. When the TSR empty state is detected, transmit data written to TDR is transferred to TSR, and serial data transmission is started. Continuous transmission is possible by writing the next transmit data to TDR during transmission of the serial data in TSR. TDR can be read or written to by the CPU at any time.

- Serial mode register (SMR)

  An 8-bit register for selecting serial communication format settings and the clock source of the baud rate generator. SMR can be read or written to by the CPU at any time.

- Serial control register (SCR)

  An 8-bit register that enables or disables transmission or reception, clock output in the asynchronous mode, and interrupt requests, and selects clock for transmission or reception. SCR can be read or written to by the CPU at any time.

- Serial status register (SSR)

  An 8-bit register containing status flags indicating the operating state of SCI3 and multiprocessor bits for transfer. SSR can be read or written to by the CPU at any time, but 1 cannot be written to TDRE, RDRF, OER, PER, or FER. Also, to clear these bits by writing 0, it is first necessary to read 1. TEND and MPBR are read-only bits, and cannot be written to.

- Bit rate register (BRR)

  An 8-bit register used to set the transmit/receive bit rate together with the baud rate generator operating clock selected with CKS1 and CKS0 of SMR. BRR can be read or written to by the CPU at any time.

- Serial port control register (SPCR)

  An 8-bit register that controls the P42/TXD31 pin. In this task, the P42/TXD31 pin is set as the TXD31 output pin, and a setting is made so that TXD31 pin output data is not inverted. When this pin is used as the IrTxD pin, the IrE bit must be set to 1 in the IrDA control register (IrCR).

- IrDA control register (IrCR)

  Comprises a bit that sets SCI3 I/O pins as normal SCI pins or IrDA pins, and bits that set the high pulse width in IrDA output pulse encoding.

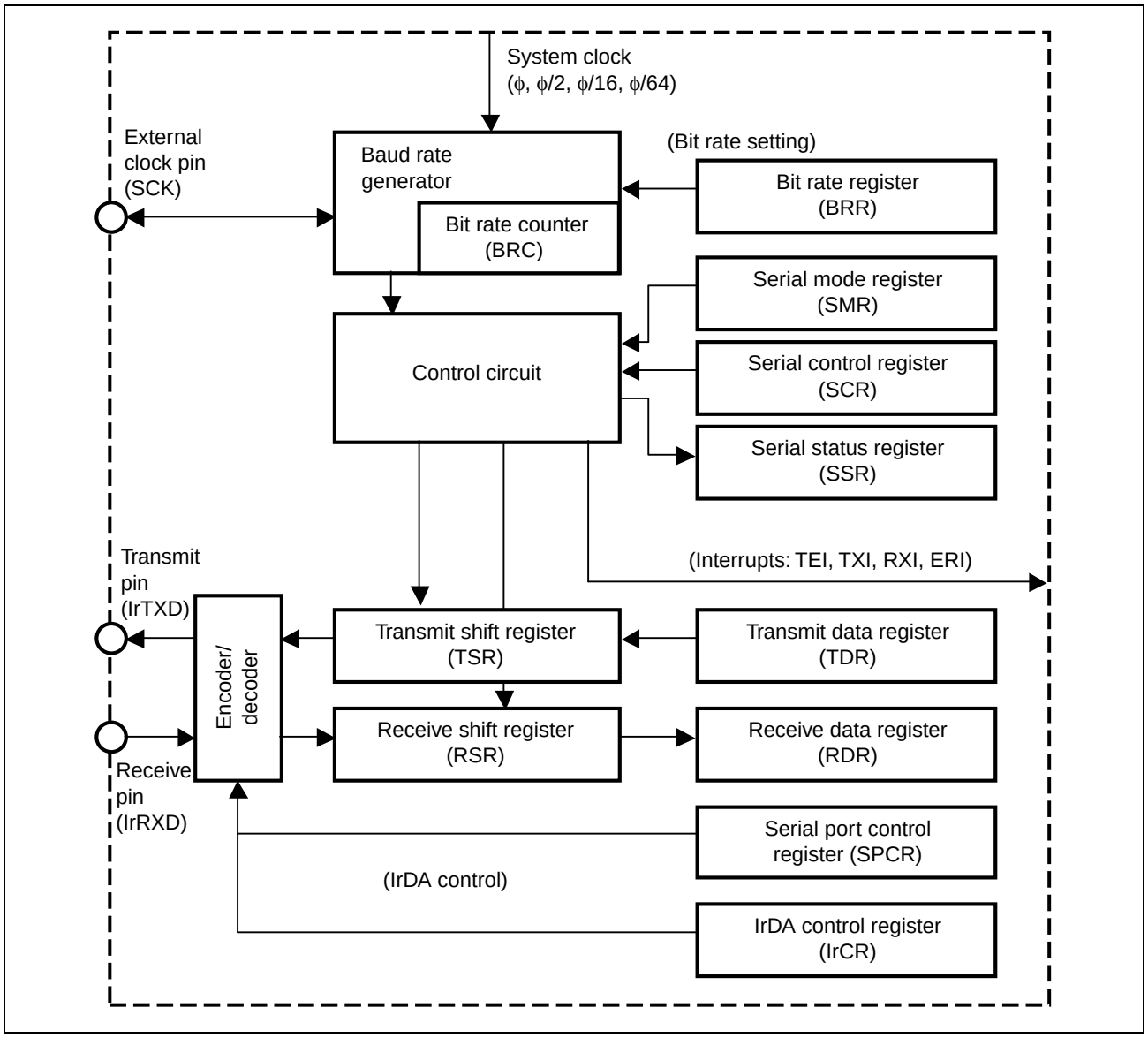


Figure 2 Block Diagram of SCI

- Examples of BRR settings in the asynchronous mode are shown in table 1. Table 1 shows values for the active (high-speed) mode when OSC is 10 MHz.

Table 1 Examples of Bit Rates and BRR Settings (Asynchronous Mode)

R Bit Rate (bits/s)	110	150	200	250	1200	2400	31250
n	2	2	2	2	2	0	0
N	177	129	97	77	15	129	9
Error (%)	–0.25	0.16	–0.35	0.16	1.73	0.16	0

Notes: 1. Settings with an error of 1% or less are recommended.
2. The BRR setting is calculated as follows.

$$N = \frac{OSC}{32 \times 2^{2n} \times B} - 1$$

$$\text{Error (\%)} = \frac{\text{B (Bit rate found from n, N, OSC)} - \text{R (Bit rate in table 1)}}{\text{R (Bit rate in table 1)}} \times 100$$

B: Bit rate (bits/s)
N: BRR setting for baud rate generator ($0 \le N \le 255$)
OSC: ϕ_{OSC} value (Hz)
n: Baud rate generator input clock no. (n = 0, 1, 2)
The relationship between n and the clock is shown in table 2.

Table 2 Relationship Between n and Clock

		SMR Settings	
n	**Clock**	**CKS1**	**CKS0**
0	ϕ	0	0
1	$\phi_w/2$, ϕ_w	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

3. The maximum bit rate (asynchronous mode) when OSC is 10 MHz is 38400 (bits/s). The settings are for the case where n = 0 and N = 7.

- The asynchronous mode is a serial communication mode in which characters in which a start bit indicating the start of communication and a stop bit indicating the end of communication are added to data and are transmitted and received, and synchronization is performed on a character-by-character basis.
- In SCI3 the transmitting unit and receiving unit are independent, enabling full-duplex communication to be carried out. Both the transmitting unit and the receiving unit have a double-buffer structure, allowing continuous transmission/reception to be performed by writing data during transmission and reading data during reception.
- In IrDA communication, transmission is performed by encoding an asynchronous mode UART frame and converting it to an IR frame, and reception is performed by converting an IR frame to a UART frame. The relationship between a UART frame and IR frame is shown in figure 4.
- The encoder outputs a high pulse of 3/16 the bit rate (1 bit width period) when UART frame serial data is 0, and does not output a pulse when serial data is 1.

- The decoder outputs serial data of "0" when a high pulse is detected in a UART frame, and outputs data "1" when there is no pulse during a 1-bit period.
- There are a total of six SCI3 interrupt sources — transmit end, transmit data empty, receive data full, and three kinds of receive error (overflow error, framing error, and parity error) — to which a common vector address is assigned.
- Interrupt requests are enabled or disabled by TIE and RIE of SCR.
- When TDRE is set to 1 in SSR, a TXI (transmit data empty interrupt) is generated. When TEND is set to 1 of SSR, a TEI (transmit end interrupt) is generated. These two interrupts are generated when transmitting.
- The initial state of TDRE of SSR is 1. Therefore, if TIE is set to 1 in SCR, enabling a transmit data empty interrupt request (TXI), before transmit data is transferred to TDR, TXI will be generated even though transmit data has not been prepared.
- The initial value of TEND of SSR is 1. Therefore, if TEIE is set to 1 in SSR, enabling a transmit end interrupt request (TEI), before transmit data is transferred to TDR, TEI will be generated even though transmit data is not transmitted.
- Performing processing to transfer transmit data to TDR in an interrupt processing routine enables these interrupts to be used effectively. Also, the generation of these interrupts (TXI and TEI) can be prevented by setting the enable bits (TIE and TEIE) for these interrupt requests to 1 after transmit data has been transferred to TDR.
- When RDRF is set to 1 in SSR, an RXI (receive data full interrupt) is generated. When OER, PER, or FER is set to 1, an ERI (receive error interrupt) is generated. These two interrupts are generated when receiving.

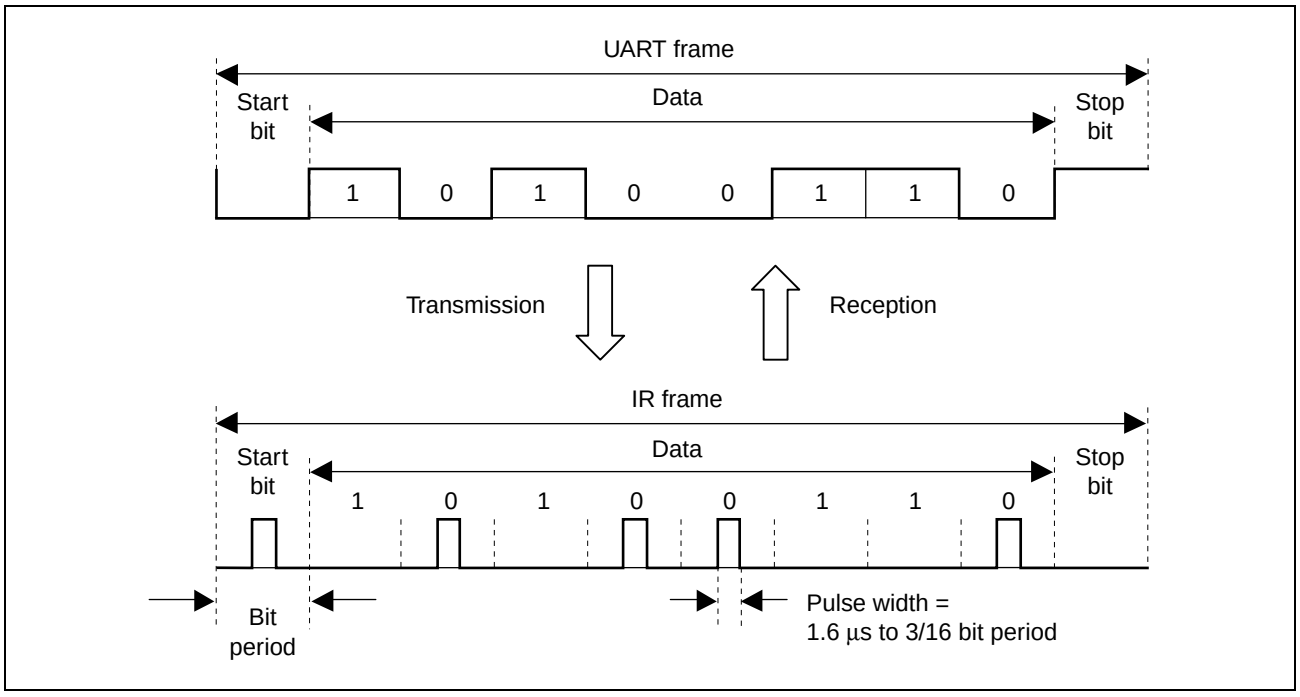


Figure 3 IrDA Communication Format

2.2 Assignment of Functions

Table 3 shows the assignment of functions in this sample task. IrDA communication is performed using functions assigned as shown in table 3.

Table 3 Assignment of Functions

Elements	Description
TSR_1	Register for transmitting serial data
TDR_1	Register that stores transmit data
SMR_1	Serial data communication format and baud rate generator clock source setting
SSR_1	Status flags indicating SCI3 operating status
BRR_1	Sets transmit/receive bit rate
RSR_1	Register for receiving serial data
RDR_1	Register that stores receive data
SPCR	TXD31, RXD31 pin function setting
IrCR	IrTXD, IrRXD pin setting, high pulse width setting
SCR_1	Transmission/reception and interrupt control, transmit/receive clock source selection
IrTXD	IrDA output pin
IrRXD	IrDA input pin

3. Principles of Operation

3.1 Transmit Operation

The principles of a transmit operation are illustrated in figure 4. IrDA transmission is performed using the hardware and software processing shown in figure 4.

- In this sample task, a transmit operation is started when PB0 becomes 0 after completion of initial settings. Four bytes of data (H'00, H'55, H'AA, and H'FF) are transmitted.

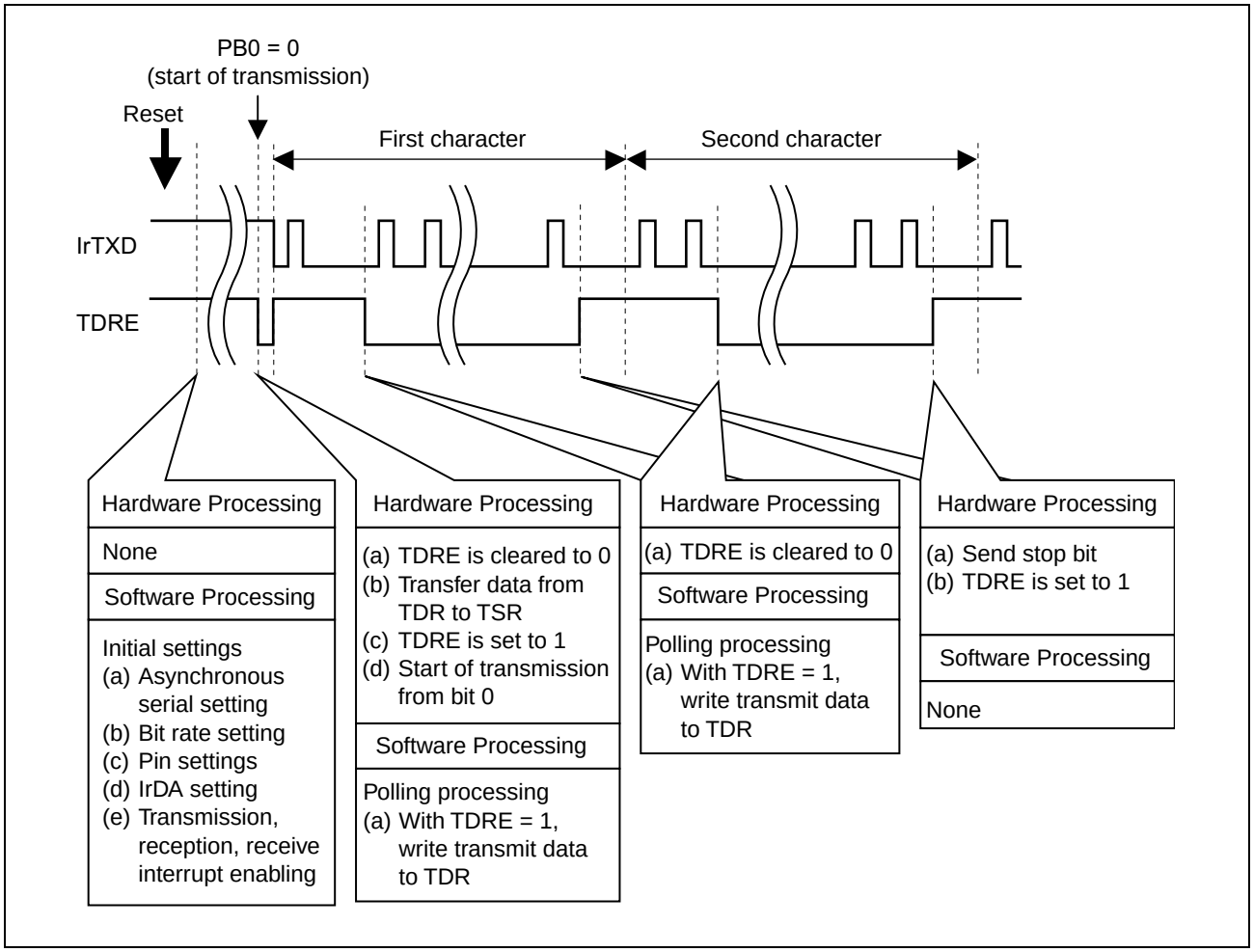


Figure 4 Principles of IrDA Transmit Operation

3.2 Receive Operation

The principles of a receive operation are illustrated in figure 5. IrDA reception is performed using the hardware and software processing shown in figure 5.

- In this sample task, a receive operation is performed using receive interrupts. After four bytes of data have been received, receive interrupts are disabled and the receive operation is terminated.

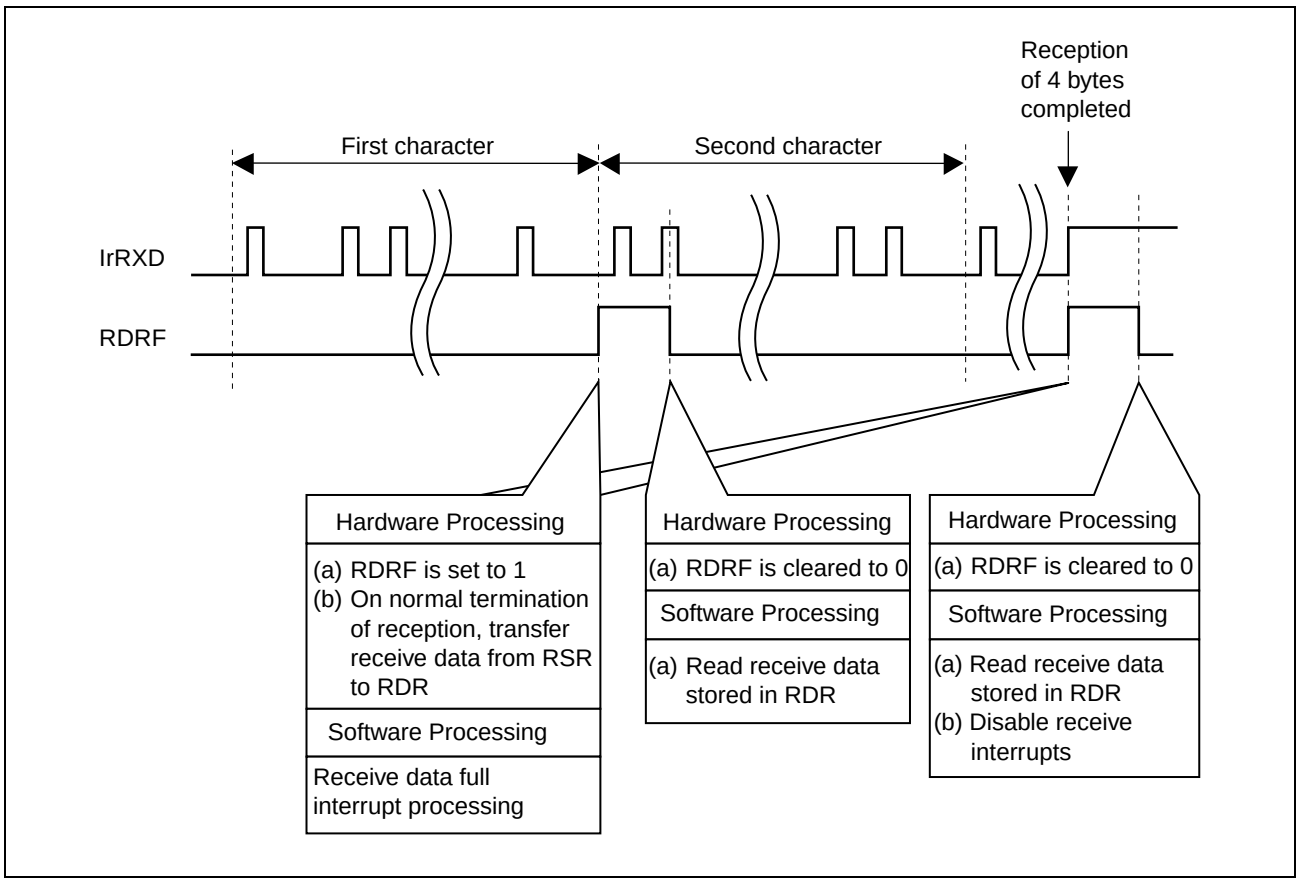


Figure 5 Principles of IrDA Receive Operation

4. Description of Software

4.1 Modules

Table 4 shows the modules used in this sample task.

Table 4 Modules

Function Name	Description
main	Initial settings, SCI3 control, interrupt enabling
int_recv_sci31	Receive interrupt processing, flag clearing, receive processing, error processing, receive interrupt disabling
init_sci31	SCI3 initial settings, IrDA setting, reception, transmission, receive interrupt enabling
trns_sci31	Transmit processing
stop_sci31	End of communication

4.2 Arguments

The arguments used in this sample task are shown in table 5.

Table 5 Arguments Used

Label	Description	Used in
unsigned char *t_ptr	Transmit data pointer	trns_sci31
unsigned char num	Number of transmit data bytes	trns_sci31

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- SPCR Serial port control register Address: H'FF91

Bit	Bit Name	Set Value	R/W	Description
4	SPC31	1	R/W	P42/TXD31 pin switching Selects whether P42/TXD31 pin is to be used as P42 pin or as TXD31 pin. 1: Functions as TXD31 output pin After setting this bit to 1, set the TE bit in SCR.

- SMR3_1 Serial mode register 3_1 Address: H'FF98

Bit	Bit Name	Set Value	R/W	Description
7	COM	0	R/W	Communication mode 0: Operates in the asynchronous mode
6	CHR	0	R/W	Character length (valid only in asynchronous mode) 0: Transmission/reception performed using 8-bit data length format
5	PE	0	R/W	Parity enable (valid only in the asynchronous mode) When this bit is set to 1, a parity bit is added when transmitting and a parity check is carried out when receiving.
4	PM	0	R/W	Parity mode (valid only in the asynchronous mode when PE = 1) 0: Transmission/reception performed using even parity 1: Transmission/reception performed using odd parity
3	STOP	0	R/W	Stop bit length (valid only in asynchronous mode) Selects the number of stop bits when transmitting. 0: 1 stop bit 1: 2 stop bits During reception, only the first stop bit is checked regardless of the setting of this bit, and if the second bit is 0 it is regarded as the start bit of the next transmit character.
2	MP	0	R/W	Multiprocessor bit 0: Multiprocessor communication function disabled 1: Multiprocessor communication function enabled
1	CKS1	0	R/W	Clock select 1, 0
0	CKS0	0	R/W	Select the clock source of the internal baud rate generator. CKS1 = 0, CKS0 = 0: ϕ clock (n = 0)

- BRR3_1 Bit rate register 3_1 Address: H'FF99

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	0	R/W	Bit rate register 3_1
6	Bit 6	0	R/W	8-bit readable/writable register used to set the bit rate.
5	Bit 5	1	R/W	Note: Set value: H'20
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- SCR3_1 Serial control register 3_1 Address: H'FF9A

Bit	Bit Name	Set Value	R/W	Description
6	RIE	1	R/W	Receive interrupt enable 1: RXI and ERI interrupt requests enabled
5	TE	1	R/W	Transmit enable 1: Transmit operation enabled
4	RE	1	R/W	Receive enable 1: Receive operation enabled
1	CKE1	0	R/W	Clock enable 1, 0
0	CKE0	0	R/W	Select the clock source. In asynchronous mode: CKE1 = 0, CKE0 = 0: Internal baud rate generator

- TDR3_1 Transmit data register 3_1 Address: H'FF9B

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	—	R/W	Transmit data register 3_1
6	Bit 6	—	R/W	8-bit register for storing transmit data
5	Bit 5	—	R/W	
4	Bit 4	—	R/W	
3	Bit 3	—	R/W	
2	Bit 2	—	R/W	
1	Bit 1	—	R/W	
0	Bit 0	—	R/W	

- SSR3_1 Serial status register 3_1 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
7	TDRE	—	R/(W)*	Transmit data register empty Indicates presence or absence of transmit data in TDR. [Setting conditions] • When TE in SCR3_1 is 0 • When data is transferred from TDR3_1 to TSR3_1 [Clearing conditions] • When 0 is written to TDRE after reading 1 from TDRE • When transmit data is written to TDR3_1
6	RDRF	—	R/(W)*	Receive data register full Indicates presence or absence of transmit data in RDR3_1. [Setting condition] • When reception ends normally and receive data is transferred from RSR3_1 to RDR3_1
5	OER	0	R/(W)*	Overflow error [Setting condition] • When an overflow error occurs during reception [Clearing condition] • When 0 is written to OER after reading 1 from OER
4	FER	0	R/(W)*	Framing error [Setting condition] • When a framing error occurs during reception [Clearing condition] • When 0 is written to FER after reading 1 from FER
2	TEND	0	R	Transmit end [Setting conditions] • When TE in SCR3_1 is 0 • When TDRE is 1 when the last transmit character bit is transmitted [Clearing conditions] • When 0 is written to TDRE after reading 1 from TDRE • When transmit data is written to TDR3_1

Note: * Only 0 can be written to clear the flag.

- RDR3_1 Receive data register 3_1 Address: H'FF9D

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	—	R	Receive data register 3_1
6	Bit 6	—	R	8-bit register for storing receive data.
5	Bit 5	—	R	
4	Bit 4	—	R	
3	Bit 3	—	R	
2	Bit 2	—	R	
1	Bit 1	—	R	
0	Bit 0	—	R	

- IrCR IrDA control register Address: H'FFA7

Bit	Bit Name	Set Value	R/W	Description
7	IrE	1	R/W	IrDA enable Sets SCI3 I/O pins as SCI pins or IrDA pins. 1: TXD31/IrTXD or RXD31/IrRXD pin operates as IrTXD or IrRXD pin
5	TE	1	R/W	Transmit enable 1: Transmit operation enabled

- PDRB Port data register B Address: H'FFDE

Bit	Bit Name	Set Value	R/W	Description
0	PB0	0	R	When PDRB is read the pin states are always returned. However, when a pin for which an analog input channel is selected by CH3 to CH0 in AMR of the A/D converter is read, 0 is returned regardless of the input voltage.

4.4 Constants Used

The constants used in this sample task are shown in table 6.

Table 6 Constants Used

Label	Constant	Description	Used in
DATA_NUM	4	Number of transmit/receive data bytes	main, int_recv_sci31

4.5 RAM Usage

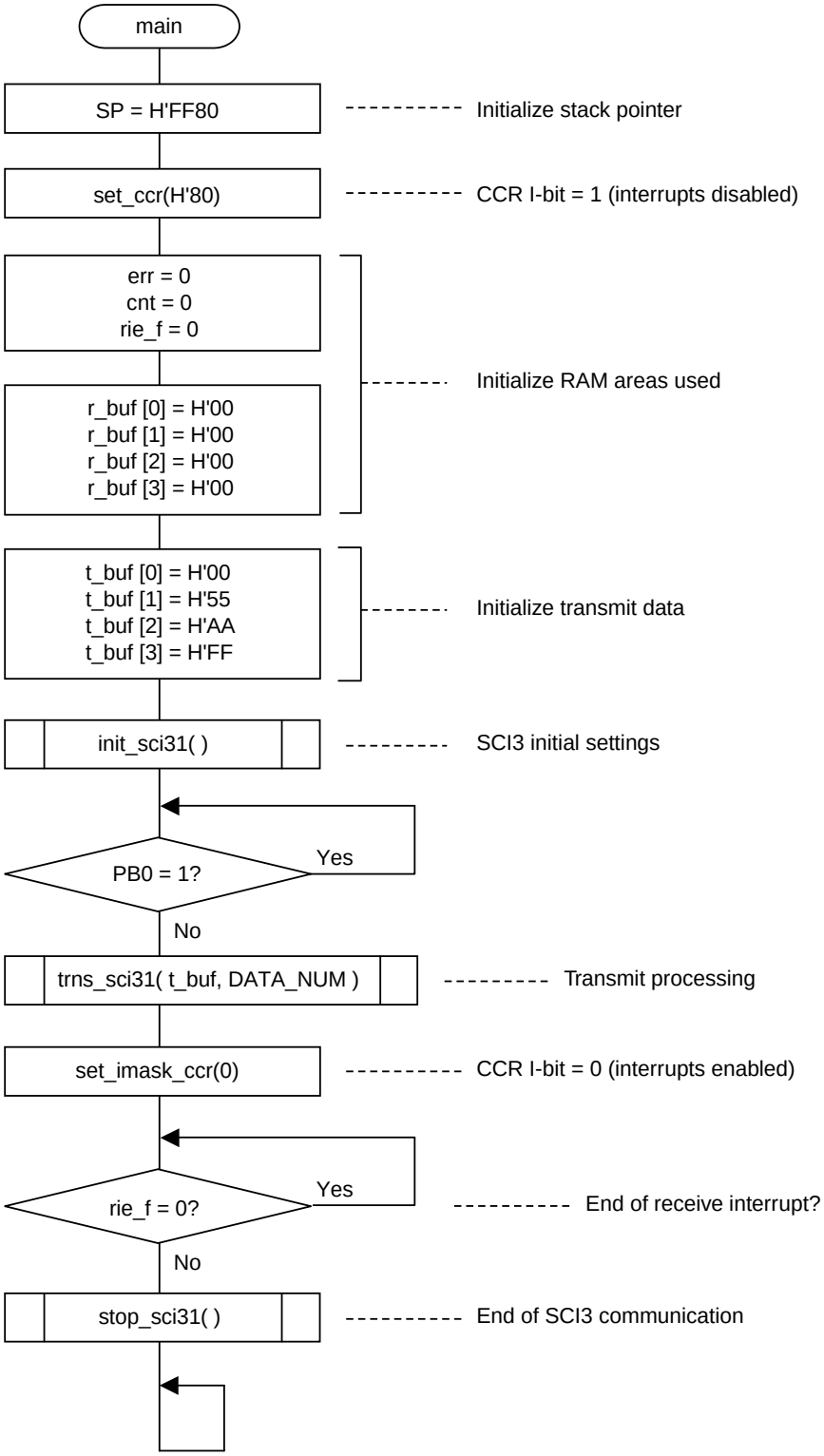
Table 7 describes RAM usage in this sample task.

Table 7 RAM Usage

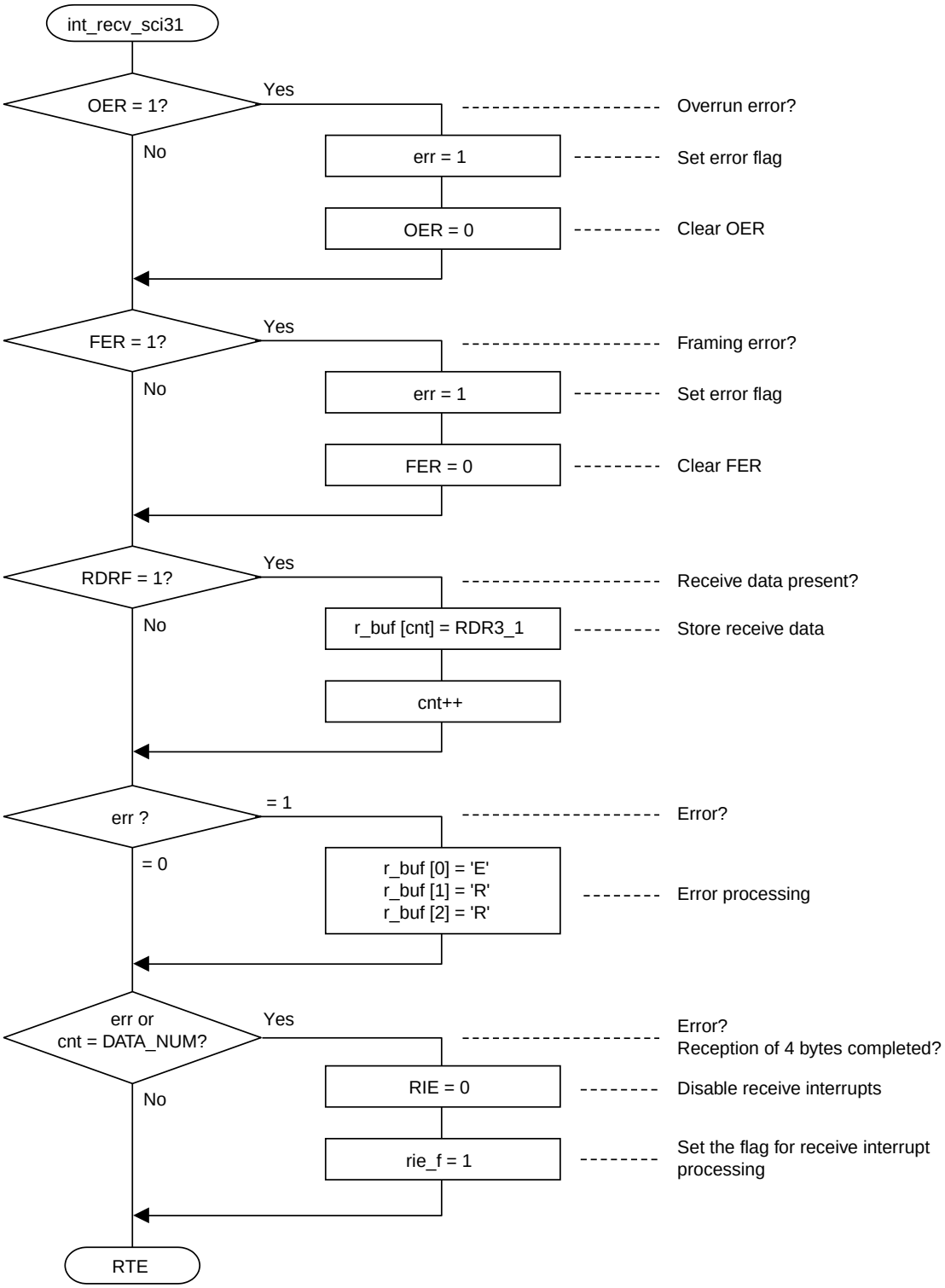
Label	Description	Amount of Memory Used	Used in
err	Receive error presence/absence	1 byte	main, int_recv_sci31
cnt	Receive data counter	1 byte	main, int_recv_sci31
rie_f	Receive interrupt end flag	1 byte	main, int_recv_sci31
r_buf[ ]	Receive data storage buffer	4 bytes	main, int_recv_sci31

5. Flowcharts

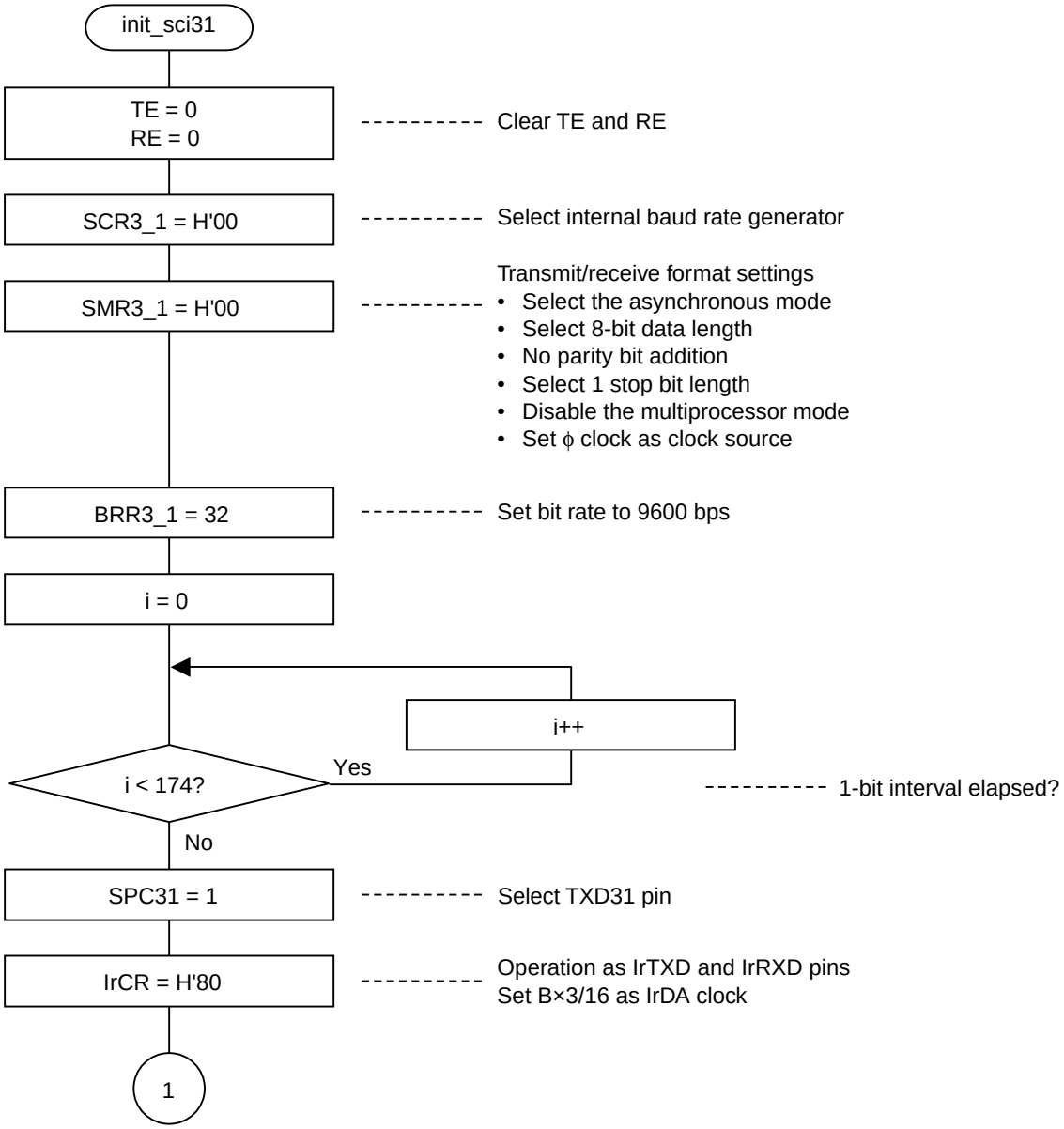
5.1 main

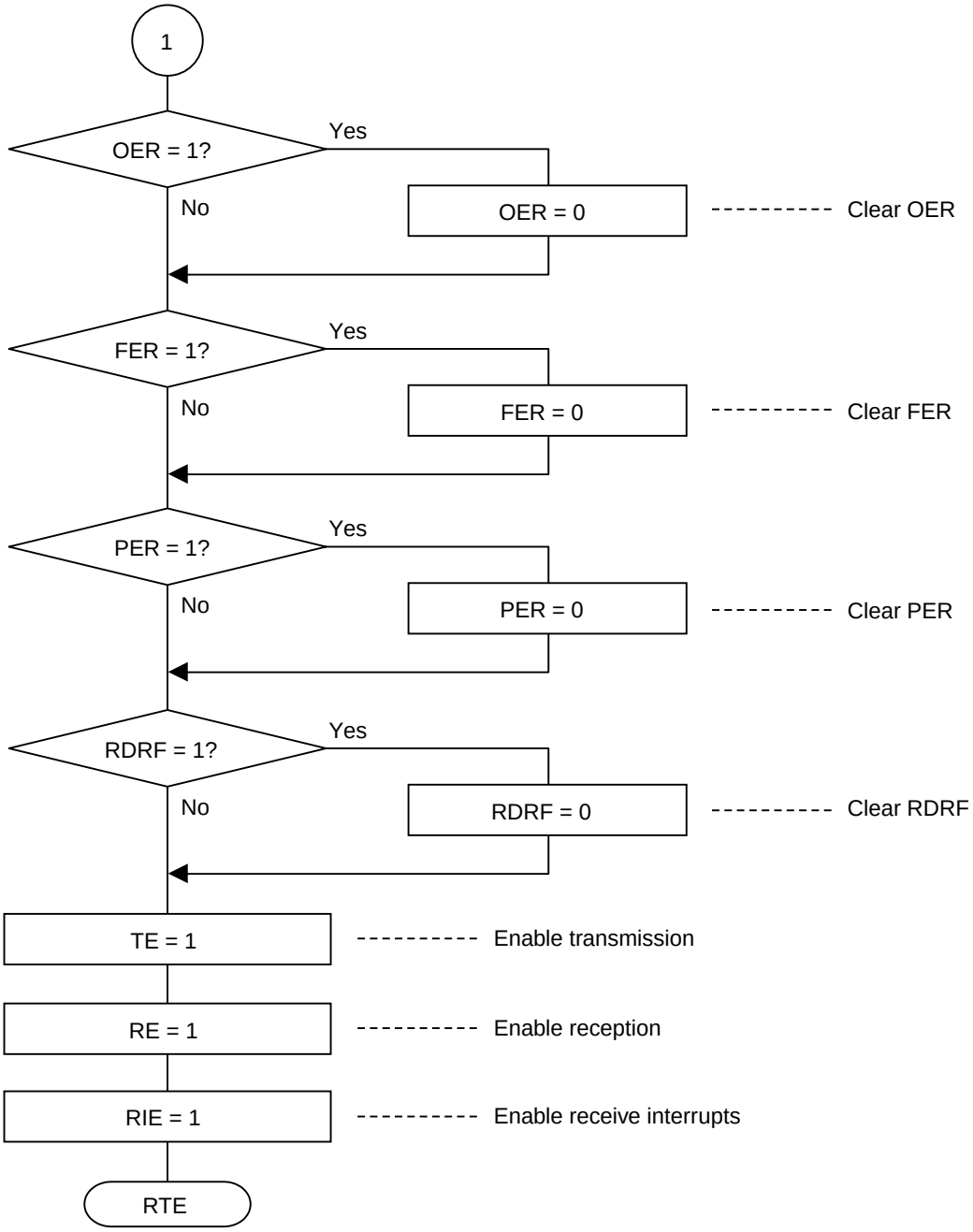


5.2 int_recv_sci31

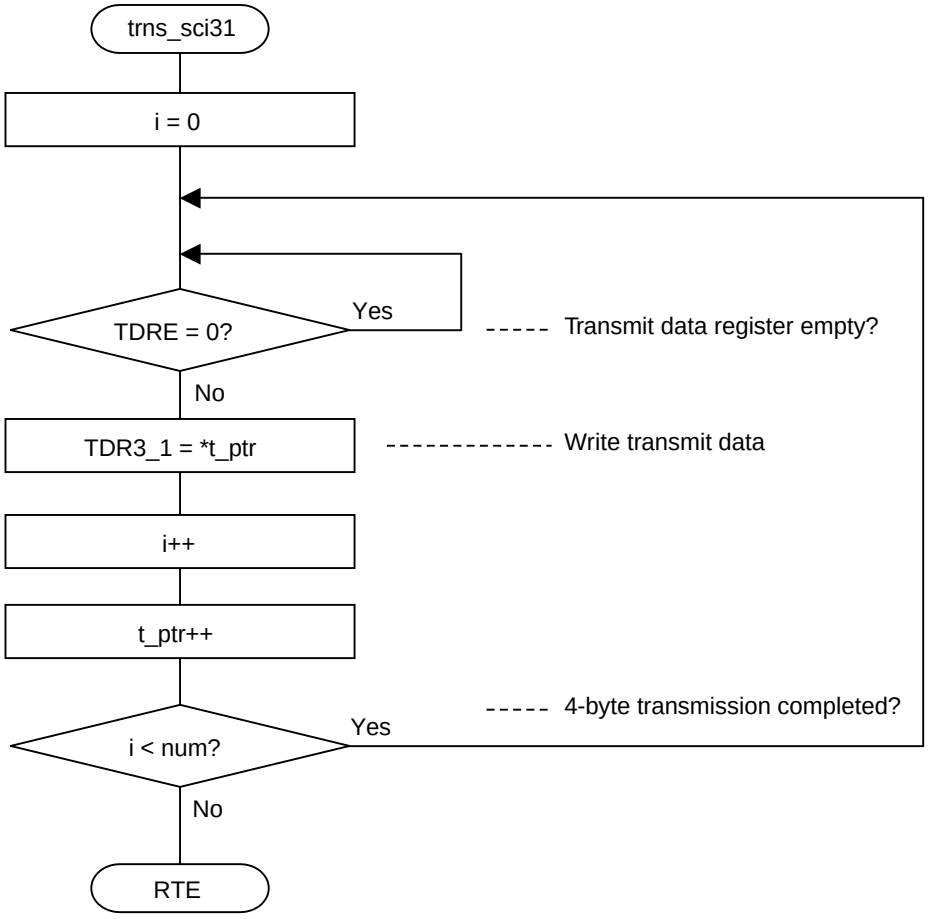


5.3 int_tci1v

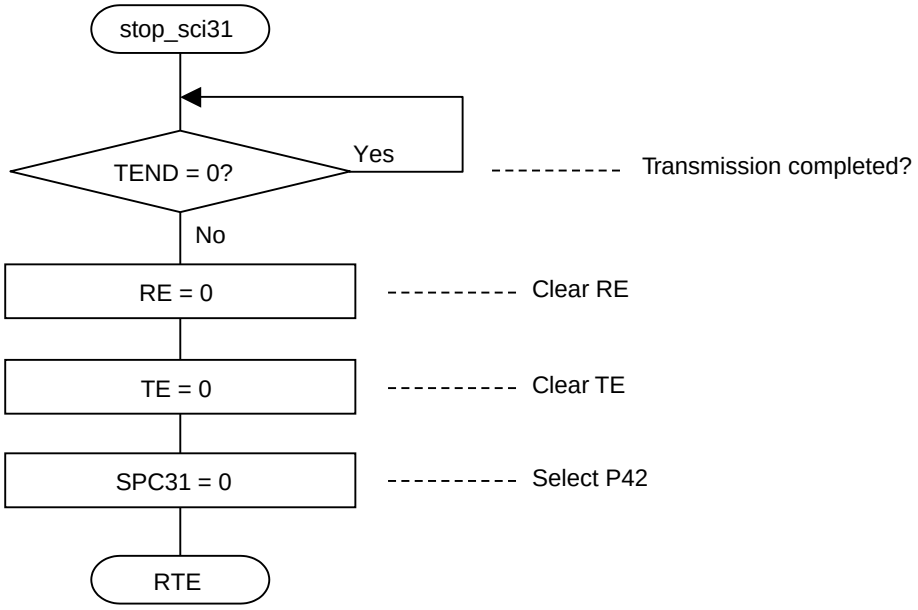

init_sci31
TE = 0
RE = 0
Clear TE and RE
SCR3_1 = H'00
Select internal baud rate generator
SMR3_1 = H'00
Transmit/receive format settings
• Select the asynchronous mode
• Select 8-bit data length
• No parity bit addition
• Select 1 stop bit length
• Disable the multiprocessor mode
• Set ϕ clock as clock source
BRR3_1 = 32
Set bit rate to 9600 bps
i = 0
i++
i < 174?
Yes
1-bit interval elapsed?
No
SPC31 = 1
Select TXD31 pin
IrCR = H'80
Operation as IrTXD and IrRXD pins
Set B×3/16 as IrDA clock
1


1
OER = 1?
Yes
No
OER = 0
Clear OER
FER = 1?
Yes
No
FER = 0
Clear FER
PER = 1?
Yes
No
PER = 0
Clear PER
RDRF = 1?
Yes
No
RDRF = 0
Clear RDRF
TE = 1
Enable transmission
RE = 1
Enable reception
RIE = 1
Enable receive interrupts
RTE

5.4 trns_sci31



5.5 stop_sci31



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'004C
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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