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April 1st, 2010
Renesas Electronics Corporation

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H8/300H SLP Series

Duty Pulse Output Using 14-Bit PWM Function

Introduction

The 14-bit PWM output function is used to output duty pulses from the PWM1 output pin.

Target Device

H8/38076R

Contents

1. Specifications

- The 14-bit PWM output function is used to output duty pulses from the PWM1 output pin, as shown in figure 1.
- This sample task outputs duty pulses with a pulse cycle of 25.6 µs, pulse high width of 19.2 µs, and duty cycle of 75%.

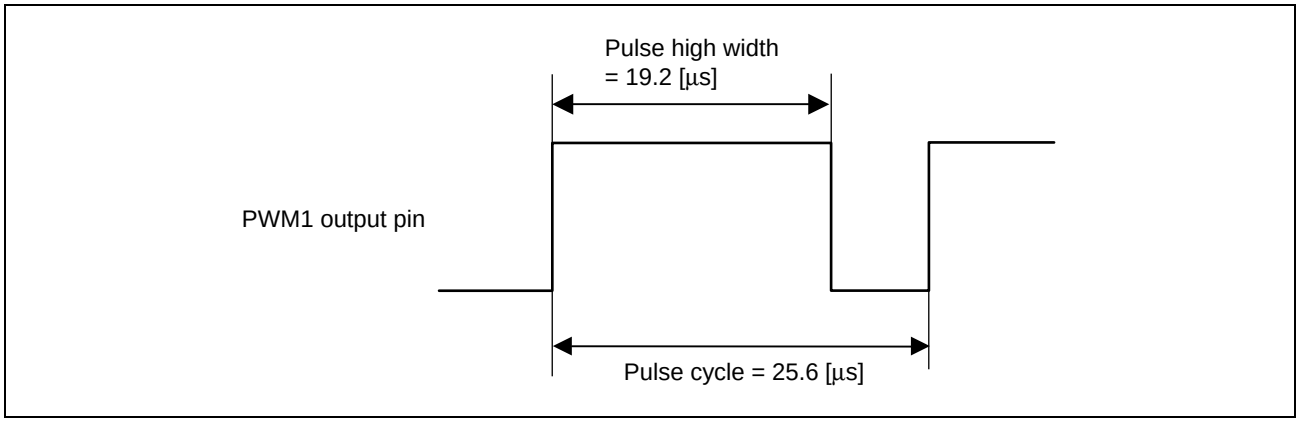


Figure 1 Duty Pulse Output Using 14-Bit PWM Function

2. Functions Used

2.1 Functions

In this sample task, the 14-bit PWM function is used to output duty pulses from the PWM1 output pin. A block diagram of the 14-bit PWM function is shown in figure 2. The block diagram of the 14-bit PWM function is explained below.

- System clock (ϕ)

  The reference clock for operating the CPU and peripheral functions (in this sample task, 10 MHz)

- PWM data register (PWDR)

  PWDR is a 14-bit write-only register that indicates the high-level width of one PWM waveform cycle when pulse-division type PWM is selected. When 14-bit data is written to PWDR, the contents written to PWDR are latched in the PWM waveform generator, and PWM waveform generation data is updated.

- PWM control register (PWCR)

  PWCR selects the input clock and standard PWM or pulse-division type PWM.

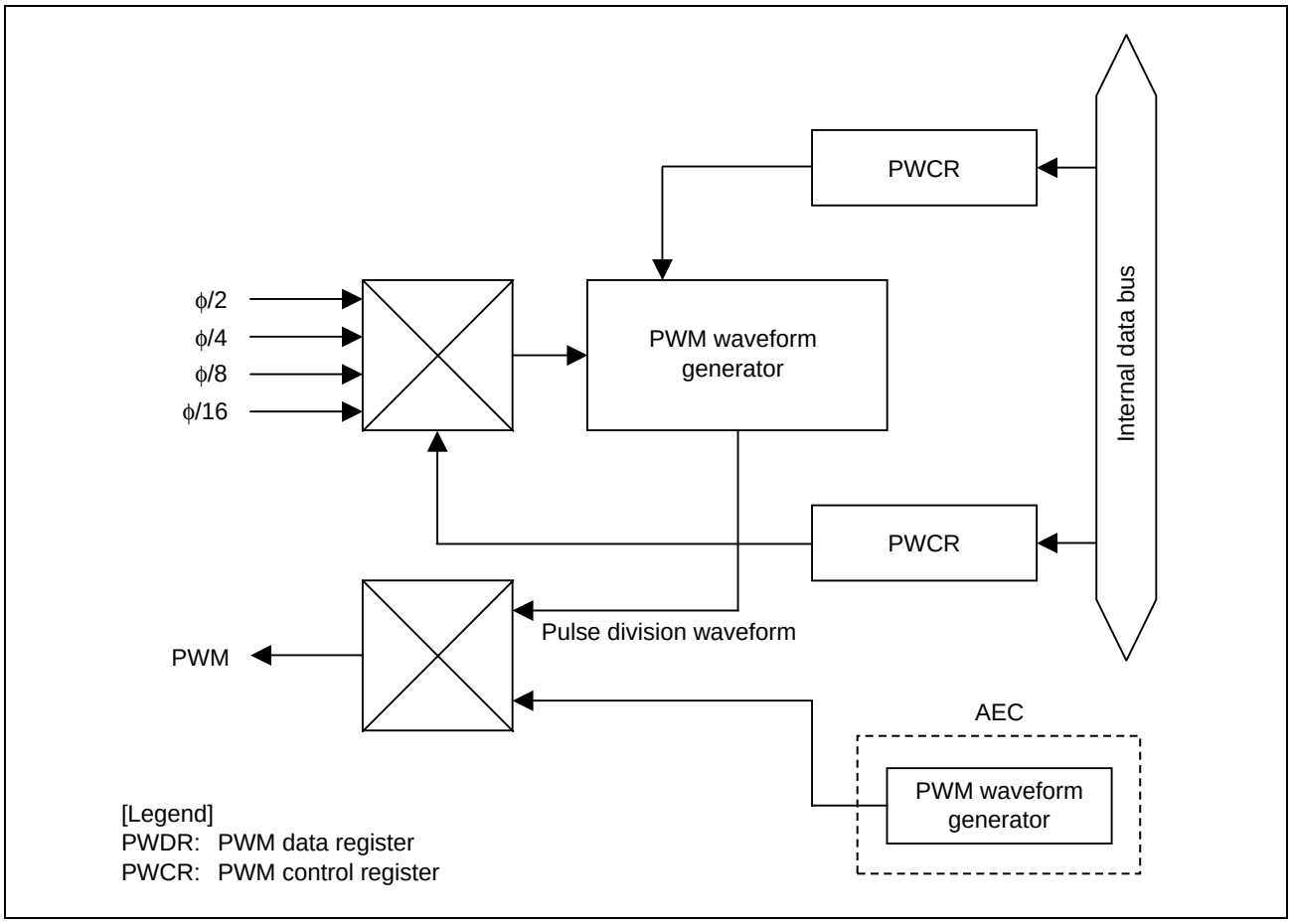


Figure 2 Block Diagram of 14-Bit PWM Function

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. PWM duty pulse is output using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Description
PMR9	Sets the p90/PWM1 pin to be used as the PWM1 output pin.
PWCR1	Sets the conversion period to 16384/ϕ, input clock supplied to the PWM to be ϕ/2, and pulse-division type PWM waveform to be output from the PWM1 output pin.
PWDR1	Sets high level width in one PWM waveform cycle to 19.2 μs.

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. By means of the hardware and software processing shown in figure 3, duty pulses are output from the PWM1 pin using the 14-bit PWM function.

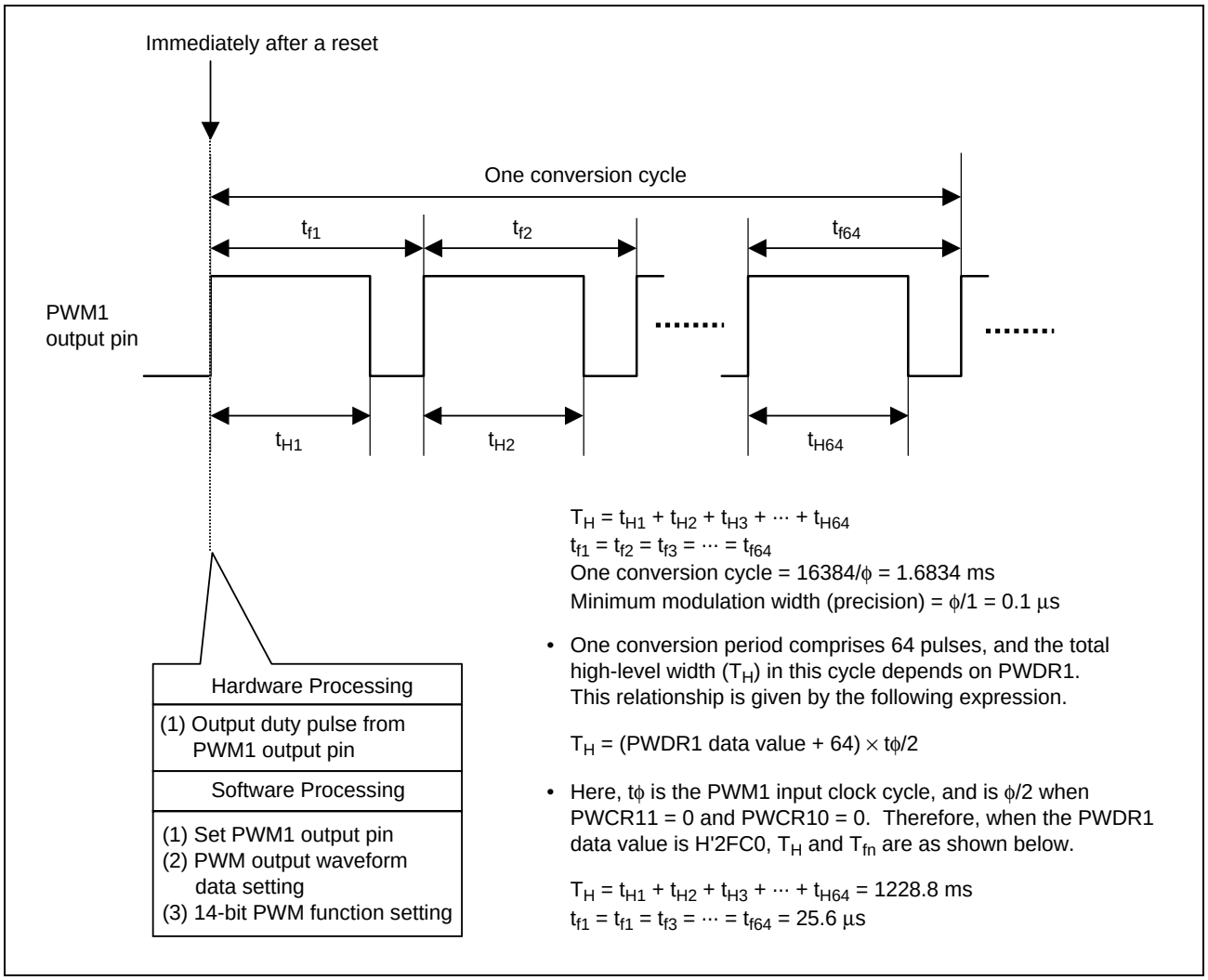


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	Sets P90/PWM1 pin as PWM1 output pin. Sets 14-bit PWM function.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- PMR9 Port mode register 9 Address: H'FFC8

Bit	Bit Name	Set Value	R/W	Description
0	PWM1	1	R/W	P90/PWM1 pin function switching Sets whether P90/PWM1 pin is to be used as P90 pin or as PWM1 pin. 0: P90 I/O pin 1: PWM1 output pin

- PWCR1 PWM control register_1 Address: H'FFD0

Bit	Bit Name	Set Value	R/W	Description
2	PWCR12	0	W	PWM output waveform select Selects whether the standard PWM waveform or pulsedivision type PWM waveform is output. 0: Pulse division PWM waveform is output 1: Standard PWM waveform is output
1	PWCR11	0	W	Clock select 1, 0
0	PWCR10	0	W	Selects the clock supplied to the 14-bit PWM. These bits are write-only bits and always read as 1. 00: Input clock = ϕ/2 (t/ϕ* = 2/ϕ) PWM waveform with 16384/ϕ conversion period and 1/ϕ minimum modulation width is generated. 01: Input clock = ϕ/4 (t/ϕ* = 4/ϕ) PWM waveform with 32768/ϕ conversion period and 2/ϕ minimum modulation width is generated. 10: Input clock = ϕ/8 (t/ϕ* = 8/ϕ) PWM waveform with 65536/ϕ conversion period and 4/ϕ minimum modulation width is generated. 11: Input clock = ϕ/16 (t/ϕ* = 16/ϕ) PWM waveform with 131072/ϕ conversion period and 8/ϕ minimum modulation width is generated.

Note: t/ϕ*: PWM1 input clock cycle

- PWDR1 PWM data register_1 Address: H'FFD2

  Function: PWDR1 is a 14-bit write-only register that indicates the high-level width of one PWM waveform cycle when pulse-division type PWM is selected. When 14-bit data is written to PWDR1, the contents written to PWDR1 are captured in the PWM waveform generator, and PWM waveform generation data is updated.

  Set value: H'EFC0

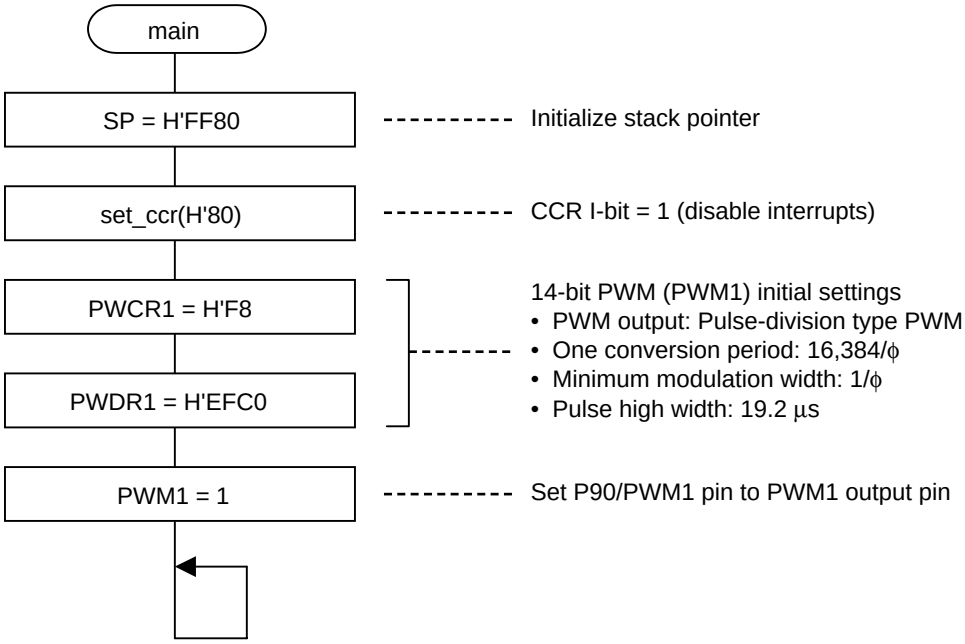
  R/W: W

4.4 RAM Usage

No RAM is used in this sample task.

5. Flowcharts

5.1 main



- Link Address Specifications

Section Name	Address
CV1	H'0000
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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