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Renesas Electronics Corporation

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**H8/300H SLP Series**

Count Start by the WKP Interrupt

**Introduction**

Turning on switch input connected to a WKP pin generates a WKP interrupt and starts incrementing of a 16-bit counter set in a 2-byte variable ("counter").

**Target Device**

H8/38076R

**Contents**

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2. Functions Used.......................................................... 3
3. Principles of Operation ............................................... 5
4. Description of Software ............................................. 6
5. Flowcharts .............................................................. 8
1. **Specifications**

1. Turning on switch input connected to the WKP0 pin generates a WKP interrupt and starts incrementing of a 16-bit counter set in a 2-byte variable ("counter").
2. A WKP interrupt is requested by falling edge detection of WKP0 pin input.
3. Incrementing of the 16-bit counter set in the 2-byte variable ("counter") is started in WKP interrupt processing.
4. An LED is switched on and off each time the 16-bit counter set in the 2-byte variable ("counter") overflows.
5. The LED is connected to the P93 output pin of port 9.
6. A sample connection diagram is shown in figure 1.

![Figure 1 Example of Connections for This Sample Task](image)

**Figure 1 Example of Connections for This Sample Task**
2. Functions Used

2.1 Functions

In this sample task, a count is started by means of a WKP interrupt. A block diagram of count starting using a WKP interrupt is shown in figure 2.

- **Wakeup edge select register (WEGR)**
  
  Selects the edge sensing direction that generates WKP7 to WKP0 pin interrupts. In this sample task, a WKP interrupt is requested on detection of a falling edge of WKP0 pin input.

- **Port mode register 5 (PMR5)**
  
  Controls switching of port 5 pin functions. The WKP7 to WKP0 pins also function as port 5 pins. To use these pins as WKP7 to WKP0 pins, bits WKP7 to WKP0 must be set to 1.

- **Wakeup interrupt request register (IWPR)**
  
  The WKP7 to WKP0 pin interrupt request status flag register. A bit is set to 1 when the WKP7 to WKP0 pins are set as input pins and a specified edge is detected.

![Block Diagram of Interrupt Controller](image)

**Figure 2** Block Diagram of Interrupt Controller
2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, counter incrementing is performed by means of WKP interrupts.

### Table 1 Assignment of Functions

<table>
<thead>
<tr>
<th>Elements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WEGR</td>
<td>WKP pin input edge selection</td>
</tr>
<tr>
<td>IENR1</td>
<td>Enables WKP pin interrupt requests</td>
</tr>
<tr>
<td>IWPR</td>
<td>WKP interrupt request flag</td>
</tr>
<tr>
<td>WKP0</td>
<td>WKP0 interrupt input pin</td>
</tr>
<tr>
<td>PMR5</td>
<td>WKP pin/port selection</td>
</tr>
</tbody>
</table>
3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, counter incrementing is performed by means of WKP interrupts.

![Figure 3 Principles of Operation](image-url)
4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2  Modules

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>main</td>
<td>WKP0 interrupt setting, sets P93 as output pin, outputs 1 (LED off)</td>
</tr>
<tr>
<td></td>
<td>After WKP0 interrupt generation, inverts P93 output due to counter overflow</td>
</tr>
<tr>
<td>int_wkp0</td>
<td>WKP0 interrupt processing, WKP0 interrupt request flag clearing, WKP0 interrupt disabling</td>
</tr>
</tbody>
</table>

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- **WEGR**  Wakeup edge select register  Address: H'FF90

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>WEGS0</td>
<td>0</td>
<td>R/W</td>
<td>Wakeup edge select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: WKP0 pin input falling edge detected</td>
</tr>
</tbody>
</table>

- **PMR5**  Port mode register 5  Address: H'FFC4

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>WKP0</td>
<td>1</td>
<td>R/W</td>
<td>P50/WKP0/SEG1 pin function switching</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When P50/WKP0/SEG1 pin is not used as SEG1 pin, sets whether it is to be used as P50 pin or as WKP0 pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Functions as WKP0 input pin</td>
</tr>
</tbody>
</table>

- **PDR9**  Port data register 9  Address: H'FFDC

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>P93</td>
<td>1</td>
<td>R/W</td>
<td>P93 data register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Register that stores P93 data. If P93 is read while PCR93 bit is set to 1, the value stored in P93 is read, regardless of the actual pin state. If P93 is read while PCR93 bit is cleared to 0, the pin state are read.</td>
</tr>
</tbody>
</table>
• **PCR9**  Port control register 9  
  Address: H'FFEC

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3   | PCR93    | 1         | W   | P93 control register  
  Controls P93 input/output. P93 is an output pin when PCR93 is set to 1, and an input pin when PCR93 is cleared to 0. This is a write-only register, and will always return a value of 1 if read. |

• **IENR1**  Interrupt enable register 1  
  Address: H'FFF3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 5   | IENWP    | 1         | R/W | Wakeup interrupt request enable  
  0: WKP0 interrupt requests disabled  
  1: WKP0 interrupt requests enabled |

• **IWPR**  Wakeup interrupt request register  
  Address: H'FFF9

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Set Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0   | IWPF0    | 0         | R/W | WKP0 interrupt request flag  
  [Setting condition]  
  When WKP0 pin is set as interrupt input pin, and the specified edge is detected  
  [Clearing condition]  
  When 0 is written |

### 4.4 Constants Used

No constants are used in this sample task.

### 4.5 RAM Usage

Table 3 describes RAM usage in this sample task.

#### Table 3  RAM Usage

<table>
<thead>
<tr>
<th>Label</th>
<th>Description</th>
<th>Amount of Memory Used</th>
<th>Used in</th>
</tr>
</thead>
</table>
| wkp0_f | Indicates that WKP0 interrupt has been generated. Performs main program control.  
  0: Not generated  
  1: Generated | 1 byte | main, int_wkp0 |
5. Flowcharts

5.1 main

```
main

SP = H'FF80

set_ccr(H'80)

P93 = 1

PCR93 = 1

counter = H'0000

wkp0_f = 0

WKEGS0 = 0
WKP0 = 1
IWPF0 = 0
IENWP = 1

set_imask_ccr(0)

wkp0_f = 1 ?

Yes

counter++

No

counter != 0 ?

Yes

P93 = ~P93~

No

Port setting
• Set P93 to 1 output

CCR I-bit = 1 (interrupts disabled)

WKP interrupt settings
• Select falling edge
• Select WKP0 pin
• Clear WKP0 interrupt request
• Enable WKP interrupts

CCR I-bit = 0 (interrupts enabled)

Clear counter

Clear main program control flag

Invert P93 output

Increment counter
```
5.2 int_wkp0

int_wkp0

IWF0 = 0

--- Clear IWF0 to 0

wp0_f = 1

--- Clear main program control flag

IENWP = 0

--- Clear IENWP to 0

RTE

- Link Address Specifications

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'0000</td>
</tr>
<tr>
<td>CV2</td>
<td>H'0016</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
<tr>
<td>B</td>
<td>H'F780</td>
</tr>
</tbody>
</table>
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Sep.16.04</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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