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Renesas Electronics Corporation

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H8/300H SLP Series

Count Start by the WKP Interrupt

Introduction

Turning on switch input connected to a WKP pin generates a WKP interrupt and starts incrementing of a 16-bit counter set in a 2-byte variable (“counter”).

Target Device

H8/38076R

Contents

1. Specifications

1. Turning on switch input connected to the $\overline{\text{WKP0}}$ pin generates a WKP interrupt and starts incrementing of a 16-bit counter set in a 2-byte variable (“counter”).
2. A WKP interrupt is requested by falling edge detection of $\overline{\text{WKP0}}$ pin input.
3. Incrementing of the 16-bit counter set in the 2-byte variable (“counter”) is started in WKP interrupt processing.
4. An LED is switched on and off each time the 16-bit counter set in the 2-byte variable (“counter”) overflows.
5. The LED is connected to the P93 output pin of port 9.
6. A sample connection diagram is shown in figure 1.

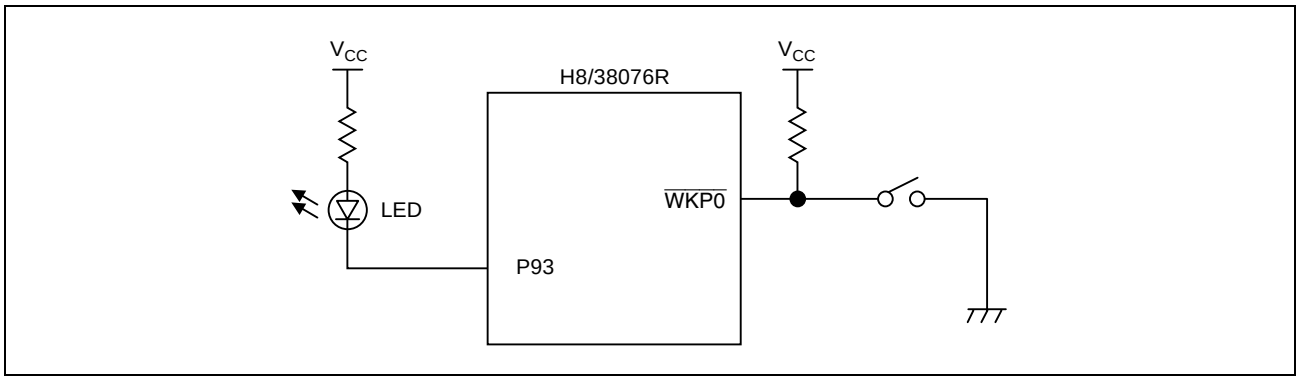


Figure 1 Example of Connections for This Sample Task

2. Functions Used

2.1 Functions

In this sample task, a count is started by means of a WKP interrupt. A block diagram of count starting using a WKP interrupt is shown in figure 2.

- Wakeup edge select register (WEGR)

  Selects the edge sensing direction that generates $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pin interrupts. In this sample task, a WKP interrupt is requested on detection of a falling edge of $\overline{\text{WKP0}}$ pin input.

- Port mode register 5 (PMR5)

  Controls switching of port 5 pin functions. The $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pins also function as port 5 pins. To use these pins as $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pins, bits $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ must be set to 1.

- Wakeup interrupt request register (IWPR)

  The $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pin interrupt request status flag register. A bit is set to 1 when the $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pins are set as input pins and a specified edge is detected.

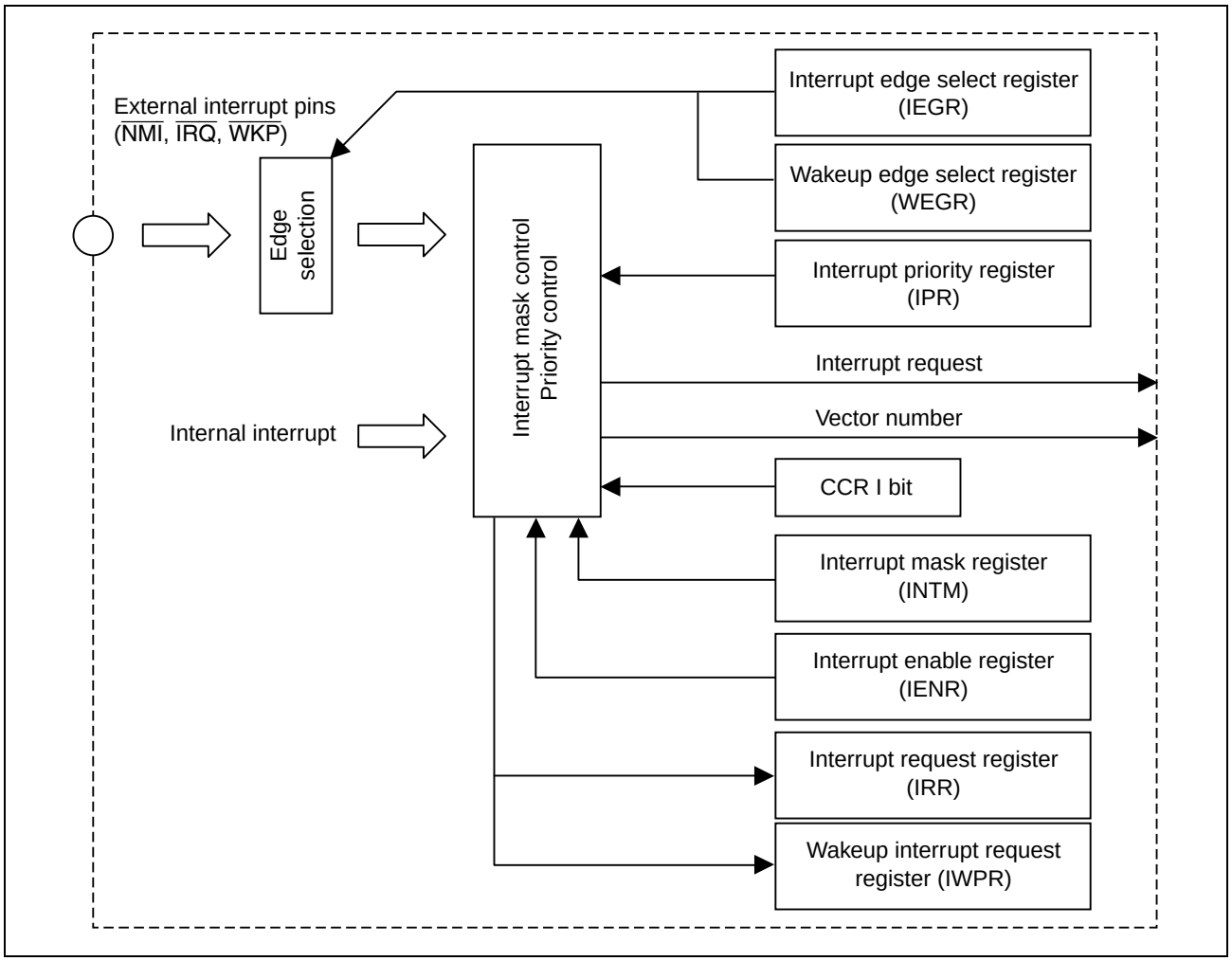


Figure 2 Block Diagram of Interrupt Controller

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, counter incrementing is performed by means of WKP interrupts.

Table 1 Assignment of Functions

Elements	Description
WEGR	$\overline{\text{WKP}}$ pin input edge selection
IENR1	Enables $\overline{\text{WKP}}$ pin interrupt requests
IWPR	WKP interrupt request flag
WKP0	$\overline{\text{WKP0}}$ interrupt input pin
PMR5	$\overline{\text{WKP}}$ pin/port selection

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, counter incrementing is performed by means of WKP interrupts.

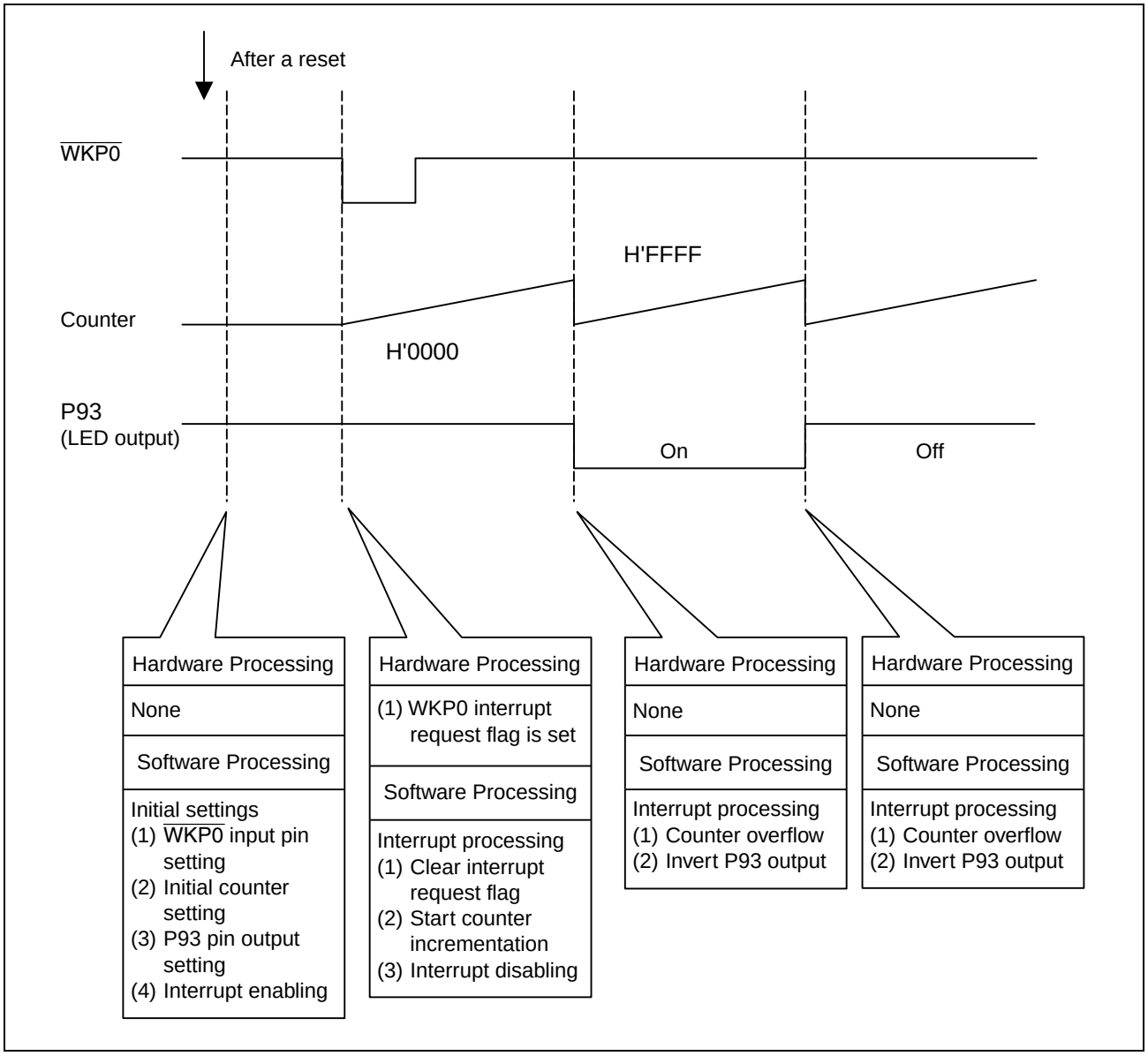


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	WKP0 interrupt setting, sets P93 as output pin, outputs 1 (LED off) After WKP0 interrupt generation, inverts P93 output due to counter overflow
int_wkp0	WKP0 interrupt processing, WKP0 interrupt request flag clearing, WKP0 interrupt disabling

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- WEGR Wakeup edge select register Address: H'FF90

Bit	Bit Name	Set Value	R/W	Description
0	WEGS0	0	R/W	Wakeup edge select 0: $\overline{\text{WKP0}}$ pin input falling edge detected

- PMR5 Port mode register 5 Address: H'FFC4

Bit	Bit Name	Set Value	R/W	Description
0	WKP0	1	R/W	P50/$\overline{\text{WKP0}}$/SEG1 pin function switching When P50/$\overline{\text{WKP0}}$/SEG1 pin is not used as SEG1 pin, sets whether it is to be used as P50 pin or as $\overline{\text{WKP0}}$ pin. 1: Functions as $\overline{\text{WKP0}}$ input pin

- PDR9 Port data register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	1	R/W	P93 data register Register that stores P93 data. If P93 is read while PCR93 bit is set to 1, the value stored in P93 is read, regardless of the actual pin state. If P93 is read while PCR93 bit is cleared to 0, the pin state are read.

- PCR9 Port control register 9 Address: H'FFEC

Bit	Bit Name	Set Value	R/W	Description
3	PCR93	1	W	P93 control register Controls P93 input/output. P93 is an output pin when PCR93 is set to 1, and an input pin when PCR93 is cleared to 0. This is a write-only register, and will always return a value of 1 if read.

- IENR1 Interrupt enable register 1 Address: H'FFF3

Bit	Bit Name	Set Value	R/W	Description
5	IENWP	1	R/W	Wakeup interrupt request enable 0: WKP0 interrupt requests disabled 1: WKP0 interrupt requests enabled

- IWPR Wakeup interrupt request register Address: H'FFF9

Bit	Bit Name	Set Value	R/W	Description
0	IWPF0	0	R/W	WKP0 interrupt request flag [Setting condition] When WKP0 pin is set as interrupt input pin, and the specified edge is detected [Clearing condition] When 0 is written

4.4 Constants Used

No constants are used in this sample task.

4.5 RAM Usage

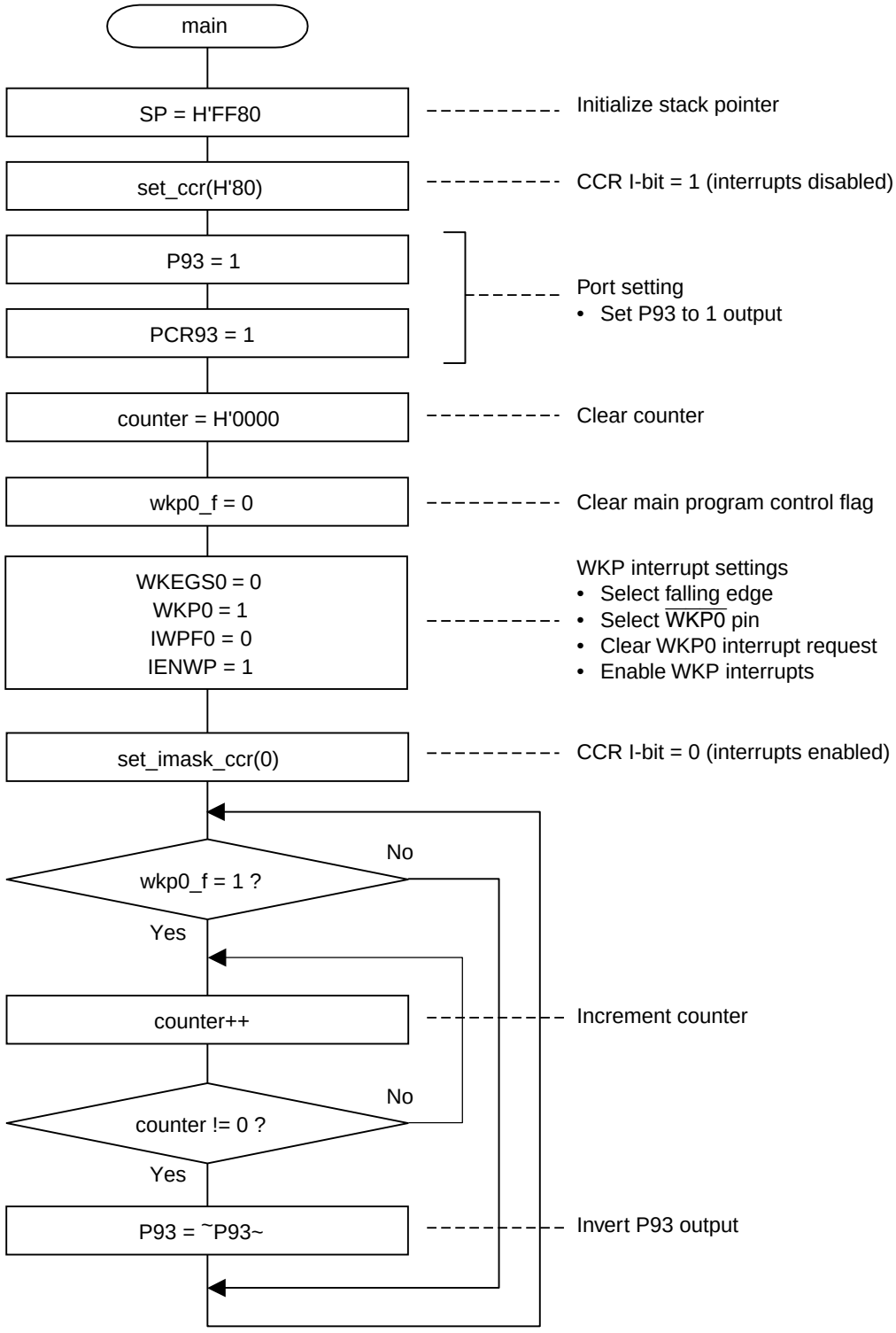
Table 3 describes RAM usage in this sample task.

Table 3 RAM Usage

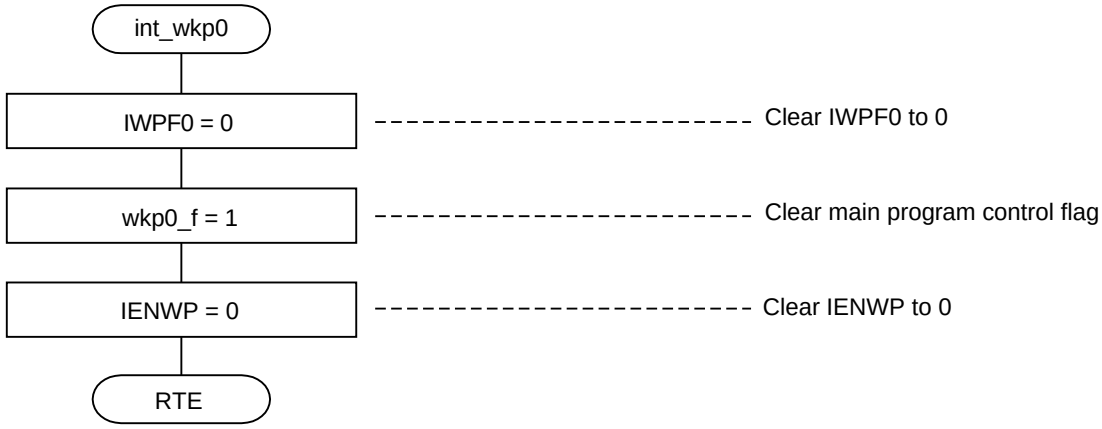
Label	Description	Amount of Memory Used	Used in
wkp0_f	Indicates that WKP0 interrupt has been generated. Performs main program control. 0: Not generated 1: Generated	1 byte	main, int_wkp0

5. Flowcharts

5.1 main



5.2 int_wkp0



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'0016
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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