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H8/300H SLP Series

Count Start by the IRQ Interrupt

Introduction

A change in an external signal is identified using the external interrupt function, and incrementing of a 16-bit counter is started.

Target Device

H8/38076R

Contents

1. Specifications

1. Turning on switch input connected to the $\overline{\text{IRQ0}}$ pin generates an IRQ interrupt and starts incrementing of a 16-bit counter set in a variable (“counter”).
2. An IRQ0 interrupt is requested by falling edge detection of $\overline{\text{IRQ0}}$ pin input.
3. An LED is switched on and off each time the 16-bit counter set in the variable (“counter”) overflows.
4. The LED is connected to the P93 output pin of port 9.
5. A sample connection diagram is shown in figure 1.

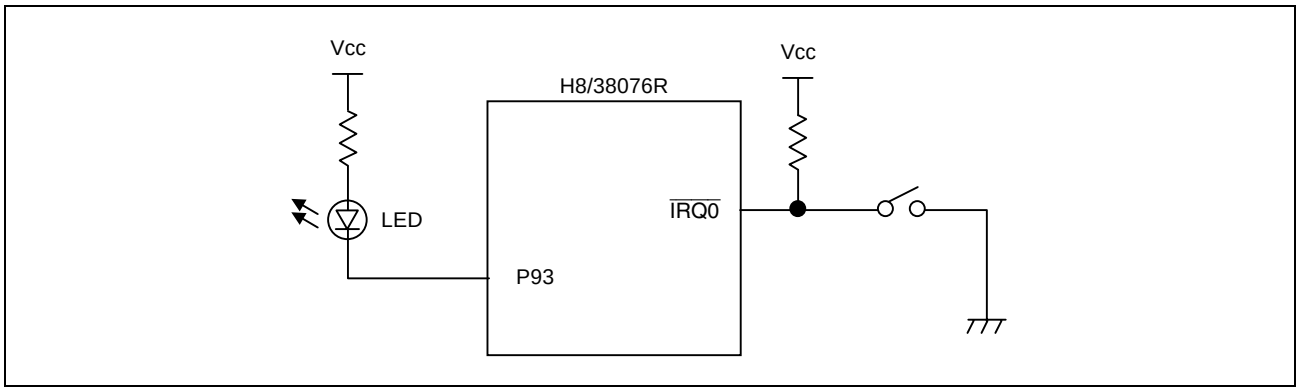


Figure 1 Example of Connections for This Sample Task

2. Functions Used

2.1 Functions

In this sample task, the external interrupt function is used to start a count by an IRQ0 external interrupt.

- There are 14 external interrupt sources: NMI, IRQ0, IRQ1, IRQ3, IRQ4, IRQAEC, and WKP0 to WKP7.
- An NMI interrupt is requested by signal input from the $\overline{\text{NMI}}$ pin. Rising/falling edge sensing can be specified for NMI interrupts by setting the NMIEG in the interrupt edge select register (IEGR).
- An NMI interrupt request has the highest priority, and is always acknowledged irrespective of the value of the I bit in CCR.
- IRQ0, IRQ1, IRQ3, and IRQ4 interrupts are requested by signals input from the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ3}}$, and $\overline{\text{IRQ4}}$ pins. Rising/falling edge sensing can be specified for IRQ0, IRQ1, IRQ3, and IRQ4 interrupts by setting IEG0, IEG1, IEG3, and IEG4 in the interrupt edge select register (IEGR).
- When a specified edge is input while the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ3}}$, and $\overline{\text{IRQ4}}$ pin functions are selected by port mode registers (PMR9, PMRB), corresponding bit IRRI0, IRRI1, IRRI3, or IRRI4 is set to 1 in interrupt flag register 1 (IRR1), and an interrupt request is generated.
- Interrupt requests can be disabled by clearing bits IEN0, IEN1, IEN3, and IEN4 to 0 in interrupt enable register 1 (IENR1).
- The interrupt priority level can be set by setting the interrupt priority register (IPR).
- A WKP interrupt is requested by signals input from one of pins $\overline{\text{WKP0}}$ to $\overline{\text{WKP7}}$. Rising/falling edge sensing can be specified for WKP interrupts by setting WKEGS0 to WKEGS7 in the wakeup edge select register (WEGR).
- When a specified edge is input while the $\overline{\text{WKP0}}$ to $\overline{\text{WKP7}}$ pin functions are selected by port mode register 5 (PMR5), corresponding bit IWPF0 to IWPF7 is set to 1 in the wakeup interrupt request register (IWPR), and an interrupt request is generated.
- Interrupt requests can be disabled by clearing IENWP to 0 in interrupt enable register 1 (IENR1).
- The interrupt priority level can be set by setting the interrupt priority register (IPR).
- An IRQAEC interrupt is input by setting IRQAEC pin input and IECPWM (AEC PWM output).
- When IRQAEC pin input is used as an external interrupt pin, ECPWME is cleared to 0 in AEGSR.
- When IRQAEC pin input is used as an external interrupt, rising-, falling-, or both-edge sensing can be specified by setting AIEGS1 and AIEGS0 in AEGSR.
- When a specified edge is input while IENEC2 is set to 1 in IENR1, the corresponding bit is set to 1 in IRR1 and an interrupt is generated.
- The interrupt priority level can be set by setting the interrupt priority register (IPR).
- The above IRQ, WKP, and IRQAEC interrupts can all be disabled by setting the I bit to 1 in the condition code register (CCR).
- Interrupt operation is described below.

  (1) When an interrupt source occurs while the corresponding bit is set to 1 in the interrupt enable register, an interrupt request signal is sent to the interrupt controller.

  (2) When interrupt request signals are sent to the interrupt controller, the interrupt with the highest level according to the interrupt levels set in IPR is selected, and lower-level interrupts are held pending.

  (3) If interrupt priority levels are the same, the higher-level interrupt request according to an order predetermined by hardware is selected.

(4) Bits INTM1 and INTM0 in the interrupt mask register (INTM), and the I bit in CRR, are referenced, and if the I bit is set to 1, interrupt requests are held pending. When the I bit is cleared to 0 and the INTM1 bit is set to 1, an interrupt of priority level 1 or below is held pending. When the I bit is cleared to 0, the INTM1 bit is cleared to 0, and the INTM0 bit is set to 1, an interrupt of priority level 0 is held pending. When the I, INTM1, and INTM0 bits are all cleared to 0, all interrupts are accepted.

(5) When an interrupt is accepted by the CPU, after the instruction being executed at that time is completed, the contents of the program counter (PC) and condition code register (CCR) are saved to a stack area. The stacked PC indicates the address of the first instruction to be executed after returning from interrupt processing.

(6) The I bit is set to 1 in CCR. This masks all interrupts except NMI and an address break.

(7) The vector address corresponding to the accepted interrupt is generated, and interrupt processing routine execution is started from the indicated address.

- Disabling interrupts by clearing the interrupt enable register, or when clearing the interrupt flag register, or clearing the interrupt flag register must be done in the interrupt masked state (I-1). If such an operation is carried out when I = 0, and conflict occurs between execution of the relevant manipulation instruction and generation of the relevant interrupt, exception handling for the generated interrupt will be executed after execution of the manipulation instruction.

- Port mode register B (PMRB)

  Sets PB0 to the $\overline{\text{IRQ0}}$ input pin function.

- Interrupt edge select register (IEGR)

  Sets the direction of an edge that generates an $\overline{\text{IRQ0}}$ pin interrupt request.

- Interrupt enable register 1 (IENR1)

  Enables $\overline{\text{IRQ0}}$ pin interrupts.

- Interrupt flag register 1 (IRR1)

  The IRQ0 interrupt request status register

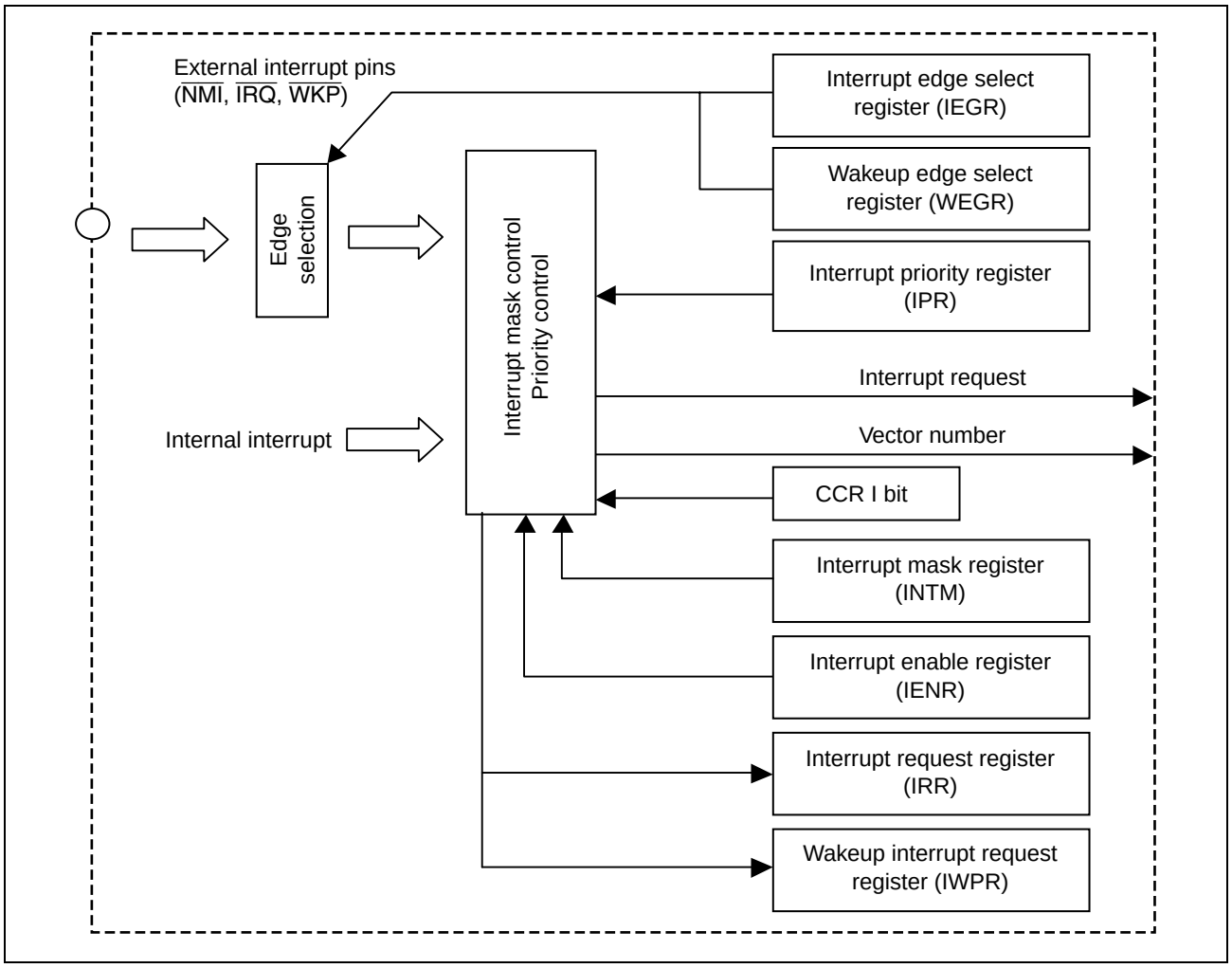


Figure 2 Block Diagram of Interrupt Controller

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, counter incrementing is performed by means of WKP interrupts.

Table 1 Assignment of Functions

Elements	Description
IEGR	$\overline{\text{IRQ0}}$ pin input edge selection
IENR1	Enables $\overline{\text{IRQ0}}$ pin interrupt requests
IRR1	IRQ0 interrupt request flag
PMRB	$\overline{\text{IRQ0}}$ pin/port selection
$\overline{\text{IRQ0}}$	$\overline{\text{IRQ0}}$ interrupt input pin

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, counter incrementing is performed by means of WKP interrupts.

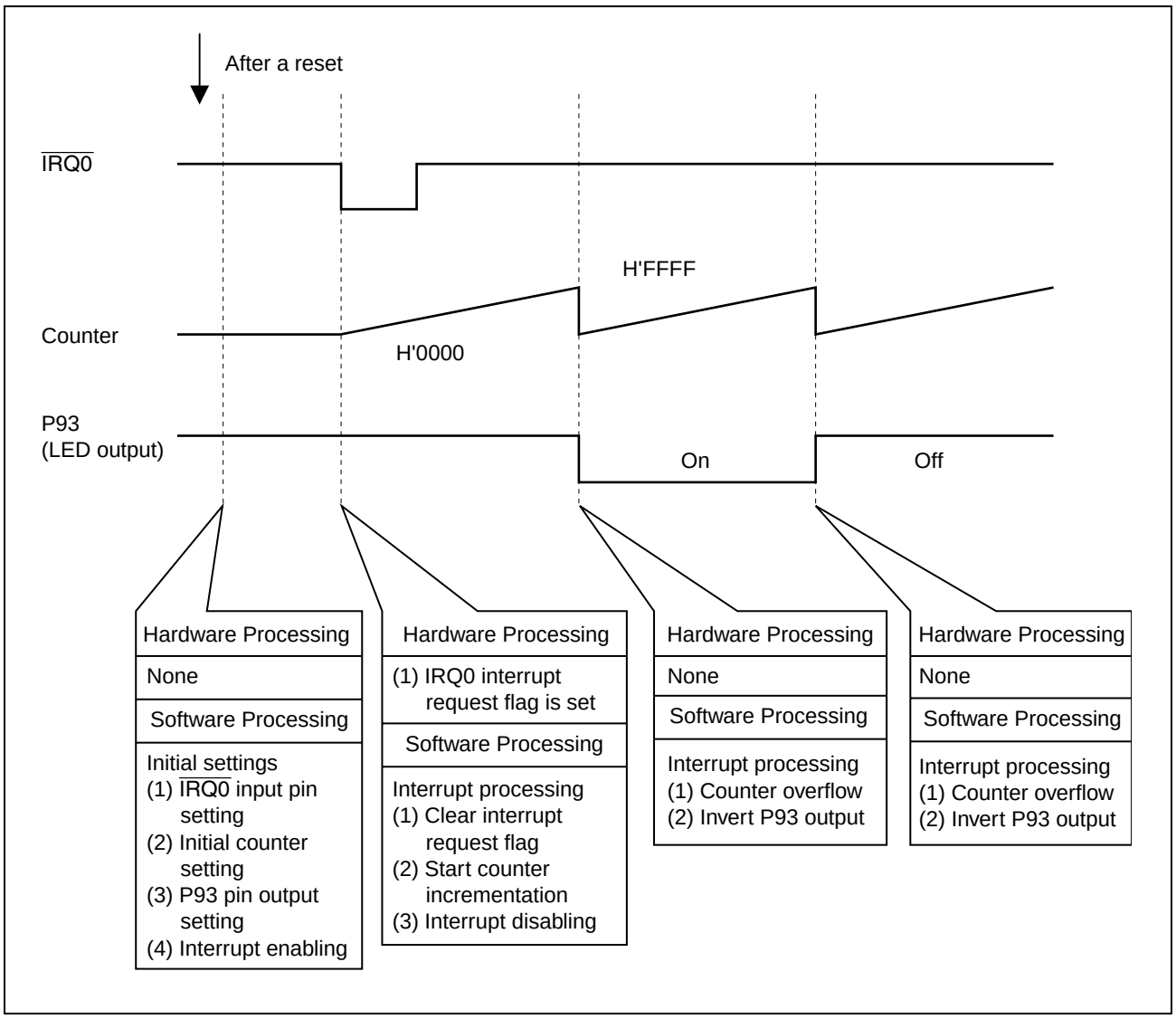


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	IRQ0 interrupt setting, sets P93 as output pin, outputs 1 (LED off) After IRQ0 interrupt generation, inverts P93 output due to counter overflow
irq0int	IRQ0 interrupt processing, clears IRRI0, disables IRQ0, and sets irq0_f to 1

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- PMRB Port mode register B Address: H'FFCA

Bit	Bit Name	Set Value	R/W	Description
0	IRQ0	1	R/W	PB0/AN0/$\overline{\text{IRQ0}}$ pin switching Sets whether PB0/AN0/$\overline{\text{IRQ0}}$ pin is to be used as PB0/AN0 pin or as $\overline{\text{IRQ0}}$ pin. 1: Functions as $\overline{\text{IRQ0}}$ input pin

- PDR9 Port data register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	1	R/W	P93 data register Register that stores P93 data. If P93 is read while PCR93 bit is set to 1, the value stored in P93 is read, regardless of the actual pin state. If P93 is read while PCR93 bit is cleared to 0, the pin state are read.

- PCR9 Port control register 9 Address: H'FFEC

Bit	Bit Name	Set Value	R/W	Description
3	PCR93	1	W	P93 control register Controls P93 input/output. P93 is an output pin when PCR93 is set to 1, and an input pin when PCR93 is cleared to 0. This is a write-only register, and will always return a value of 1 if read.

- IEGR Interrupt edge select register Address: H'FFF2

Bit	Bit Name	Set Value	R/W	Description
0	IEG0	0	R/W	IIRQ0 edge select 0: $\overline{\text{IRQ0}}$ pin input falling edge detected

- IENR1 Interrupt enable register 1 Address: H'FFF3

Bit	Bit Name	Set Value	R/W	Description
0	IEN0	1	R/W	IRQ0 interrupt request enable 0: IRQ0 interrupt requests disabled 1: IRQ0 interrupt requests enabled

- IRR1 Interrupt flag register 1 Address: H'FFF6

Bit	Bit Name	Set Value	R/W	Description
0	IRRI0	0	R/W	IRQ0 interrupt request flag [Setting condition] When $\overline{\text{IRQ0}}$ pin is set as interrupt input pin, and specified edge is detected [Clearing condition] When 0 is written to this bit

4.4 Constants Used

No constants are used in this sample task.

4.5 RAM Usage

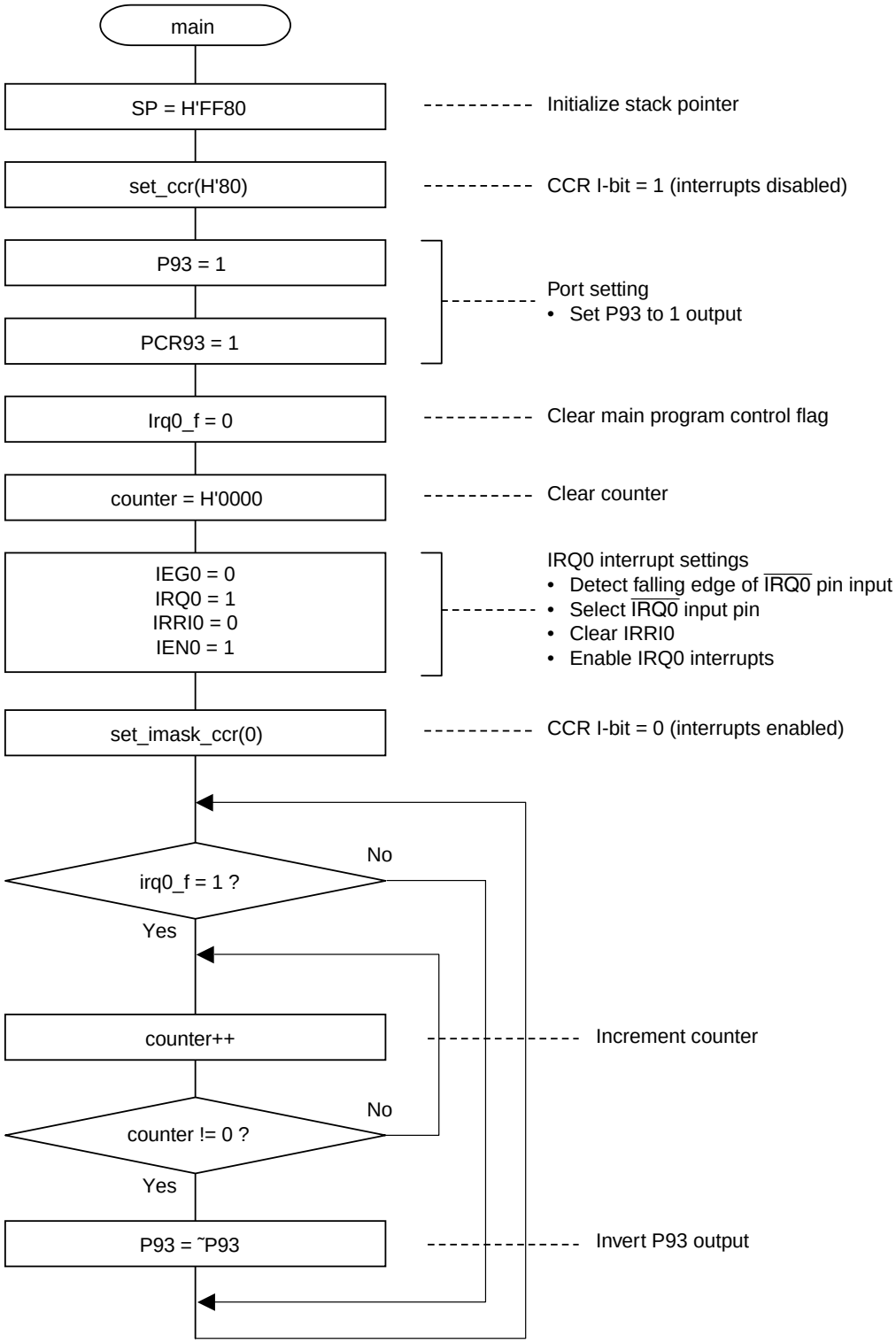
Table 3 describes RAM usage in this sample task.

Table 3 RAM Usage

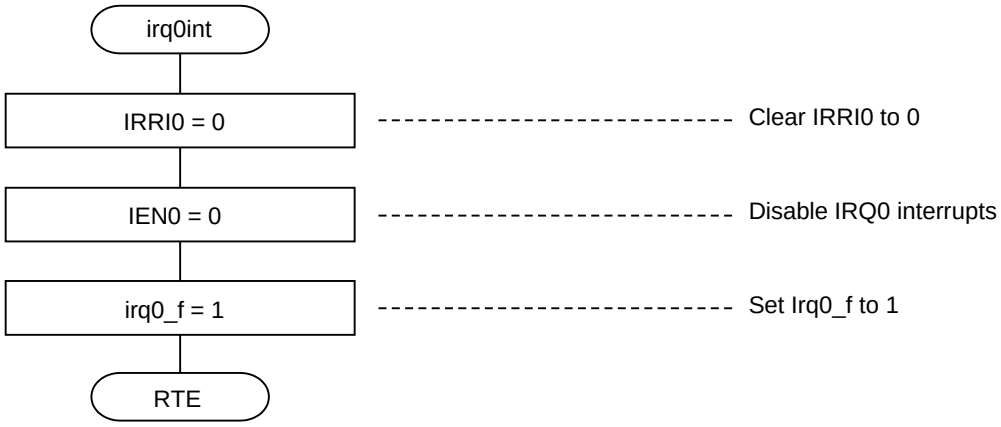
Label	Description	Amount of Memory Used	Used in
irq0_f	Indicates that IRQ0 interrupt has been generated. Performs main program control. 0: Not generated 1: Generated	1 byte	main, irq0int

5. Flowcharts

5.1 main



5.2 irq0int



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'000C
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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