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H8/300H SLP Series

Asynchronous Event Counter Operation Using the 16-Bit Mode

Introduction

The asynchronous event counter is used in the 16-bit mode to invert port output in fixed cycles. 2-MHz event input is performed at the asynchronous event input L (AEVL) pin, and P40 pin output is inverted every overflow cycle (32.768 ms) of a 16-bit event counter combining event counter H (ECH) and event counter L (ECL).

Target Device

H8/38076R

Contents

1. Specifications

- The asynchronous event counter is used in the 16-bit mode to invert the P40 pin output every fixed cycle (32.768 ms), as shown in figure 1.
- A 16-bit event counter is used in which the event counter H (ECH) input clock functions as the event counter L (ECL) overflow signal, and ECH and the ECL is incremented by means of 2-MHz event input to the asynchronous event input L (AEVL) pin.
- P40 pin output is inverted by 16-bit event counter overflow interrupt processing.
- The event input enable interrupt input (IRQAEC) pin is fixed to a high level by hardware.

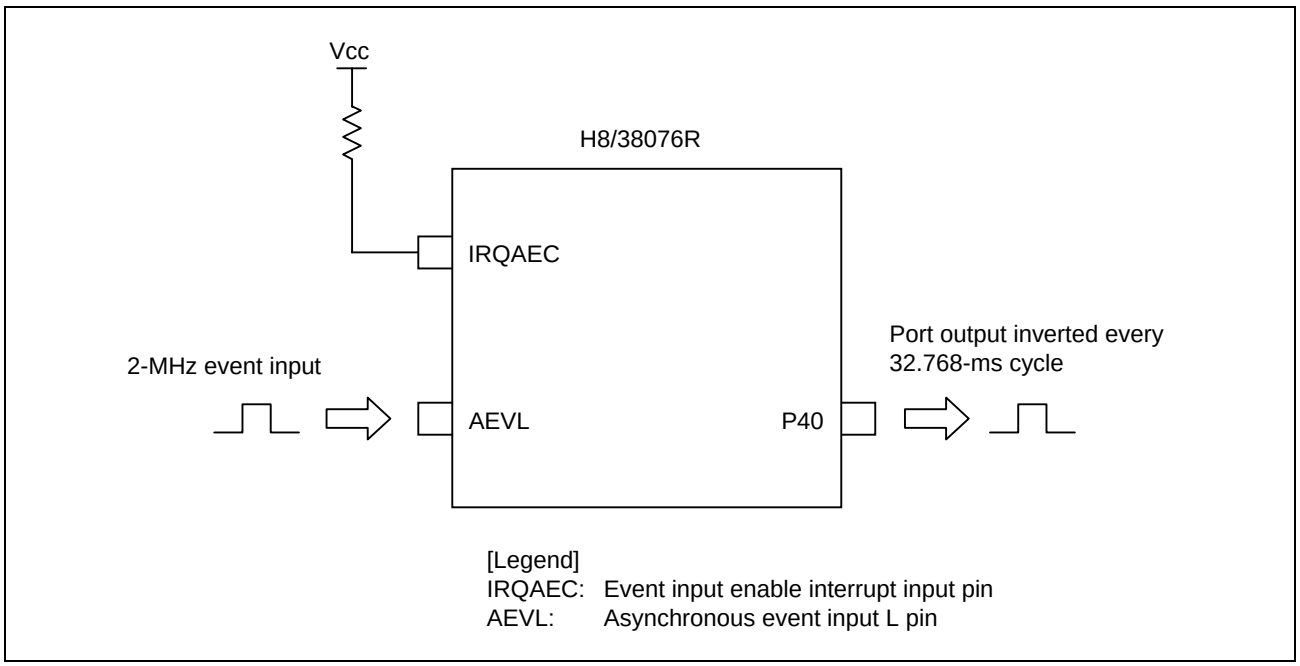


Figure 1 Example of Event Counter Operation in the 16-Bit Mode

2. Functions Used

2.1 16-Bit Mode Asynchronous Event Counter Function

In this sample task, the asynchronous event counter function is used in the 16-bit mode to invert the output of the P40 pin at every overflow cycle of the 16-bit event counter due to event input to the asynchronous event input L (AEVL) pin. A block diagram of the asynchronous event counter in the 16-bit mode is shown in figure 2. The block diagram of the asynchronous event counter in the 16-bit mode is explained below.

- System clock (ϕ)

  10-MHz clock used as the reference clock for operating the CPU and peripheral function modules
- Prescaler S (PSS)

  A 13-bit counter with ϕ as input, incremented every cycle
- Input pin edge select register (AEGSR)

  Performs asynchronous event input L (AEVL) pin input edge sense detection selection, event counter PWM operation control and IRQAEC selection
- Event counter control register (ECCR)

  Selects event counter L (ECL) input clock.
- Event counter control/status register (ECCSR)

  Detects event counter H (ECH) overflow, selects event counter usage, enables/disables ECH and ECL input event clock input control, and controls ECH and ECL reset.
- Event counter H (ECH)

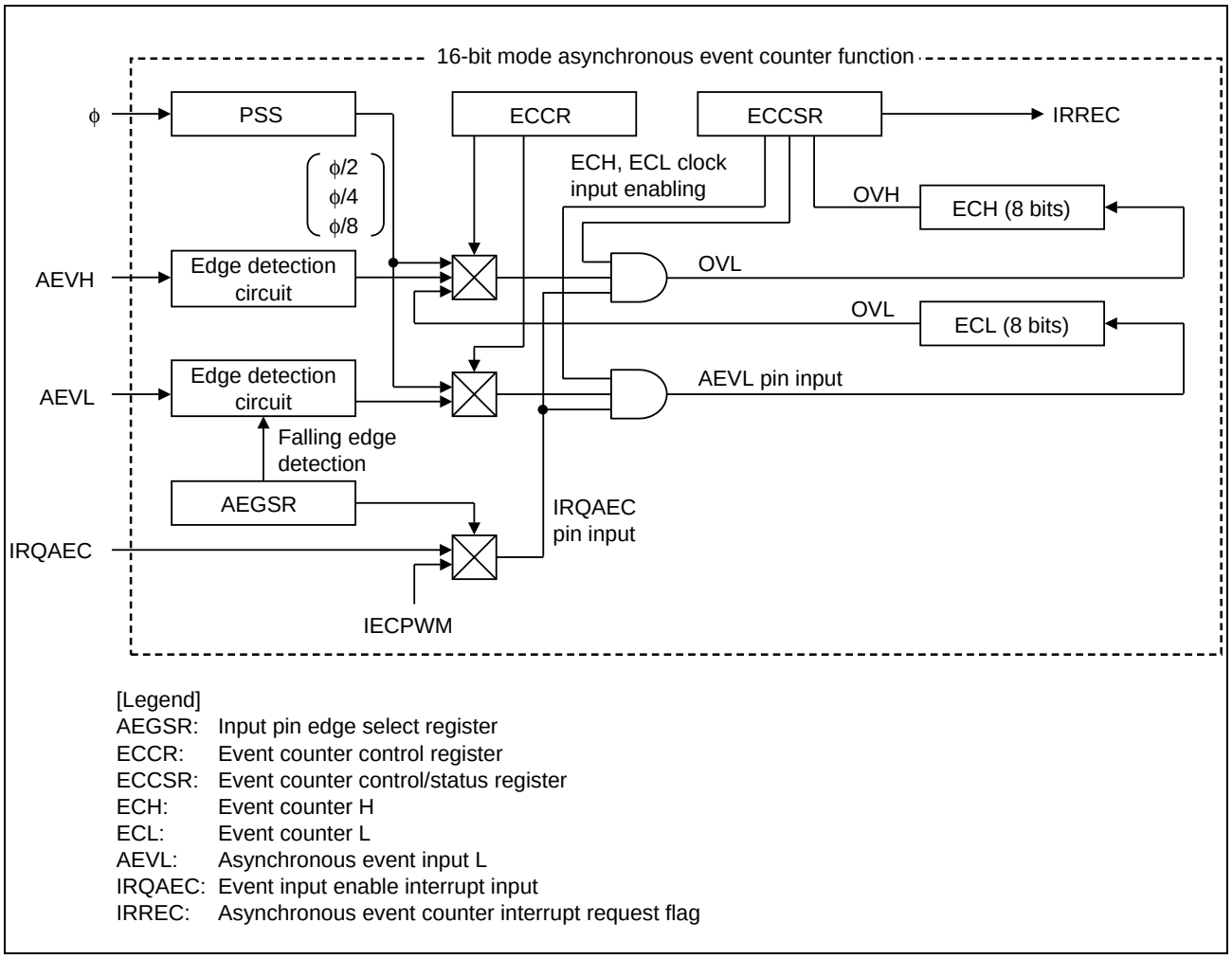
  Operates as the upper 8-bit up-counter of the 16-bit event counter formed in combination with ECL.
- Event counter L (ECL)

  Operates as the lower 8-bit up-counter of the 16-bit event counter formed in combination with ECH.
- Asynchronous event input L (AEVL) pin

  Event input pin for input to event counter L (ECL)
- Event input enable interrupt input (IRQAEC) pin

  Interrupt enable pin that enables event input
- Asynchronous event counter interrupt request (IRREC)

  Interrupt request generated by overflow of 16-bit event counter



[Legend]
AEGSR: Input pin edge select register
ECCR: Event counter control register
ECCSR: Event counter control/status register
ECH: Event counter H
ECL: Event counter L
AEVL: Asynchronous event input L
IRQAEC: Event input enable interrupt input
IRREC: Asynchronous event counter interrupt request flag

Figure 2 Block Diagram of the 16-Bit Mode Asynchronous Event Counter Function

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, P40 pin output is inverted every 16-bit event counter overflow cycle by means of the 16-bit mode asynchronous event counter function.

Table 1 Assignment of Functions

Elements	Description
AEGSR	Sets falling edge detection for the AEVL pin, and halts of event counter PWM operation and IRQAEC.
ECCR	Sets AEVL pin event input as ECL input clock.
ECCSR	Sets ECH overflow detection, and ECH and ECL as single-channel 16-bit event counter, enables ECH and ECL event clock input, and controls ECH and ECL reset.
ECH	8-bit up-counter using ECL overflow signal as input clock
ECL	8-bit up-counter using AEVL pin event input as input clock
AEVL pin	Event input pin performing 2-MHz event input
IRQAEC pin	High level is input to enable ECH and ECL event input.
IRREC	ECH overflow interrupt request, in interrupt processing of which P40 pin output is inverted
IENEC	Enables IRREC interrupt request.
P40 pin	Output is inverted every ECH overflow interrupt cycle.
PDR4	Used to set P40 pin output data.
PCR4	Sets P40 pin to output.
PMR1	Sets P11/AEVL pin to AEVL input.

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. By means of the hardware and software processing shown in figure 3, the asynchronous event counter function is used in 16-bit mode to invert the output of the P40 pin every 16-bit event counter overflow cycle.

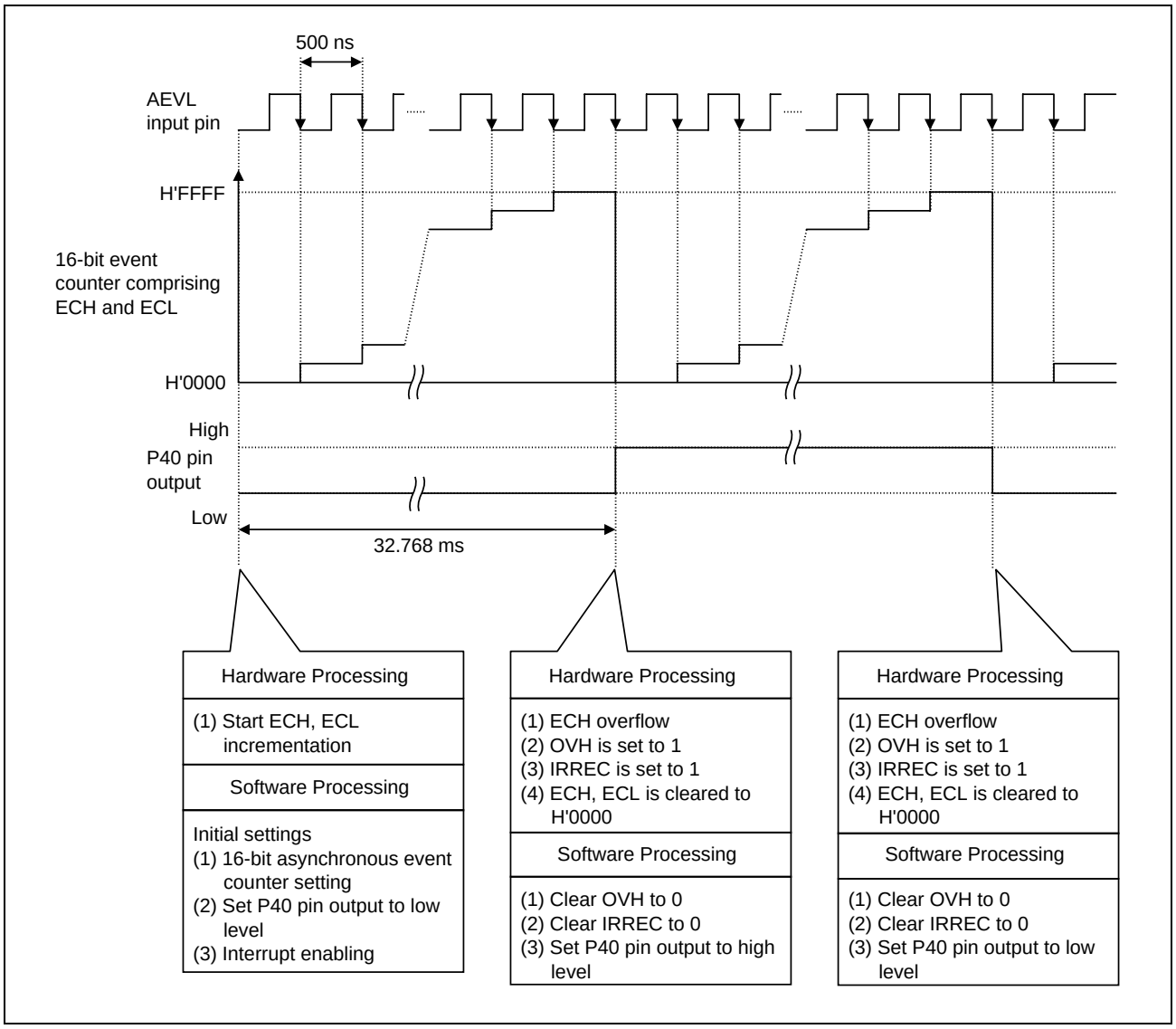


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	16-bit mode asynchronous event counter setting, P40 pin output setting, asynchronous event counter interrupt request enabling
int_aec	Asynchronous event counter interrupt request flag clearing, P40 pin output inversion

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- AEGSR Input pin edge select register Address: H'FF92

Bit	Bit Name	Set Value	R/W	Description
5	ALEGS1	0	R/W	AEC edge select L
4	ALEGS0	0		Selects AEVL pin edge detection. ALEGS1 = 0, ALEGS0 = 0: AEVL pin falling edge detected
1	ECPWME	0	R/W	Event counter PWM enable Controls event counter PWM operation and selects IRQAEC. ECPWME = 0: AEC PWM operation halts and IRQAEC selected

- ECCR Event counter control register Address: H'FF94

Bit	Bit Name	Set Value	R/W	Description
5	ACKL1	0	R/W	AEC clock select L
4	ACKL0	0		Selects clock used by ECL. ACKL1 = 0, ACKL0 = 0: AEVL pin input

- ECCSR Event counter control/status register Address: H'FF95

Bit	Bit Name	Set Value	R/W	Description
7	OVH	0	R/W*	Counter overflow H Status flag indicating that ECH has overflowed [Setting condition] When ECH value changes from H'FF to H'00 [Clearing condition] When 0 is written to OVH after reading 1 from OVH
4	CH2	0	R/W	Channel select Selects how ECH and ECL event counters are used CH2 = 0: ECH and ECL used as single-channel 16-bit event counter
3	CUEH	1	R/W	Count-up enable H Enables/disables event clock input to ECH. CUEH = 1: ECH event clock input enabled

Note: * Only a 0 write for flag clearing is possible.

- ECCSR Event counter control/status register Address: H'FF95

Bit	Bit Name	Set Value	R/W	Description
2	CUEL	1	R/W	Count-up enable L Enables/disables event clock input to ECL. CUEL = 1: ECL event clock input enabled
0	CRCH	1	R/W	Counter reset control H Controls ECH reset. CRCH = 1: ECH reset cleared and up-count function enabled
0	CRCL	1	R/W	Counter reset control L Controls ECL reset. CRCL = 1: ECL reset cleared and up-count function enabled

- ECH Event counter H Address: H'FF96

  ECH is an 8-bit readable up-counter that operates as an independent 8-bit event counter. ECH also operates as the upper 8-bit up-counter of a 16-bit event counter formed in combination with ECL.

Bit	Bit Name	Set Value	R/W	Description
7	ECH7	0	R	Either the external asynchronous event AEVH pin, $\phi/2$, $\phi/4$, or $\phi/8$ can be selected as the input clock source. ECH can be cleared to H'00 by software.
6	ECH6	0	R	
5	ECH5	0	R	
4	ECH4	0	R	
3	ECH3	0	R	
2	ECH2	0	R	
1	ECH1	0	R	
0	ECH0	0	R	

- ECL Event counter L Address: H'FF97

ECL is an 8-bit readable up-counter that operates as an independent 8-bit event counter. ECL also operates as the lower 8-bit up-counter of a 16-bit event counter formed in combination with ECH.

Bit	Bit Name	Set Value	R/W	Description
7	ECL7	0	R	Either the external asynchronous event AEVL pin, $\phi/2$, $\phi/4$, or $\phi/8$ can be selected as the input clock source. ECL can be cleared to H'00 by software.
6	ECL6	0	R	
5	ECL5	0	R	
4	ECL4	0	R	
3	ECL3	0	R	
2	ECL2	0	R	
1	ECL1	0	R	
0	ECL0	0	R	

- IRR2 Interrupt flag register 2 Address: H'FFF7

Bit	Bit Name	Set Value	R/W	Description
0	IRREC	0	R/W	Asynchronous event counter interrupt request flag [Setting condition] When asynchronous event counter overflows [Clearing condition] When 0 is written to the bit

- IENR2 Interrupt enable register 2 Address: H'FFF4

Bit	Bit Name	Set Value	R/W	Description
0	IENEC	1	R/W	Asynchronous event counter interrupt enable When this bit is set to 1, asynchronous event counter interrupt requests are enabled.

- PDR4 Port data register 4 Address: H'FFD7

Bit	Bit Name	Set Value	R/W	Description
0	P40	0	R/W	Port data register 40 Stores P40 data. If port 4 is read while PCR4 bits are set to 1, the values stored in PDR4 are read, regardless of the actual pin states. If port 4 is read while PCR4 bits are cleared to 0, the pin states are read.

- PCR4 Port control register 4 Address: H'FFE7

Bit	Bit Name	Set Value	R/W	Description
0	PCR40	1	W	Port control register 40 Controls P40 input/output. P40 is an output pin when PCR40 is set to 1, and an input pin when PCR40 is cleared to 0. PCR40 is a write-only bit. This bit is always read as 1.

- PMR1 Port mode register 1 Address: H'FFC0

Bit	Bit Name	Set Value	R/W	Description
1	AEVL	1	R/W	P11/AEVL pin function switching Sets whether P11/AEVL pin is to be used as P11 pin or as AEVL pin. AEVL = 1: Functions as AEVL input pin

4.4 Constants Used

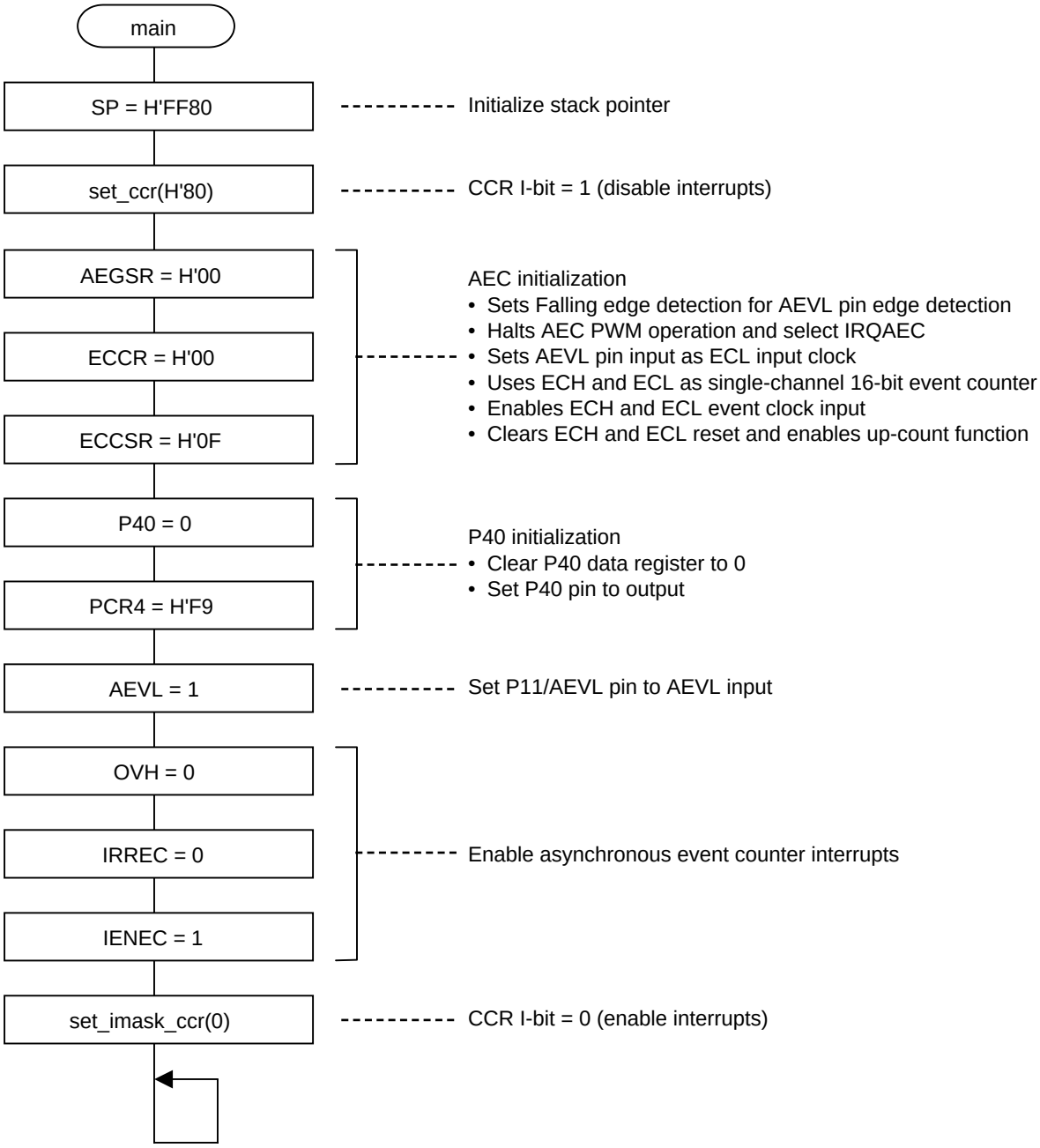
No constants are used in this sample task.

4.5 RAM Usage

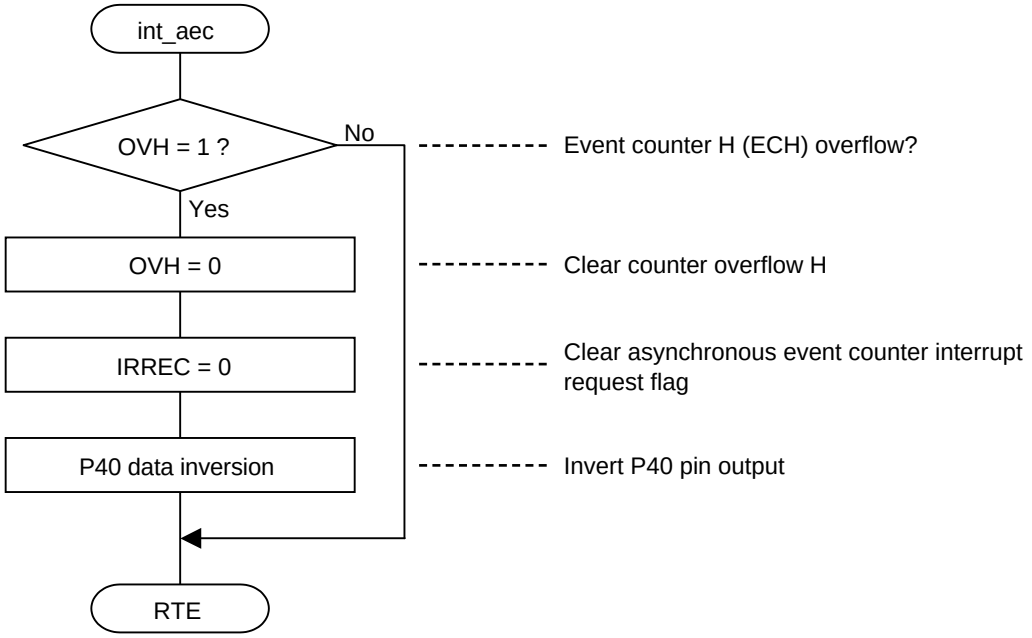
No RAM is used in this sample task.

5. Flowcharts

5.1 main



5.2 int_aec



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'0038
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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