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Renesas Electronics Corporation

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H8/300H SLP Series

AEC Interval Timer Operation Using the 8-Bit Mode

Introduction

The asynchronous event counter is used as an interval timer in the 8-bit mode to invert port output in fixed cycles. P40 pin output is inverted every 8-bit event counter L (ECL) overflow cycle (102.4 µs).

Target Device

H8/38076R

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1. Specifications

- The asynchronous event counter is used as an interval timer in the 8-bit mode to invert P40 pin output in fixed cycles (102.4 µs), as shown in figure 1.
- Event counter L (ECL) is used as an independent event counter, and the ECL is incremented by means of internal clock ϕ/4.
- P40 pin output is inverted by ECL overflow interrupt processing.
- The event input enable interrupt input (IRQAEC) pin is fixed to a high level by hardware.

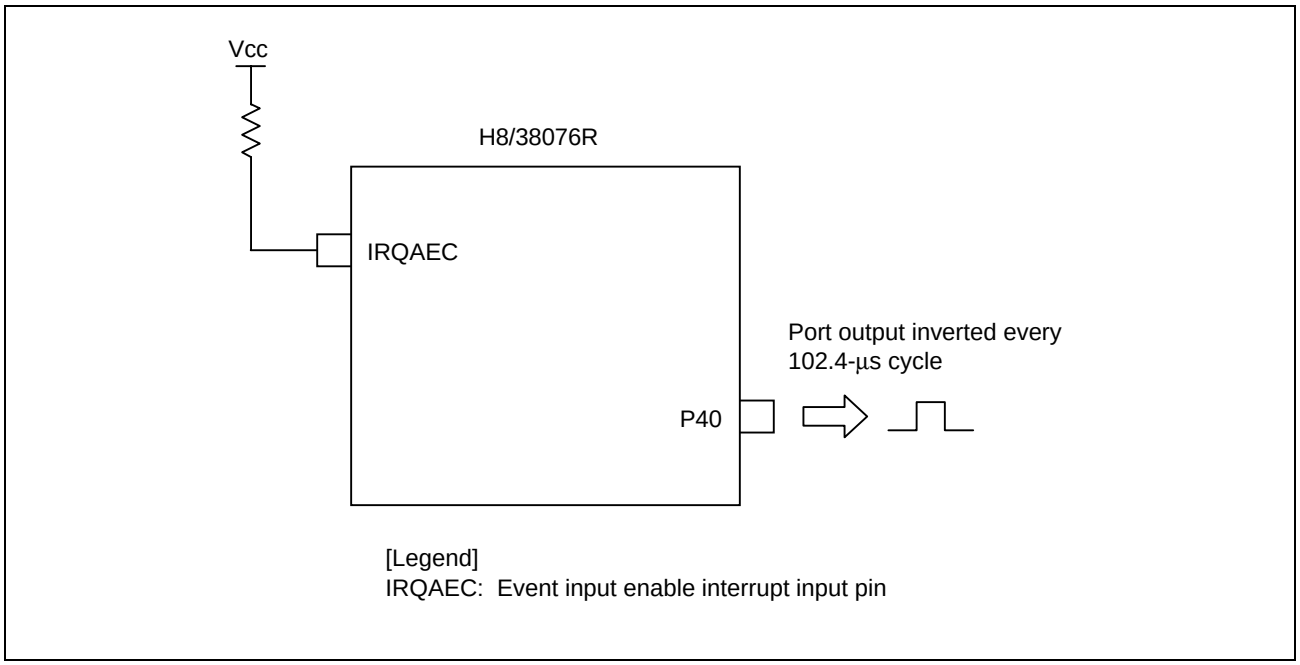


Figure 1 Example of AEC Interval Timer Operation in the 8-Bit Mode

2. Functions Used

2.1 8-Bit Mode Asynchronous Event Counter Function

In this sample task, the asynchronous event counter function is used in 8-bit mode to invert the output of the P40 pin every event counter L (ECL) overflow cycle based on internal clock ϕ/4. A block diagram of the asynchronous event counter in the 8-bit mode is shown in figure 2. The block diagram of the asynchronous event counter in the 8-bit mode is explained below.

- System clock (ϕ)

  10-MHz clock used as the reference clock for operating the CPU and peripheral functions
- Prescaler S (PSS)

  A 13-bit counter with ϕ as input, incremented every cycle
- Input pin edge select register (AEGSR)

  Performs event counter PWM operation and selects IRQAEC
- Event counter control register (ECCR)

  Selects event counter L (ECL) input clock.
- Event counter control/status register (ECCSR)

  Detects event counter L (ECL) overflow, selects event counter usage, enables/disables ECL input event clock input control, and controls ECL reset.
- Event counter L (ECL)

  An 8-bit readable up-counter that operates as an independent 8-bit counter.
- Asynchronous event input L (AEVL) pin

  Event input pin for input to event counter L (ECL)
- Event input enable interrupt input (IRQAEC) pin

  Interrupt enable pin that enables event input
- Asynchronous event counter interrupt request (IRREC)

  Interrupt request generated by overflow of event counter L (ECL)

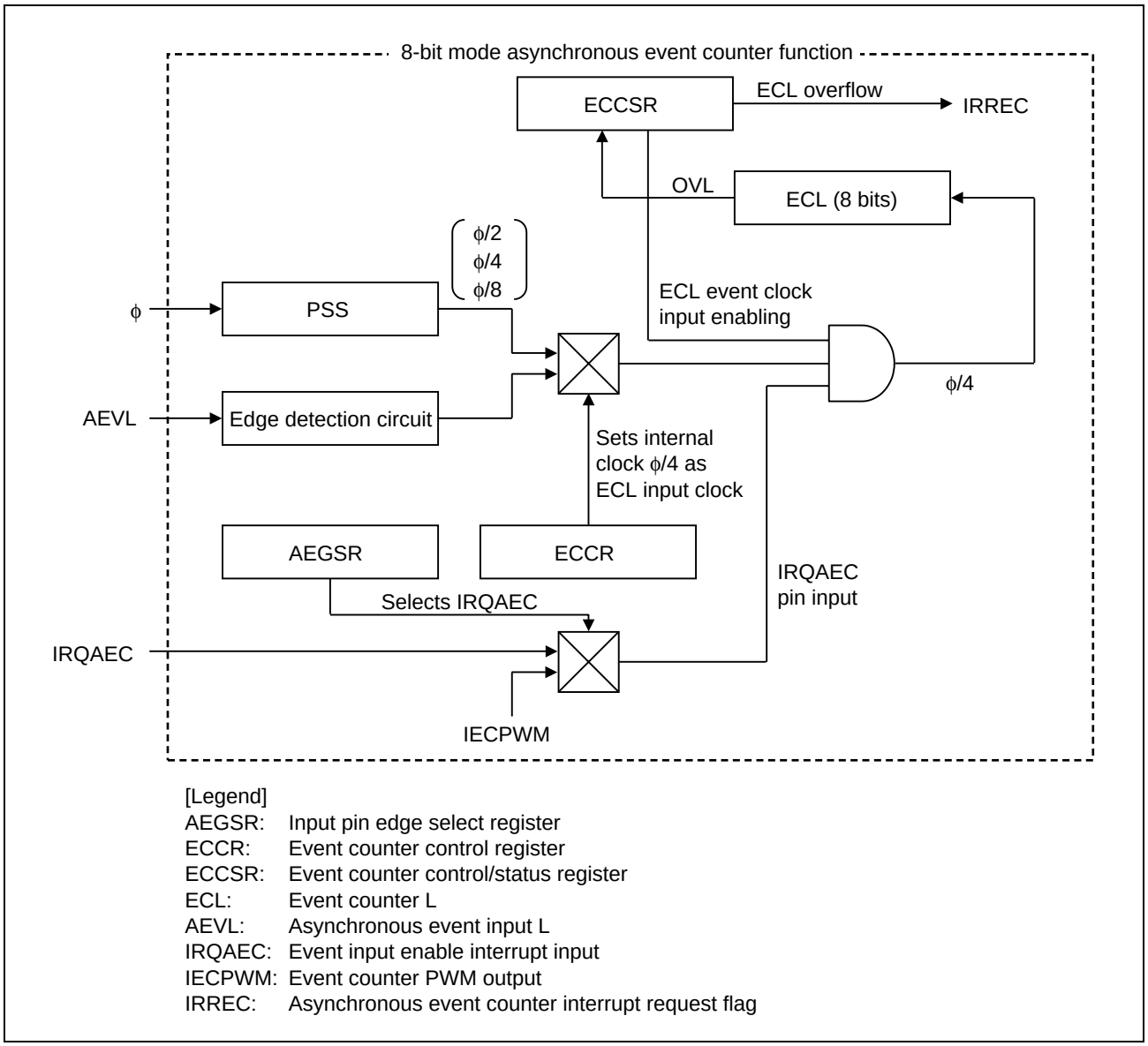


Figure 2 Block Diagram of the 8-Bit Mode Asynchronous Event Counter Function

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, P40 pin output is inverted every internal clock φ/4 based event counter L (ECL) overflow cycle by means of the 8-bit mode asynchronous event counter function.

Table 1 Assignment of Functions

Elements	Description
AEGSR	Halts event counter PWM operation and selects IRQAEC.
ECCR	Sets internal clock φ/4 as ECL input clock.
ECCSR	Sets ECL overflow detection, and ECL as independent 8-bit event counter, enables ECL event clock input, and controls ECL reset.
ECL	8-bit up-counter using internal clock φ/4 as input clock
IRQAEC pin	High level is input to enable ECL event input.
IRREC	ECL overflow interrupt request, in interrupt processing of which P40 pin output is inverted
IENEC	Enables IRREC interrupt request.
P40 pin	Output is inverted every ECL overflow interrupt cycle.
PDR4	Used to set P40 pin output data.
PCR4	Sets P40 pin to output.

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. By means of the hardware and software processing shown in figure 3, the asynchronous event counter function is used in the 8-bit mode to invert the output of the P40 pin every internal clock ϕ/4 based event counter L (ECL) overflow cycle.

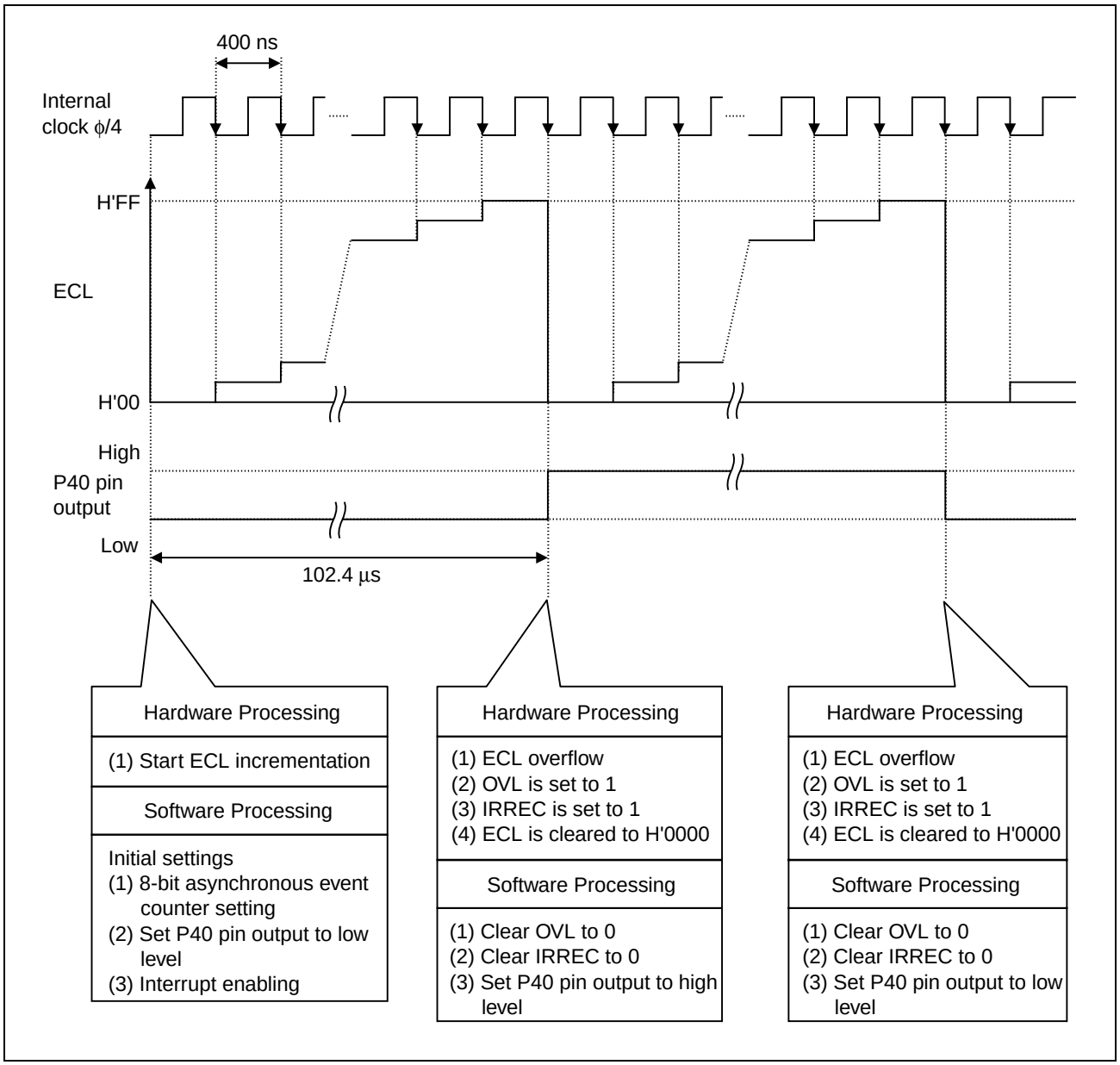


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	8-bit mode asynchronous event counter setting, P40 pin output setting, asynchronous event counter interrupt request enabling
int_aec	Asynchronous event counter interrupt request flag clearing, P40 pin output inversion

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- AEGSR Input pin edge select register Address: H'FF92

Bit	Bit Name	Set Value	R/W	Description
1	ECPWME	0	R/W	Event counter PWM enable Controls event counter PWM operation and selects IRQAEC. ECPWME = 0: AEC PWM operation halts and IRQAEC selected

- ECCR Event counter control register Address: H'FF94

Bit	Bit Name	Set Value	R/W	Description
5	ACKL1	1	R/W	AEC clock select L
4	ACKL0	0		Selects clock used by ECL. ACKL1 = 0, ACKL0 = 0: Internal clock ϕ/4

- ECCSR Event counter control/status register Address: H'FF95

Bit	Bit Name	Set Value	R/W	Description
6	OVL	0	R/W*	Counter overflow L Status flag indicating that ECL has overflowed [Setting condition] When ECL value changes from H'FF to H'00 while CH2 is set to 1 [Clearing condition] When 0 is written to OVL after reading 1 from OVL
4	CH2	1	R/W	Channel select Selects how ECH and ECL event counters are used CH2 = 1: ECH and ECL used as a 2-channel 8-bit event counter
2	CUEL	1	R/W	Count-up enable L Enables/disables event clock input to ECL. CUEL = 1: ECL event clock input enabled

Note: * Only a 0 write for flag clearing is possible.

- ECCSR Event counter control/status register Address: H'FF95

Bit	Bit Name	Set Value	R/W	Description
0	CRCL	1	R/W	Counter reset control L Controls ECL reset. CRCL = 1: ECL reset cleared and up-count function enabled

- ECL Event counter L Address: H'FF97

ECL is an 8-bit readable up-counter that operates as an independent 8-bit event counter. ECL also operates as the lower 8-bit up-counter of a 16-bit event counter formed in combination with ECH.

Bit	Bit Name	Set Value	R/W	Description
7	ECL7	0	R	Either the external asynchronous event AEVL pin, $\phi/2$, $\phi/4$, or $\phi/8$ can be selected as the input clock source. ECL can be cleared to H'00 by software.
6	ECL6	0	R	
5	ECL5	0	R	
4	ECL4	0	R	
3	ECL3	0	R	
2	ECL2	0	R	
1	ECL1	0	R	
0	ECL0	0	R	

- IRR2 Interrupt flag register 2 Address: H'FFF7

Bit	Bit Name	Set Value	R/W	Description
0	IRREC	0	R/W	Asynchronous event counter interrupt request flag [Setting condition] When asynchronous event counter overflows [Clearing condition] When 0 is written to this bit

- IENR2 Interrupt enable register 2 Address: H'FFF4

Bit	Bit Name	Set Value	R/W	Description
0	IENEC	1	R/W	Asynchronous event counter interrupt enable When this bit is set to 1, asynchronous event counter interrupt requests are enabled.

- PDR4 Port data register 4 Address: H'FFD7

Bit	Bit Name	Set Value	R/W	Description
0	P40	0	R/W	Port data register 40 Stores P40 data. If port 4 is read while PCR4 bits are set to 1, the values stored in PDR4 are read, regardless of the actual pin states. If port 4 is read while PCR4 bits are cleared to 0, the pin states are read.

- PCR4 Port control register 4 Address: H'FFE7

Bit	Bit Name	Set Value	R/W	Description
0	PCR40	1	W	Port control register 40 Controls P40 input/output. P40 is an output pin when PCR40 is set to 1, and an input pin when PCR40 is cleared to 0. PCR40 is a write-only bit. This bit is always read as 1.

4.4 Constants Used

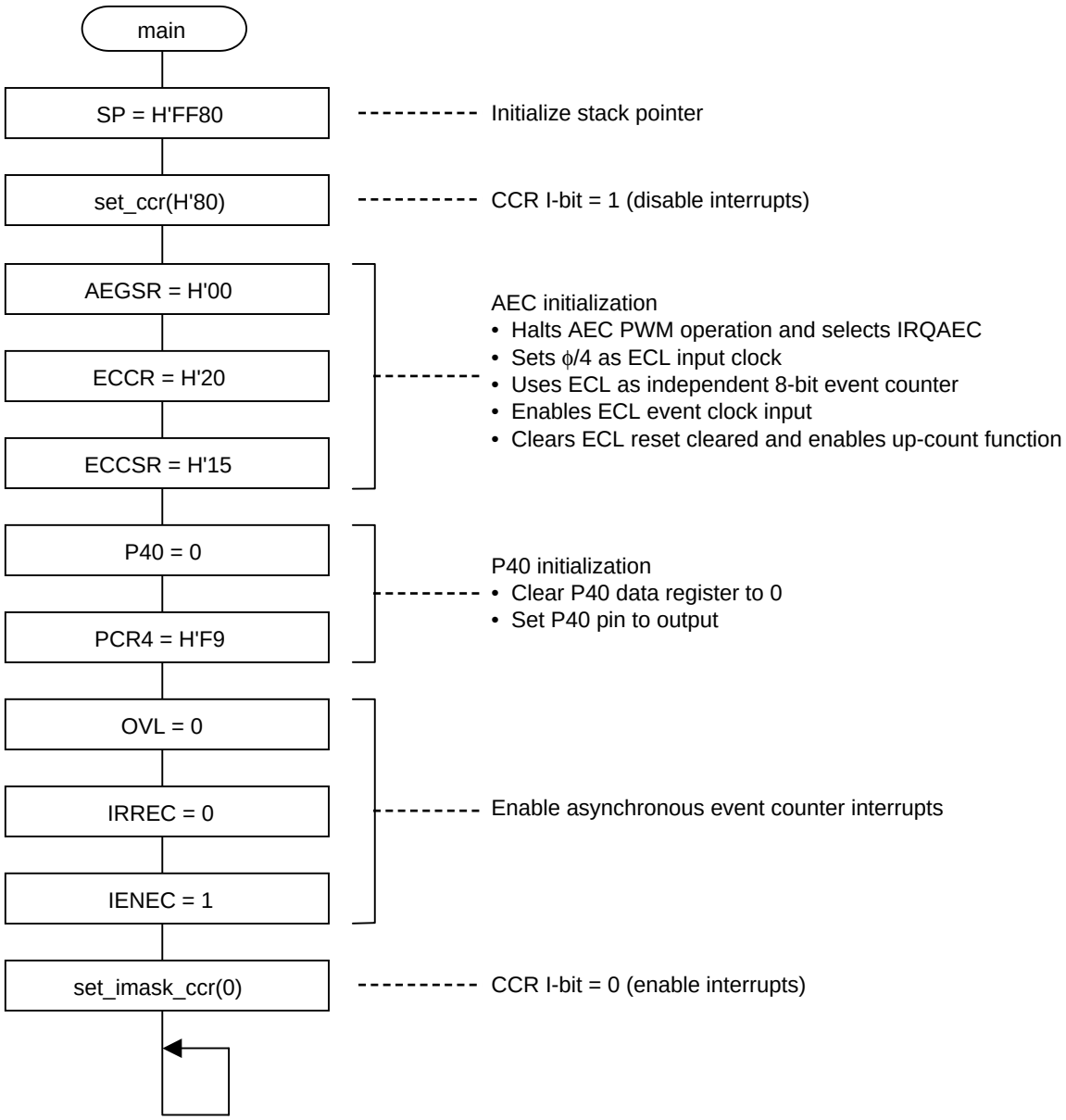
No constants are used in this sample task.

4.5 RAM Usage

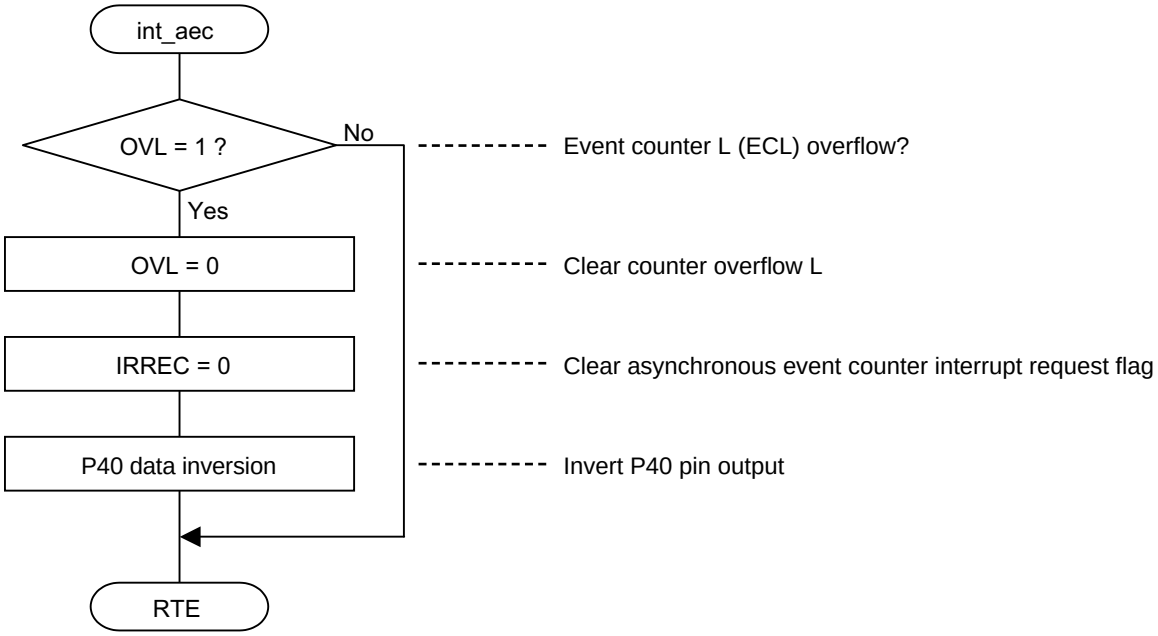
No RAM is used in this sample task.

5. Flowcharts

5.1 main



5.2 int_aec



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'0038
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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