RZ/G Series, 2nd and 3rd Generation
PCB Design Guideline for RGMII Interface

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Information

This document describes an outline of the reduced gigabit media independent interface (RGMII) and how to implement the low end devices in the RZ/G2 series with RGMII for connection with external PHY devices or PHY switches.

This document consists of the following three major sections:

1. Specifications of the RGMII in outline
2. Specifications of low end RZ/G2 devices for RGMII in outline
3. Notes for connecting external PHY devices and PHY switches

Target Device

- RZ/G2L
- RZ/G2LC
- RZ/V2L
- RZ/G2UL
- RZ/Five
- RZ/G3S
- RZ/G3E

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1. Specifications of the RGMII in Outline

The RGMII is a specification for the connection between the MAC and PHY of Ethernet communications interface. The RGMII is intended to reduce the number of signals required for Ethernet communications at 10-, 100-, or 1000 Mbps compared to former standards, the media independent interface (MII) specified in the IEEE802.3u and the gigabit media independent interface (GMII) specified in the IEEE802.3z.

This document will refer to version 2.0 released on April in 2002 and version 1.3 released on December in 2000. The version 2.0 is the result of major changes from version 1.3. The major changes are following two specifications.

(1) The IO specification change
Version 1.3: 2.5-V **CMOS** interface voltages (defined by JEDEC EIA/JESD8-5) are used with all IO pins.
Version 2.0: 1.5-V **HSTL** interface voltages (defined by JEDEC EIA/JESD8-6) are used with all IO pins.

(2) The extension of timing specification
Version 1.3: A single timing specification is stipulated. This specification states a delay on the board, and is referred to as **original RGMII** in version 2.0.
Version 2.0: Two timing specifications are stipulated. The **RGMII-ID** specification newly added to version 2.0 states a delay inside the device.

1.1 Signal Specification

The MAC and the PHY are connected with fourteen signals in the RGMII. Data and control signals are latched on both rising and falling edges of the clock signal. This allows for the reduction of the number of signals compared to the GMII on same clock speed (125 MHz).

Table 1.1 Definition of Signals

Signal	Source	Sink	Description
TXC	MAC	PHY	Reference clock for use in transmission. It runs at 125, 25, or 2.5 MHz, depending on the link speed.
TD[3:0]	MAC	PHY	Data being transmitted. The meanings of the signals differ with the edge of the TXC signal. Specifically, they contain bits 3:0 on ↑ of TXC and bits 7:4 on ↓ of TXC.
TX_CTL	MAC	PHY	Control signal for transmission. The meaning of the signal differs with the edge of the TXC signal. Specifically, it represents TXEN on ↑ of TXC and TXERR on ↓ of TXC.
RXC	PHY	MAC	Reference clock for use in reception. It runs at 125, 25, or 2.5 MHz, depending on the link speed.
RD[3:0]	PHY	MAC	Data being received. The meanings of the signals differ with the edge of the RXC signal. Specifically, they contain bits 3:0 on ↑ of RXC and bits 7:4 on ↓ of RXC.
RX_CTL	PHY	MAC	Control signal for reception. The meaning of the signal differs with the edge of the RXC signal. Specifically, it represents RXDV on ↑ of RXC and RXERR on ↓ of RXC.
MDIO	MAC or PHY	MAC or PHY	IO signal for control over the PHY layer. The specification is the same as that for an MII.
MDC	MAC	PHY	Clock signal for control over the PHY layer. The specification is the same as that for an MII.

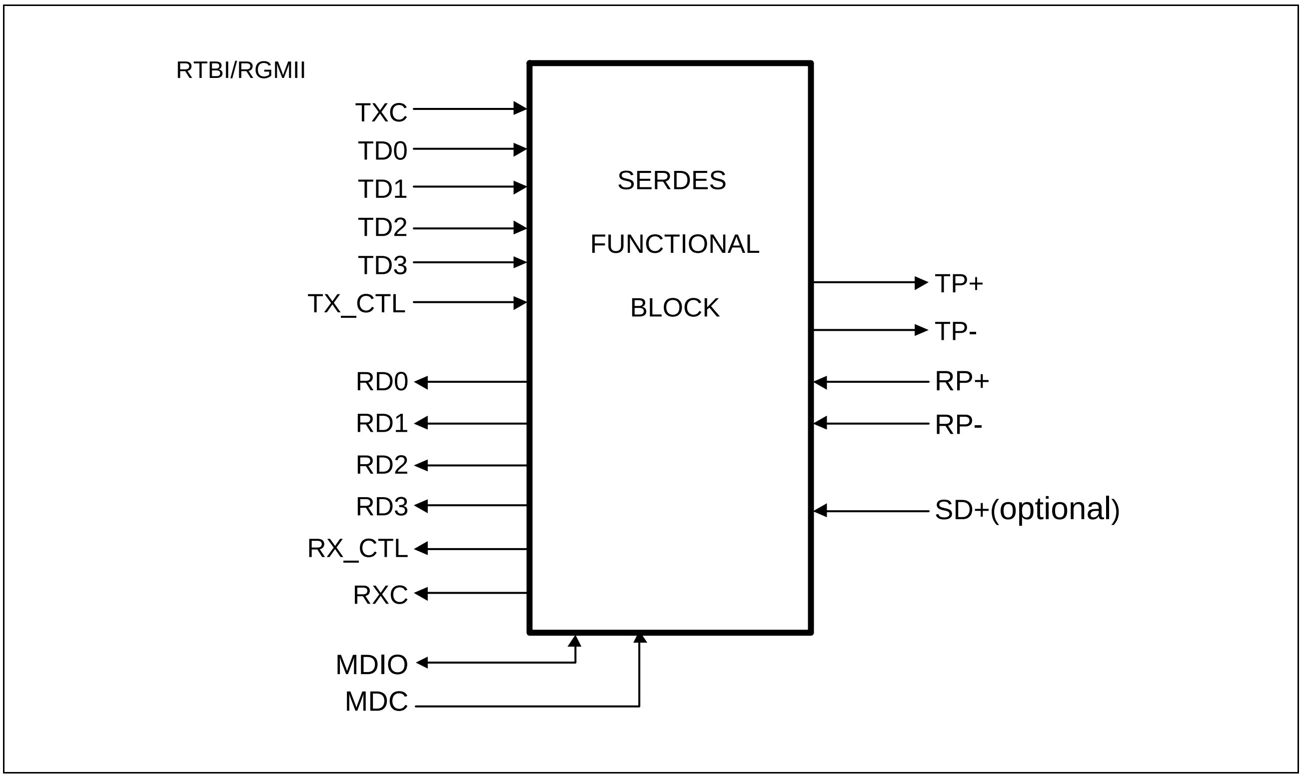

Figure 1.1 System Diagram

1.2 Timing Specification

The RGMII defines two types of timing specification as the original RGMII and the RGMII-ID. While the timing specification in the version 1.3 and earlier is called the original RGMII, the timing specification in version 2.0 is called RGMII-ID.

The difference between the original RGMII and the RGMII-ID is following:

Original RGMII

Clock signals must be delayed from 1.5 ns to 2.0 ns relative to the data signals. This delay is implemented by PCB design.

RGMII-ID

Clock signals must be delayed at least 1.2 ns relative to the data signals. This delay is implemented by the internal design of the MAC devices.

1.2.1 Original RGMII

The original RGMII timing specification refers to version 1.3 and earlier.

Though data and clock generated simultaneously by the MAC, skew between the received data and clock must satisfy TskewT and TskewR shown in the table and figure below. This indicates that 1.5 to 2.0-ns delay is needed to implement in PCB design.

Table 1.2 Timing Specification for Original RGMII Timing

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at Receiver)	1	1.8	2.6	ns
Tcyc	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
Tr/Tf	Rise/Fall Time (20-80%)			0.75	ns

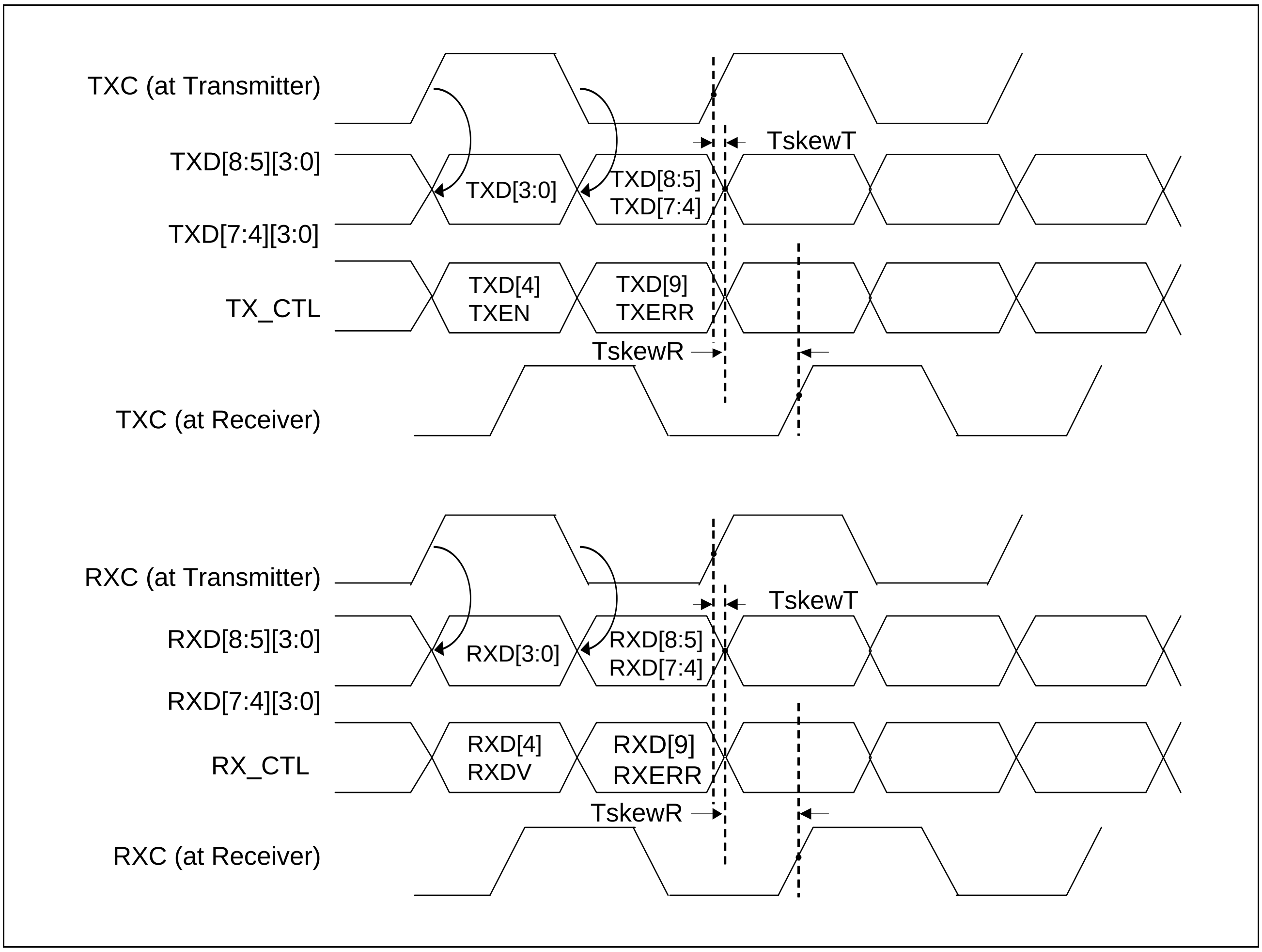

Figure 1.2 Timing Diagram for the original RGMII

1.2.2 RGMII-ID

The RGMII-ID timing specification was added in version 2.0.

While the skew between the data and clock was required to be generated by the PCB design in original RGMII, the skew is now generated by the MAC for RGMII-ID. The MAC adds delays to the clock for TsetupT and TholdT.

Table 1.3 Timing Specification in RGMII-ID

Symbol	Parameter	Min	Typical	Max	Units
TsetupT	Data to Clock output Setup (at Transmitter-integrated delay)	1.2	2.0		ns
TholdT	Data to Clock output Hold (at Transmitter-integrated delay)	1.2	2.0		ns
TsetupR	Data to Clock input Setup (at Receiver-integrated delay)	1.0	2.0		ns
TholdR	Data to Clock input Hold (at Receiver-integrated delay)	1.0	2.0		ns
Tcyc	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
Tr/Tf	Rise/Fall Time (20-80%)			0.75	ns

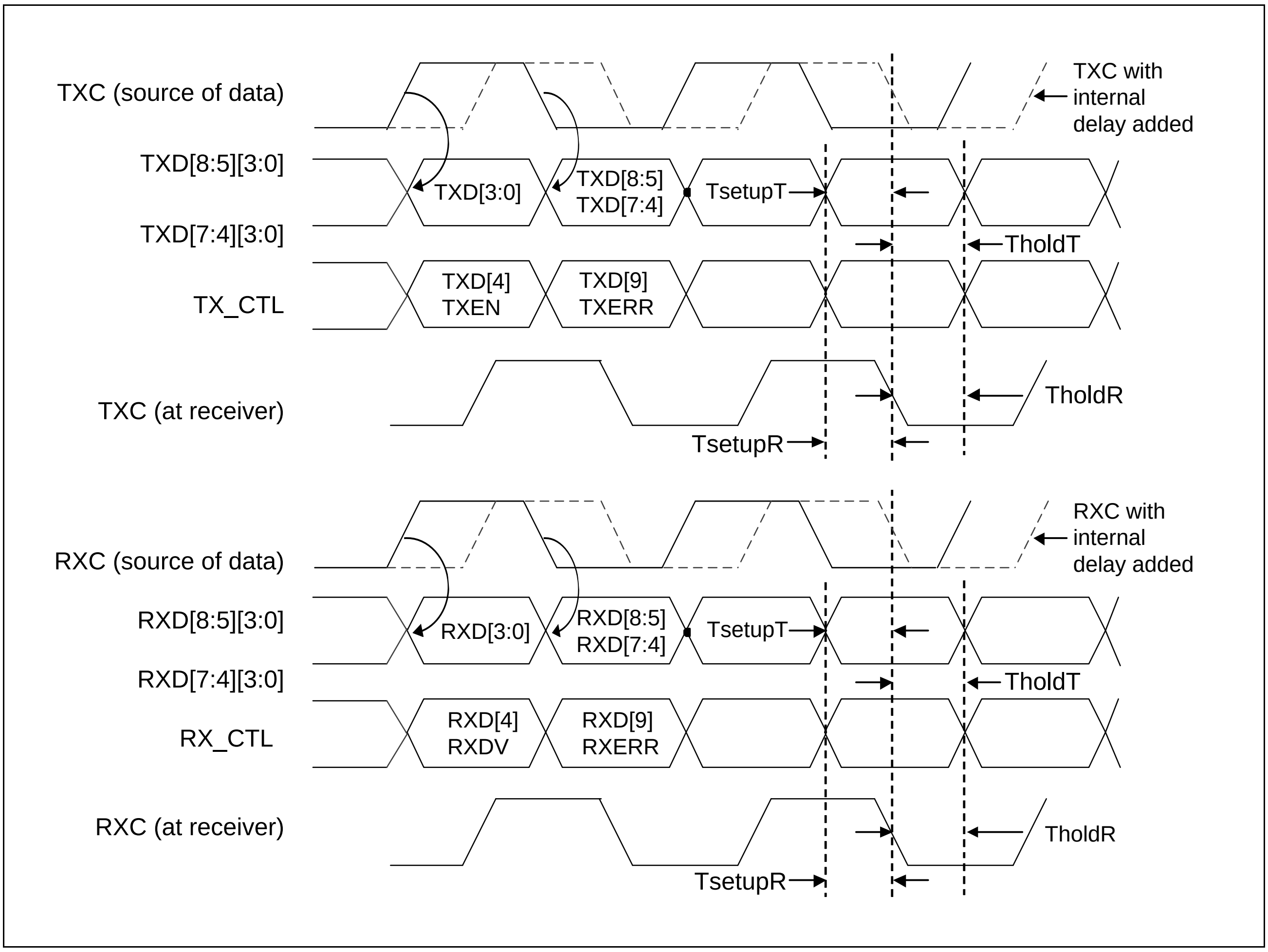

Figure 1.3 Timing Diagram for the RGMII-ID

1.3 I/O Specification

The I/O specification of RGMII was changed from version 1.3 to 2.0.

In version 1.3, all signals including MDIO and MDC are defined as operating with 2.5-V CMOS interface voltages. In version 2.0, on the other hand, they are defined as operating with 1.5-V HSTL interface voltages.

Table 1.4 Interface Specifications

RGMII Version	Interface	Reference
1.3	2.5-V CMOS	JEDEC EIA/JESD8-5
2.0	1.5-V HSTL	JEDEC EIA/JESD8-6

2. Specifications of the low end RZ/G2 series for the RGMII

In this section, specifications of the RGMII for the low end RZ/G2 series MPU is described.

2.1 Signal Specifications

The correspondence between pins of RZ/G devices and RGMII signals is given in table 2-1 below. All RZ/G signals have same functions respective RGMII signals.

Table 2.1 Correspondence between RGMII and RZ/G Signals

RGMII Signal	RZ/G Signal	Input/Output	Voltage
TXC	ETn_TXC/TX_CLK	Output	1.8, 2.5, 3.3 V
TD[3:0]	ETn_TXD[3:0]	Output	1.8, 2.5, 3.3 V
TX_CTL	ETn_TX_CTL/TX_EN	Output	1.8, 2.5, 3.3 V
RXC	ETn_RXC/RX_CLK	Input	1.8, 2.5, 3.3 V
RD[3:0]	ETn_RXD[3:0]	Input	1.8, 2.5, 3.3 V
RX_CTL	ETn_RX_CTL/RX_DV	Input	1.8, 2.5, 3.3 V
MDIO	ETn_MDIO	Output	1.8, 2.5, 3.3 V
MDC	ETn_MDC	Input/Output	1.8, 2.5, 3.3 V

2.2 Timing Specifications

Table 2.2 Ethernet-IF Access Timing (Ether RGMII)

Item		Symbol	Min.	Typ.	Max.	Unit	capaci-tance	Remarks	Figures
Ether RGMII	Data to clock output skew @ transmitter	T_{skewT}	−500	0	500	ps	8 pF	Tx RGMII	Figure 2.1
	Data to clock input skew @ receiver	T_{skewR}	1	1.8	2.6	ns	8 pF		
	Data to clock output setup @ transmitter integrated delay	T_{setupT}	1.2	2.0	—	ns	8 pF	Rx RGMII-ID	Figure 2.2
	Clock to data output hold @ transmitter integrated delay	T_{holdT}	1.2	2.0	—	ns	8 pF		
	Data to clock input setup setup @ receiver integrated delay	T_{setupR}	1.0	2.0	—	ns	8 pF	Rx RGMII-ID	Figure 2.2
	Data to clock input setup hold @ receiver integrated delay	T_{holdR}	1.0	2.0	—	ns	8 pF		
	Clock cycle duration	T_{cyc}	7.2	8	8.8	ns	8 pF	—	—
	Duty cycle for gigabit	Duty_G	40*1	50	60*1	%	8 pF		
	Duty cycle for 10/100T	Duty_T	40*1	50	60*1	%	8 pF		
	Rise/fall time	T_r/T_f	—	—	0.75	ns	8 pF		

Note 1. Relaxed from regulation of RGMII.

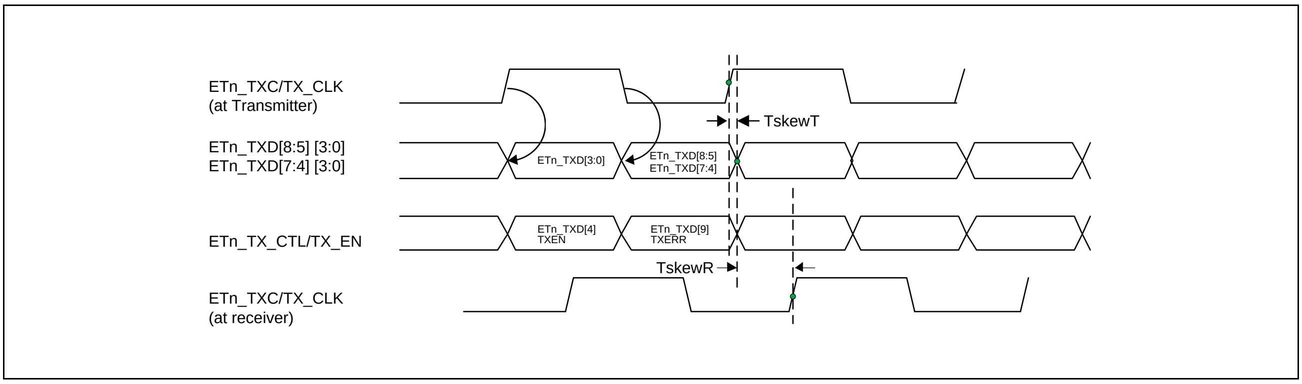

Figure 2.1 Multiplexing & Timing Diagram — RGMII (Transmitter)

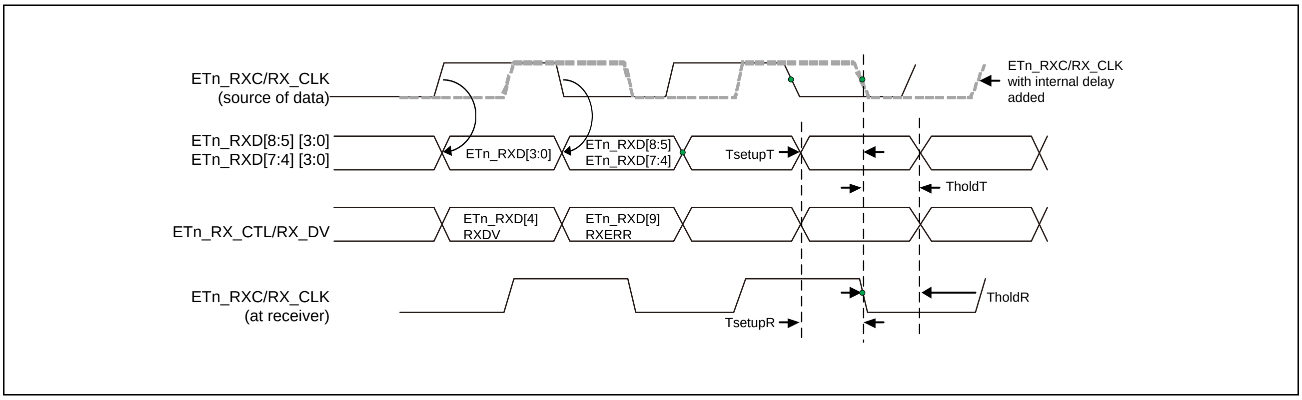

Figure 2.2 Multiplexing & Timing Diagram — RGMII-ID (Receiver)

3. Notes for Implementation

3.1 Assumed External Devices

We assume that two types of devices, PHY devices and switches, may be externally connected to the RZ/G2 devices with RGMII. And in either case, the check points described in this section are applicable.

- PHY device

  This type of device is used for systems with a single port directly connected to an Ethernet cable.

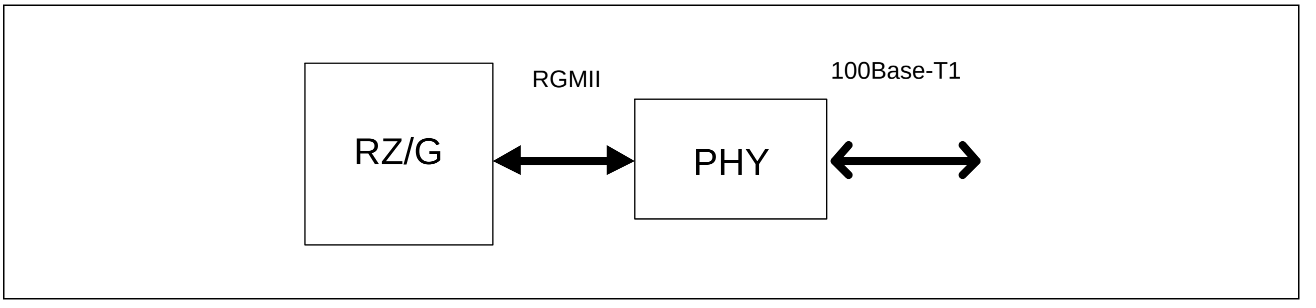

Figure 3.1 Block Diagram of Connection RZ/G and PHY Device

- PHY Switch

  Switches are used for systems with multiple ports connected to multiple Ethernet cables.

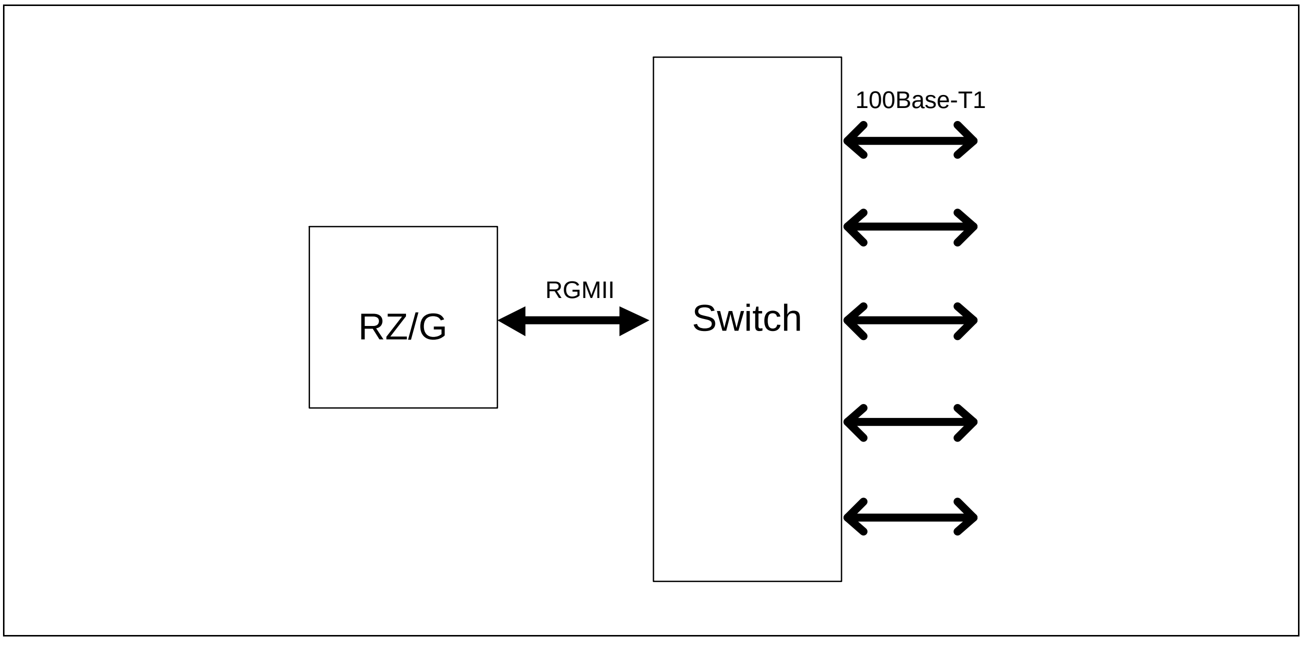

Figure 3.2 Block Diagram of Connection RZ/G and PHY Switch

3.2 Points and Assumptions

The following summarizes points to confirm the connection between an RZ/G2 device and an external PHY device.

- The external device must support the MII/RGMII.

  If the external device does not support, bridge circuitry is needed.

- The I/O specification of the external device must support an operation voltage 1.8 to 3.3V.

  If the external device doesn't support the I/O operating range, level shifters are needed.

- The external device should support RGMII-ID (the device has an internal delay function) for receiving data.

  A device that supports RGMII-ID timing can generally make changes to timing, such as enabling or disabling delays and handling fine adjustment of the delay settings. Select the appropriate combination of settings.

The timing specification is on the assumption that the requirements for board design include the conditions below.

- The wiring lengths of RXC, RD[3:0], and RX_CTL on the PCB must be the same.

  In this case, the delay time to be added for RXC must not be less than the values for the other signals (namely, the wiring length for RXC must not be shorter than the lengths for the other signals).

- The wiring lengths of TXC, TD[3:0], and TX_CTL on the PCB must be the same.

  In this case, the delay time to be added for TXC must not be less than the values for the other signals (namely, the wiring length for TXC must not be shorter than the lengths for the other signals).

3.3 Delay Implementation

The MPU does not have a function to add the TX clock delay internally. So, the implementation of the delay is depends on the delay function of the PHY itself, and is different in the following three cases. Confirm the delay function of the PHY before designing the PCB. In any case, it is recommended to simulate the signal delay for verification.

3.3.1 With an External PHY Able to Add Delay for Both RXC and TXC

In this case, the delay on the PCB design is not needed.

3.3.2 With an External PHY Able to Add Delay Only for RXC

In this case, the delay for the TXC should be implemented in the PCB design.

3.3.3 With an External PHY Unable to Add Delay for Both TXC and RXC

In this case, the delay for both TXC and RXC should be implemented in the PCB design.

4. References

1. Reduced Gigabit Media Independent Interface (RGMII) Version 1.3, 12/10/2000
   http://web.archive.org/web/20160303212629/http://www.hp.com/rnd/pdfs/RGMIIv1_3.pdf
2. Reduced Gigabit Media Independent Interface (RGMII) Version 2.0, 4/1/2002
   http://web.archive.org/web/20160303171328/http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf
3. RZ/G2L Group, RZ/G2LC Group User's Manual: Hardware
   https://www.renesas.com/document/mah/rzg2l-group-rzg2lc-group-users-manual-hardware-0
4. RZ/V2L Group User's Manual: Hardware
   https://www.renesas.com/document/mah/rzv2l-group-users-manual-hardware
5. RZ/Five Group User's Manual: Hardware
   https://www.renesas.com/document/mah/rzfive-group-users-manual-hardware

REVISION HISTORY	RZ/G Series, 2nd and 3rd Generation PCB Design Guideline for RGMII Interface

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 07, 2022	—	First edition issued
1.10	Nov. 24, 2022	1, 14	The RZ/Five product, added
		14	4. References: The description in 3. and 4. , modified
1.20	Nov. 16, 2023	1	The RZ/G3S product, added
1.30	Feb. 21, 2025	—	The RZ/G3E product, added.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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