

RX Family and M32C/R32C Series

Guide for Migration from the M32C/R32C to the RX: A/D and D/A Converters

Abstract

This document describes migration from the A/D and D/A converters in the M32C/R32C Series to the A/D and D/A converters in the RX Family.

Products

- RX Family
- M32C/80 Series
- R32C/100 Series

This document explains migration from the M32C/R32C Series to the RX Family, using the RX660 Group MCU as an example of the RX Family, the M32C/87 Group MCU as an example of the M32C/80 Series MCU, and the R32C/118 Group MCU as an example of the R32C/100 Series MCU. When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

There are differences in terminology between the RX Family MCU and the M32C/R32C Series MCU.

The table below shows the differences in terminology.

Differences in Terminology Between the MCUs of the RX Family and M32C/R32C Series

Item	M32C/R32C Series	RX Family
Peripheral function registers	Special function registers (SFRs)	I/O registers

Contents

1. General Differences in the A/D and D/A Converters	4
1.1 A/D converter.....	4
1.2 D/A converter.....	8
2. Functional Differences in the A/D Converter	9
2.1 Example of A/D Conversion for the Output from One Sensor	9
2.2 Example of A/D Conversion for the Outputs from Two Sensors with Differing Responsiveness	10
3. Appendix	11
3.1 Points on Migration from the M32C/R32C to the RX	11
3.1.1 Interrupts	11
3.1.2 Module Stop Function	11
3.1.3 I/O Ports	12
3.2 I/O Register Macros.....	13
3.3 Intrinsic Functions.....	13
4. Reference Documents	14

1. General Differences in the A/D and D/A Converters

1.1 A/D converter

This section explains general differences in the A/D converter.

Table 1.1 shows General Differences in the A/D Converter Between the M32C/87 and the RX660. Table 1.2 shows General Differences in the A/D Converter Between the R32C/118 and the RX660.

Table 1.1 General Differences in the A/D Converter Between the M32C/87 and the RX660

Item	M32C (M32C/87)	RX (RX660)
	A/D converter	12-bit A/D converter
A/D conversion method	Successive approximation conversion method (capacitive coupling amplifier)	Successive approximation
Analog input voltage	0 V to AVCC (3.0 to 5.5 V)	0 V to AVCC0 (3.0 to 5.5 V)
Operating clock	<ul style="list-style-type: none"> fAD fAD divided by 2 fAD divided by 3 fAD divided by 4 fAD divided by 6 fAD divided by 8 	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio is one of the following. PCLK to ADCLK frequency division ratio = 1:1, 1:2, 2:1, or 4:1
Resolution	8 or 10 bits	12 bits
Operating modes	<ul style="list-style-type: none"> One-shot mode Repeat mode Single sweep mode Repeat sweep mode 0 Repeat sweep mode 1 Multi-port single sweep mode Multi-port repeat sweep mode 0 	Single scan mode Continuous scan mode Group scan mode (Double-trigger mode selectable)
Analog input pins	34 ^{*1} <ul style="list-style-type: none"> AN0 to AN7 AN0_0 to AN0_7 AN2_0 to AN2_7 AN15_0 to AN15_7^{*2} ANEX0 and ANEX1 	24 <ul style="list-style-type: none"> 24 analog input pins
Internally generated analog input	—	<ul style="list-style-type: none"> One for the temperature sensor One for the internal reference voltage One for the self-diagnosis function
Conditions to start A/D conversion	<ul style="list-style-type: none"> Software trigger External trigger^{*3} Hardware trigger (When the timer B2 interrupt request of the timer function for controlling a 3-phase motor is issued) 	<ul style="list-style-type: none"> Software trigger Asynchronous trigger (ADTRG0# pin)^{*4} Synchronous trigger (triggers from the MTU, ELC, and TMR)
Sample and hold function	Available	Available
Low power consumption	Available	Module can be set to the module stop state
A/D-converted value addition function	—	Available

Item	M32C (M32C/87)	RX (RX660)
	A/D converter	12-bit A/D converter
Self-diagnosis function	—	Self-diagnosis function, analog input disconnection detection assist function
Event link function	—	A/D conversion can be started when an event signal is input.
Interrupts	A/D conversion interrupt	A/D scan end interrupt (S12ADI, S12GBADI, or S12GCADI) Compare interrupt (S12CMPAI or S12CMPBI)
Conversion cycle	<ul style="list-style-type: none"> When AVCC = 3.0 to 3.6 V 8-bit resolution: 4.9 μs (per channel, when ϕAD = 10 MHz *5) When AVCC = 4.2 to 5.5 V 10-bit resolution: 2.06 μs 8-bit resolution: 1.75 μs (per channel, when ϕAD = 16 MHz *6) 	0.9 μ s (per channel, when ADCLK = 60 MHz)
Error	<ul style="list-style-type: none"> When AVCC = 3.3 V (DNL differential nonlinearity error) ± 1 LSB (maximum) (INL integral nonlinearity error) ± 2 LSB (maximum) Example when AVCC is 3.3 V and resolution is 8 bits: Error of ± 25.781 mV (maximum) *7 When AVCC = 5.5 V (DNL differential nonlinearity error) ± 1 LSB (maximum) (INL integral nonlinearity error) AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 *2, ANEX0, ANEX1: ± 3 LSB (maximum) External operating amplifier connection mode: ± 7 LSB (maximum) Example when AVCC is 5.0 V and resolution is 10 bits: Error of ± 14.648 mV (maximum) *7 	(DNL differential nonlinearity error) ± 1 LSB (typical) (INL integral nonlinearity error) ± 1.5 LSB (typical), ± 2.5 LSB (maximum) Example when AVCC is 3.3 V: Error of ± 2.014 mV (maximum) *7

- Notes: 1. This value applies to 144-pin packages. The number of pins is 26 in 100-pin packages.
2. 100-pin packages do not have pins AN15_0 to AN15_7.
3. If an external trigger is input during A/D conversion, the current A/D conversion is halted, and A/D conversion starts again.
4. If an asynchronous trigger is input during A/D conversion, A/D conversion continues.
5. Make sure that the conversion cycle does not exceed 10 MHz. If $f(\text{CPU}) (=f_{\text{AD}})$ is 24 MHz, divide it by 3 to set ϕ AD at 8 MHz. At this time, the time required for A/D conversion is 6.1 μ s.
6. If $f(\text{XIN})$ exceeds 16 MHz, divide it to set ϕ AD at 16 MHz or lower.
7. The voltage calculated assumes the conditions listed in the Electrical Characteristics – the actual error may vary.

Table 1.2 General Differences in the A/D Converter Between the R32C/118 and the RX660

Item	R32C (R32C/118) A/D converter	RX (RX660) 12-bit A/D converter
A/D conversion method	Successive approximation conversion method (capacitive coupling amplifier)	Successive approximation
Analog input voltage	0 V to AVCC (3.0 to 5.5 V)	0 V to AVCC0 (3.0 to 5.5 V)
Operating clock	fAD, fAD/2, fAD/3, fAD/4, fAD/6, or fAD/8	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio is one of the following. PCLK to ADCLK frequency division ratio = 1:1, 1:2, 2:1, or 4:1
Resolution	8 or 10 bits	12 bits
Operating modes	<ul style="list-style-type: none"> One-shot mode Repeat mode Single sweep mode Repeat sweep mode 0 Repeat sweep mode 1 Multi-port single sweep mode Multi-port repeat sweep mode 0 	Single scan mode Continuous scan mode Group scan mode (Double-trigger mode selectable)
Analog input pins	34 ^{*1} <ul style="list-style-type: none"> AN0 to AN7 AN0_0 to AN0_7 AN2_0 to AN2_7 AN15_0~AN15_7 ^{*2} ANEX0 and ANEX1 	24 <ul style="list-style-type: none"> 24 analog input pins
Internally generated analog input	—	<ul style="list-style-type: none"> One for the temperature sensor One for the internal reference voltage One for the self-diagnosis function
Conditions to start A/D conversion	<ul style="list-style-type: none"> Software trigger External trigger ^{*3} Hardware trigger (When the timer B2 interrupt request of the timer function for controlling a 3-phase motor is issued) 	<ul style="list-style-type: none"> Software trigger Asynchronous trigger (ADTRG0# pin) ^{*4} Synchronous trigger (triggers from the MTU, ELC, and TMR)
Sample and hold function	Available	Available
Low power consumption	Available	Module can be set to the module stop state
A/D-converted value addition function	—	Available
Self-diagnosis function	—	Self-diagnosis function, analog input disconnection detection assist function
Event link function	—	A/D conversion can be started when an event signal is input.
Interrupts	A/D conversion interrupt	A/D scan end interrupt (S12ADI, S12GBADI, or S12GCADI) Compare interrupt (S12CMPAI or S12CMPBI)

Item	R32C (R32C/118)	RX (RX660)
	A/D converter	12-bit A/D converter
Conversion cycle	<ul style="list-style-type: none"> When AVCC = 3.0 to 3.6 V 10-bit resolution with the sample and hold function enabled: 3.3 μs 8-bit resolution with the sample and hold function enabled: 2.8 μs (per channel, when ϕAD = 10 MHz) When AVCC = 4.2 to 5.5 V 10-bit resolution with the sample and hold function enabled: 2.06 μs 10-bit resolution with the sample and hold function disabled: 3.69 μs 8-bit resolution with the sample and hold function enabled: 1.75 μs 8-bit resolution with the sample and hold function disabled: 3.06 μs (per channel, when ϕAD = 16 MHz) 	0.9 μ s (per channel, when ADCLK = 60 MHz)
Error	<ul style="list-style-type: none"> When AVCC = 3.3 V (DNL differential nonlinearity error) ± 1 LSB (maximum) (INL integral nonlinearity error) AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 *2, ANEX0, ANEX1: ± 5 LSB (maximum) External operating amplifier connection mode: ± 7 LSB (maximum) Example when AVCC is 3.3 V: Error of ± 16.113 mV (maximum) *5 When AVCC = 5.0 V (DNL differential nonlinearity error) ± 1 LSB (maximum) (INL integral nonlinearity error) AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7 *2, ANEX0, ANEX1: ± 3 LSB (maximum) External operating amplifier connection mode: ± 7 LSB (maximum) Example when AVCC is 5.0V: Error of ± 14.648 mV (maximum) *5 	<p>(DNL differential nonlinearity error) ± 1 LSB (typical) (INL integral nonlinearity error) ± 1.5 LSB (typical), ± 2.5 LSB (maximum)</p> <p>Example when AVCC is 3.3 V: Error of ± 2.014 mV (maximum) *5</p>

- Notes: 1. This value applies to 144-pin packages. The number of pins is 26 in 100-pin packages.
2. 100-pin packages do not have pins AN15_0 to AN15_7.
3. If an external trigger is input during A/D conversion, the current A/D conversion is halted, and A/D conversion starts again.
4. If an asynchronous trigger is input during A/D conversion, A/D conversion continues.
5. The voltage calculated assumes the conditions listed in the Electrical Characteristics – the actual error may vary.

1.2 D/A converter

This section explains general differences in the D/A converter.

Table 1.3 shows General Differences in the D/A Converter Between the M32C/87 and the RX660. Table 1.4 shows General Differences in the D/A Converter Between the R32C/118 and the RX660.

Table 1.3 General Differences in the D/A Converter Between the M32C/87 and the RX660

Item	M32C (M32C/87)	RX (RX660)
	D/A converter	12-bit D/A converter
Resolution	8 bits	12 bits
D/A conversion on channels 0 and 1	—	Independently controlled or single whole controlled can be selected
Selectable formats	—	Whether data in the data register is right-aligned or left-aligned can be selected
Analog output pins	2 pins • DA0 and DA1	2 pins • DA0 and DA1
Low power consumption	—	Module can be set to the module stop state
Event link function	—	D/A0 conversion can be started when an event signal is input.

Table 1.4 General Differences in the D/A Converter Between the R32C/118 and the RX660

Item	R32C (R32C/118)	RX (RX660)
	D/A converter	12-bit D/A converter
Resolution	8 bits	12 bits
D/A conversion on channels 0 and 1	—	Independently controlled or single whole controlled can be selected
Selectable formats	—	Whether data in the data register is right-aligned or left-aligned can be selected
Analog output pins	2 pins • DA0 and DA1	2 pins • DA0 and DA1
Low power consumption	—	Module can be set to the module stop state
Event link function	—	D/A0 conversion can be started when an event signal is input.

2. Functional Differences in the A/D Converter

This section explains the differences in using the A/D converter to perform A/D conversion.

The explanations in this section are based on the cases where the A/D converters of the RX660 Group and M32C/R32C Series MCUs operate under the conditions shown in Table 2.1.

Table 2.1 Modes Used in A/D Converter Operating Example

No.	Operating Example	M32C/R32C	RX
1	A/D convert the output from one sensor (refer to the operation shown in Figure 2.1)	One-shot mode	Single scan mode
2	A/D convert the output from two sensors with differing responsiveness (refer to the operation shown in Figure 2.2)	Single sweep mode	Group scan mode

2.1 Example of A/D Conversion for the Output from One Sensor

This section shows an example in which the RX660 Group and M32C/R32C Series MCUs operate according to the timing chart in Figure 2.1. For the modes to be used, refer to Table 2.1.

Operational example common to the RX660 and M32C/R32C:

- (1) When conversion starts
A/D conversion is started.
- (2) When A/D conversion ends
When A/D conversion is completed, the converted value is stored in an A/D register, and an A/D conversion complete interrupt request is generated. The A/D conversion result is read in the interrupt handling.

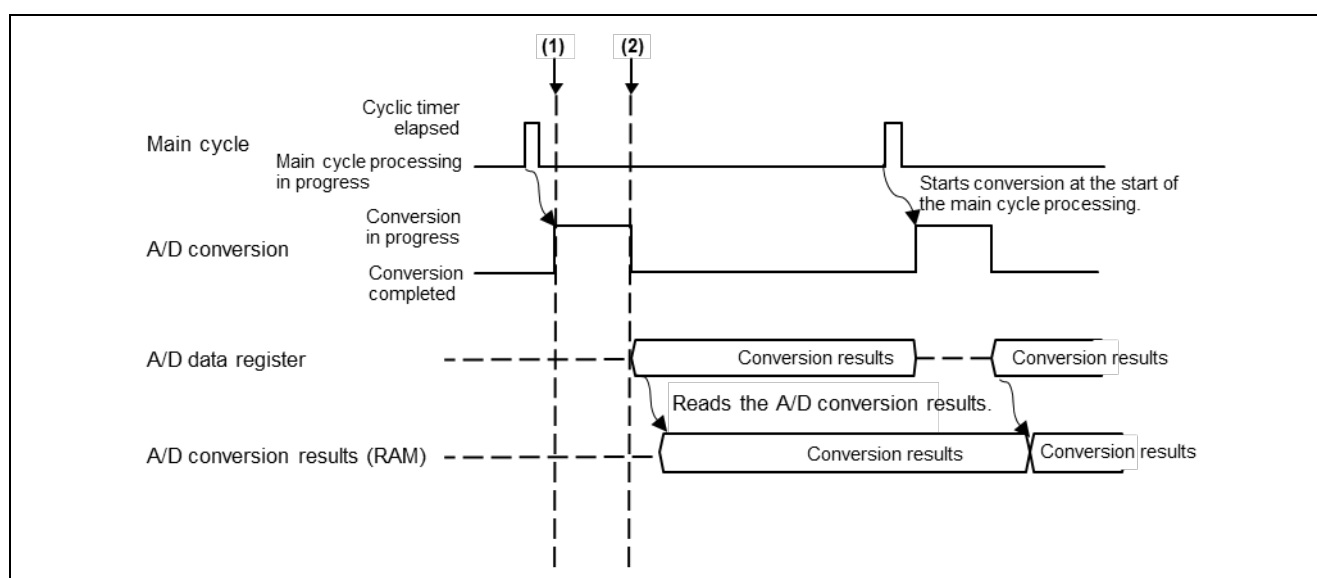


Figure 2.1 Timing Chart for A/D Conversion for the Output from One Sensor

2.2 Example of A/D Conversion for the Outputs from Two Sensors with Differing Responsiveness

This section shows an example in which the RX660 Group and M32C/R32C Series MCUs operate according to the timing chart in Figure 2.2. For the modes to be used, refer to Table 2.1.

Operational example of the RX660:

Output from a sensor with good response is converted on A/D channel 0 using the MTU0.TGRA0 source. Output from a sensor with poor response is converted on A/D channel 1 using the MTU0.TGRB0 source.

(1) When conversion starts

The TGRA0 source is generated, and A/D conversion starts on A/D channel 0.

(2) When A/D conversion on A/D channel 0 ends

A/D conversion on A/D channel 0 is completed.

(3) When A/D conversion on A/D channel 1 starts

The TGRB0 source is generated approximately 150 μ s after the A/D conversion start trigger, and A/D conversion starts on A/D channel 1.

(4) When A/D conversion on A/D channel 1 ends

A/D conversion on A/D channel 1 is completed. When all A/D conversions are completed, an interrupt request about completion of A/D conversions is generated. The A/D conversion result is read in the interrupt handling.

Operational example of the M32C/R32C:

In single sweep mode, the sensor with good response uses A/D channel 0 for A/D conversion and the sensor with poor response uses A/D channel 5 for A/D conversion. A conversion wait of approximately 150 μ s is secured with the conversion time for the AN0 to AN4 pins.

(1) When conversion starts

A/D conversion is started on A/D channel 0.

(2) When A/D conversion on A/D channel 0 ends

A/D conversion on A/D channel 0 is completed.

(3) When A/D conversion on A/D channel 5 starts

A/D conversion is started on A/D channel 5.

(4) When A/D conversion on A/D channel 5 ends

A/D conversion on A/D channel 5 is completed. When all A/D conversions are completed, an interrupt request about completion of A/D conversions is generated. The A/D conversion result is read in the interrupt handling.

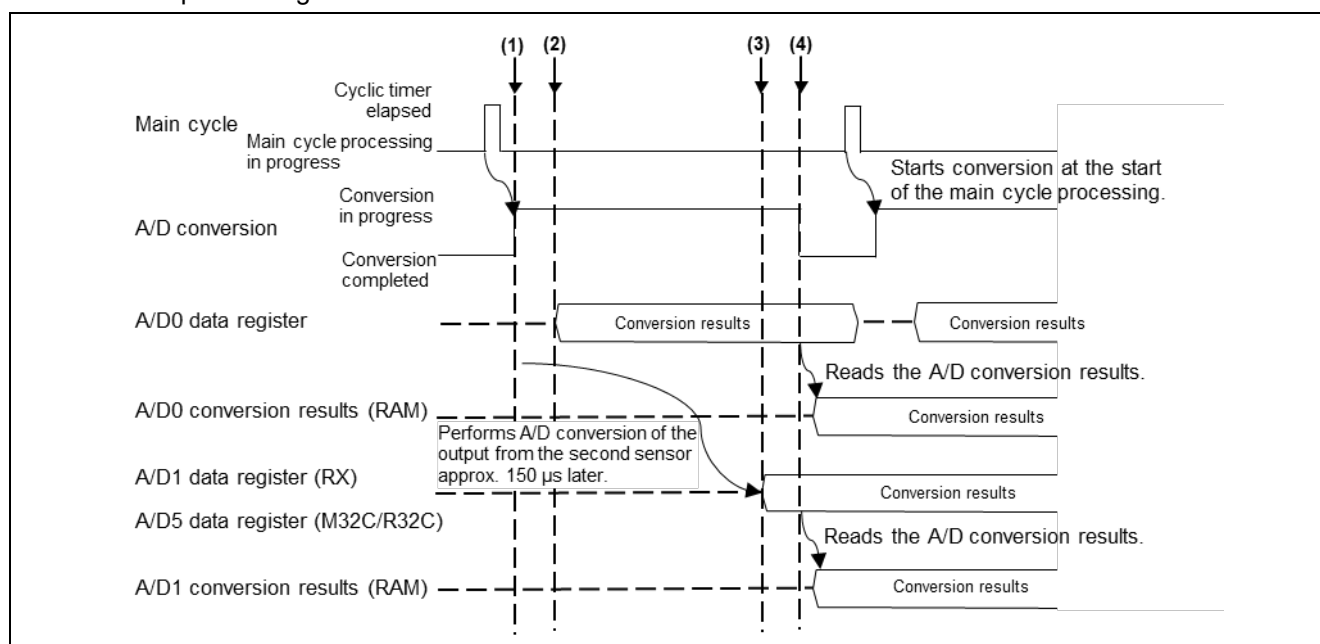


Figure 2.2 Timing Chart for A/D Conversion for the Outputs from Two Sensors with Differing Responsiveness

3. Appendix

3.1 Points on Migration from the M32C/R32C to the RX

This section explains points on migration from the M32C/R32C to the RX.

3.1.1 Interrupts

For the RX Family, when an interrupt request is received while all of the following conditions are met, the interrupt occurs.

- The I flag (PSW.I bit) is 1.
- Registers IER and IPR in the ICU are set to enable interrupts.
- The interrupt request is enabled by the interrupt request enable bits for peripheral functions.

Table 3.1 shows Comparison of Conditions for Interrupt Generation Between the M32C/R32C and the RX.

Table 3.1 Comparison of Conditions for Interrupt Generation Between the M32C/R32C and the RX

Item	M32C/R32C	RX
I flag	When the I flag is set to 1 (enabled), the maskable interrupt request can be accepted.	
Interrupt request flag	When an interrupt request is generated by a peripheral function, the interrupt request flag becomes 1 (interrupt requested).	
Interrupt priority level	Selected by setting bits ILVL2 to ILVL0.	Selected by setting the IPR[3:0] bits.
Interrupt request enable	—	Specified by setting the IER register.
Interrupt enable for peripheral functions	—	Interrupts can be enabled or disabled in each peripheral function.

For more information, refer to sections Interrupt Controller (ICU), CPU, and sections for other peripheral functions used in the User's Manual: Hardware.

3.1.2 Module Stop Function

The RX Family has the ability to stop each peripheral module individually.

By transitioning unused peripheral modules to the module stop state, power consumption can be reduced.

After a reset is released, all modules (with a few exceptions) are in the module stop state.

Registers for modules in the module stop state cannot be written to or read.

For more information, refer to the Low Power Consumption section in the User's Manual: Hardware.

3.1.3 I/O Ports

In the RX Family, the MPC must be configured in order to assign I/O signals from peripheral functions to pins.

Before performing pin I/O control in the RX Family, perform the following two operations:

- In the MPC.PFS register, select the peripheral functions that are assigned to the appropriate pins.
- In the PMR register for I/O ports, select the function for the pin to be used as a general I/O port or I/O port for a peripheral function.

The M32C/R32C provides a function select register that allows the user to select whether to use the pin as an I/O port or for the output port for a specific peripheral function.

Before performing pin I/O control in the M32C, perform the following two operations:

- Function select registers B to E: Use these registers to select the peripheral function that can be assigned to the target pin.
- Function select register A: Use this register to select whether the target pin is to be used as a general I/O port or for the selected peripheral function.

Before performing pin I/O control in the R32C, perform the following operation:

- Function select register: Use this register to select the peripheral function that can be assigned and to select whether the target pin is to be used as a general I/O port or for the selected peripheral function.

Table 3.2 shows Comparison of I/O Settings for Peripheral Function Pins Between the M32C and the RX.

Table 3.3 shows Comparison of I/O Settings for Peripheral Function Pins Between the R32C and the RX.

Table 3.2 Comparison of I/O Settings for Peripheral Function Pins Between the M32C and the RX

Function	M32C (in the case of the M32C/87)	RX (in the case of the RX660)
Select the pin function	With the function select registers B to E, I/O ports for peripheral functions can be assigned by selecting from multiple pins.	With the PFS register, I/O ports for peripheral functions can be assigned by selecting from multiple pins.
Switch between general I/O port and peripheral function	With the function select register A, the corresponding pin function can be selected as a general I/O port or a peripheral function.	With the PMR register, the corresponding pin function can be selected as a general I/O port or a peripheral function.

Table 3.3 Comparison of I/O Settings for Peripheral Function Pins Between the R32C and the RX

Function	R32C (in the case of the R32C/118)	RX (in the case of the RX660)
Select the pin function	With the function select register, the corresponding pin function can be selected as a general I/O port or a peripheral function.	With the PFS register, I/O ports for peripheral functions can be assigned by selecting from multiple pins.
Switch between general I/O port and peripheral function	Output ports for peripheral functions can be assigned by selecting from multiple pins.	With the PMR register, the corresponding pin function can be selected as a general I/O port or a peripheral function.

For details on the RX, refer to the chapters on the multi-function pin controller (MPC) and I/O ports in the user's manual for hardware.

For details on the M32C, refer to the chapter on programmable I/O ports in the user's manual for hardware.

For details on the R32C, refer to the chapter on I/O ports in the user's manual for hardware.

3.2 I/O Register Macros

Macro definitions listed in Table 3.4 can be found in the RX I/O register definitions (iodefine.h).

The readability of programs can be achieved with these macro definitions.

Table 3.4 shows Macro Usage Examples.

Table 3.4 Macro Usage Examples

Macro	Usage Example
IR("module name", "bit name")	IR(MTU0, TGIA0) = 0 ; The IR bit corresponding to MTU0.TGIA0 is cleared to 0 (no interrupt request is generated).
DTCE("module name", "bit name")	DTCE (MTU0, TGIA0) = 1 ; The DTCE bit corresponding to MTU0.TGIA0 is set to 1 (DTC activation is enabled).
IEN("module name", "bit name")	IEN(MTU0, TGIA0) = 1 ; The IEN bit corresponding to MTU0.TGIA0 is set to 1 (interrupt enabled).
IPR("module name", "bit name")	IPR(MTU0, TGIA0) = 0x02 ; The IPR bit corresponding to MTU0.TGIA0 is set to 2 (interrupt priority level 2).
MSTP("module name")	MSTP(MTU) = 0 ; The MTU0 Module Stop bit is set to 0 (module stop state is canceled).
VECT("module name", "bit name")	#pragma interrupt (Excep_MTU0_TGIA0 (vect=VECT(MTU0, TGIA0)) The interrupt function is declared for the corresponding MTU0.TGIA0 register.

3.3 Intrinsic Functions

The RX Family has intrinsic functions for setting control registers and special instructions. When using intrinsic functions, include machine.h.

Table 3.5 shows Examples of Differences in the Settings of Control Registers and Descriptions of Special Instructions Between the M32C/R32C and the RX.

Table 3.5 Examples of Differences in the Settings of Control Registers and Descriptions of Special Instructions Between the M32C/R32C and the RX

Item	Description	
	M32C/R32C	RX
Set the I flag to 1	asm("fset i");	setpsw_i (); ^{*1}
Set the I flag to 0	asm("fclr i");	clrpsw_i (); ^{*1}
Expanded into the WAIT instruction	asm("wait");	wait(); ^{*1}
Expanded into the NOP instruction	asm("nop");	nop(); ^{*1}

Note: 1. The machine.h file must be included.

4. Reference Documents

User's Manual: Hardware

RX660 Group User's Manual: Hardware (R01UH0937EJ)

M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual (REJ09B0180)

R32C/118 Group User's Manual: Hardware (R01UH0212EJ)

If you are using a product that does not belong to the above groups, refer to the applicable user's manual for hardware.

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family CC-RX Compiler User's Manual (R20UT3248EJ)

C Compiler Package for the M32C Series (M3T-NC308WA)

C Compiler Package for the R32C Series

The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 10, 24	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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