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Generating a TCS File using Frequency List Wizard in Timing Commander

This document explains how generate a TCS file using the Frequency List Wizard feature in Timing Commander. The document is applicable to the following ClockMatrix devices: RC32012A, RC32112A, RC22112A, 8A34005, and RC38612.

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1. Introduction

In order to create a simple configuration in selected ClockMatrix devices, Renesas added a new feature to Timing Commander called "Frequency Wizard." To use this feature, a user enters the configuration into the Frequency Wizard tab, including input frequencies, output frequencies, groups, signal types, crystal frequency, and an optional OCXO/TCXO frequency. Each clock (input and output) must be mapped to up to four possible groups that set which outputs lock to the same set of inputs. From this specification, the tool will generate a TCS file with the required channel and output details based on the customer requirements. This feature is available in Timing Commander Personality 10.9.0 and later.

2. Supported Devices

The following ClockMatrix devices are supported:

- RC32012A (SysDPLL, 1 x DPLL, 3 x Synth with TDC)
- RC32112A (SysDPLL, 1 x DPLL, 5 x Synth with TDC)
- RC22112A (no SysDPLL, no DPLL, 5 x Synth, no TDC)

In addition, this feature can also generate TCS (Timing Commander Setup) files for the 8A34005 and RC38612 but should only be used for simple configurations for these more complicated devices.

3. Frequency List Wizard Window

Figure 1 shows a typical use of the frequency list wizard. For this example, the requirements are:

- 1. Input 10MHz and output 20MHz
- 2. Input 25MHz and output 20MHz



Figure 1. Frequency List Wizard



The user must map these signals to groups into the tool. In this case, requirement 1 is mapped to group A and requirement 2 is mapped to group B. The 20MHz output in group A is locked to the 10MHz input while the 20MHz in group B is locked to the 25MHz input.

The input crystal (Xtal) frequency is always required but the OCXO/TCXO frequency is optional.

4. Example 1

The configuration for example 1 is shown in the table.

Input Frequency (MHz)	Output Frequency (MHz)
10	10
20	20
25	25
40	40

The user must add the four groups to show that each pair of input and output frequencies are independent. Figure 2 shows this same configuration as entered into the GUI.

Frequency List Wizard					
Solve					
	INPUTS			<u>OUTPUTS</u>	
FREQUENCY	SIGNAL TYPE	GROUP	FREQUENCY	SIGNAL TYPE	GROUP
10 🎦	CMOS ~	🖸 🔺 🎦	10 🎦	LVCMOSInPhase Y	' 🗂 🔺 🎦
20 🞦	CMOS ~	🖸 в 🖌 🎦	20 🞦	LVCMOSInPhase Y	в ど 🛅
25 🎦	CMOS ~	🖸 🗸 🖸	25 🦰	LVCMOSInPhase Y	· 🖸 c 💉 🖸
40 🞦	CMOS ~	🖸 🕞 🖌 🖸	40 🎦	LVCMOSInPhase Y	· 🖸 🖸 🖌 🖸
			<u> </u>	LVCMOSInPhase Y	· 🗂 🔺 🗂
			<u> </u>	LVCMOSInPhase Y	· 📑 🔺 📑
				LVCMOSInPhase Y	A Y 🗂
				LVCMOSInPhase Y	· 🗅 🔺 🗂
				LVCMOSInPhase Y	- A
				LVCMOSInPhase Y	
				LVCMOSInPhase Y	
				IVCMOSInPhase Y	
				Evenuosiin hase	
				Input Xtal Frequency:	49.152MHz
				OCXO/TCXO Frequency:	10MHz

Figure 2. Example 1 – Frequency List Wizard Screenshot

After the user enters the configuration, Timing Commander will create the configuration shown in Figure 3. The algorithm maps groups A, B, C, and D to Channels 0, 2, 5, and 7, respectively. Similarly, outputs are mapped to Q0, Q3, Q2, and Q6.



Figure 3. Example 1 – Timing Commander Diagram View

5. Example 2 – With Output TDC

When the specified frequency list needs multiple channels in the device, the tool will automatically configure the combo bus and Output TDC (OTDC) as needed. To see a configuration with the OTDC enabled, it will need at least 8 outputs with one input and inputs and outputs being in the same group.

For the example configuration in Figure 4, group A has more outputs than can be connected to a single DPLL channel in the device, so the tool used DPLL0 as the main DPLL and used DPLL2 to drive additional outputs. Both DPLLs are locked to the input clock and DPLL2 is aligned to DPLL0 via the OTDC.



Figure 4. Example 2 – Frequency List Wizard Screenshot

As shown in Figure 5, group A contains clk0, DPLL0, DPLL1, Q0, Q1, Q3, Q4, Q5, Q6, Q9, and Q10. The outputs are assigned out of order due to the limited connections between the DPLLs and outputs in the device.



Figure 5. Example 2 – Timing Commander Diagram View

Figure 6 shows the details of the OTDC configuration as generated by the tool. This was automatically generated by tools and should not be changed.



Figure 6. Example 2 – Output TDC Details

6. Device-specific Limitations

The frequency list wizard understands the feature set of each device and limits the configurations as needed:

- RC32012A Only A input group allowed; four output groups allowed
- RC32112A Only A input group allowed; four output groups allowed
- RC22112A No input groups allowed; only A output group allowed
- 8A34005, RC38612 Four inputs groups allowed; four output groups allowed

For more information about each device's features, see the device datasheets located on <u>ClockMatrix Timing</u> <u>Solutions | Renesas</u>.

7. Revision History

Revision	Date	Description
1.00	June 21, 2023	Initial release.

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