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April 1st, 2010
Renesas Electronics Corporation

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H8SX Family

Generating Long-Period Pulse Output

Introduction

Pulses with a long period are output using the 16-bit timer pulse unit (TPU). Two channels of the 16-bit timer are cascaded to form a 32-bit counter, which is used in generation of long-period pulse output.

Target Device

H8SX/1653

Contents

1. Specifications

(1) Long-period pulses are output as shown in figure 1. The output pulse in this sample task has a period of 2.8 ms and a low-level width of 0.7 ms.
(2) Long-period operation is implemented using a 32-bit counter that is configured by cascade connection of TPU_4 and TPU_5.
(3) Pulse waveforms are output by TPU_4 in PWM mode 1.

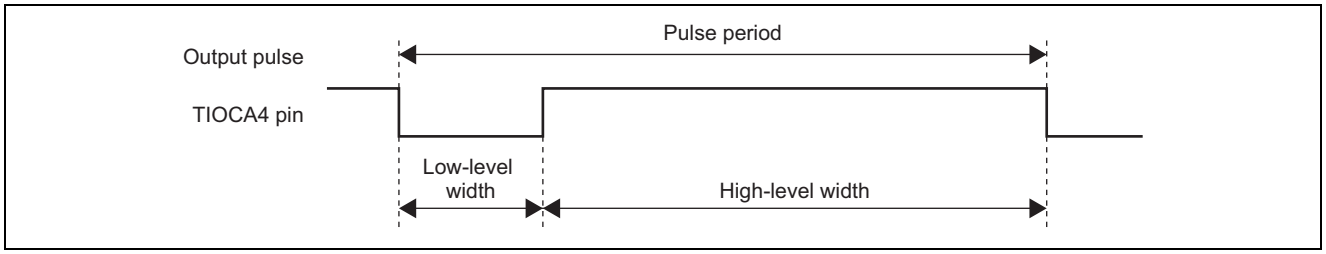


Figure 1 Example of Long-Period Pulse Output

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	12 MHz
	System clock (Iϕ):	48 MHz
	Peripheral module clock (Pϕ):	24 MHz
	External bus clock (Bϕ):	48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	
Development tool	High-performance Embedded Workshop Version 4.00.03	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 2 Section Setting

Address	Section Name	Description
H'001000	P	Program area

3. Description of Modules Used

The TPU performs 32-bit counter operation by cascade connection of TPU_4 and TPU_5 to output long-period pulses. Figure 2 shows a block diagram. The TPU registers are described below.

- Timer start register (TSTR)
  TSTR starts or stops TCNT operation for channels 0 to 5. Before setting the operating mode in TMDR or setting the TCNT counter clock in TCR, counting by TCNT should be stopped.

- Timer control register_4, _5 (TCR_4, TCR_5)
  TCR controls the TCNT on each channel. The TPU has a total of six TCR registers, one for each channel. TCR register settings should be made only while TCNT operation is stopped.

- Timer I/O control register_4, _5 (TIOR_4, TIOR_5)
  TIOR controls timer general registers (TGR). The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.
  The initial output specified by TIOR is applied while the counter is stopped (the CST bit in TSTR is cleared to 0). In PWM mode 2, TIOR specifies the output at the point when the counter is cleared to 0.
  When TIOR is set to specify TGRC or TGRD for buffer operation, the above setting becomes invalid and the TGR register operates as a buffer register.
  When TIOR is set to configure an input capture function, the DDR and ICR bits for the corresponding pin should be set to 0 and 1, respectively.

- Timer counter_4, _5 (TCNT_4, TCNT_5)
  TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel. TCNT is initialized to H'0000 by a reset or in hardware standby mode. TCNT cannot be accessed in 8-bit units and must always be accessed in 16-bit units.

- Timer general register A_4 (TGRA_4)
- Timer general register B_4 (TGRB_4)
  TGR is a 16-bit readable/writable register that can be used as either an output-compare or input-capture register. The TPU has 16 general registers, four each for channels 0 and 3, and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated as buffer registers. TGR cannot be accessed in 8-bit units and must always be accessed in 16-bit units. Combinations of TGR and buffer register in buffer operation are TGRA–TGRC and TGRB–TGRD.

- Timer mode register_4 (TMDR_4)
  TMDR sets the operating mode for each channel. TPU_4 is set in PWM mode 1 in this sample task.

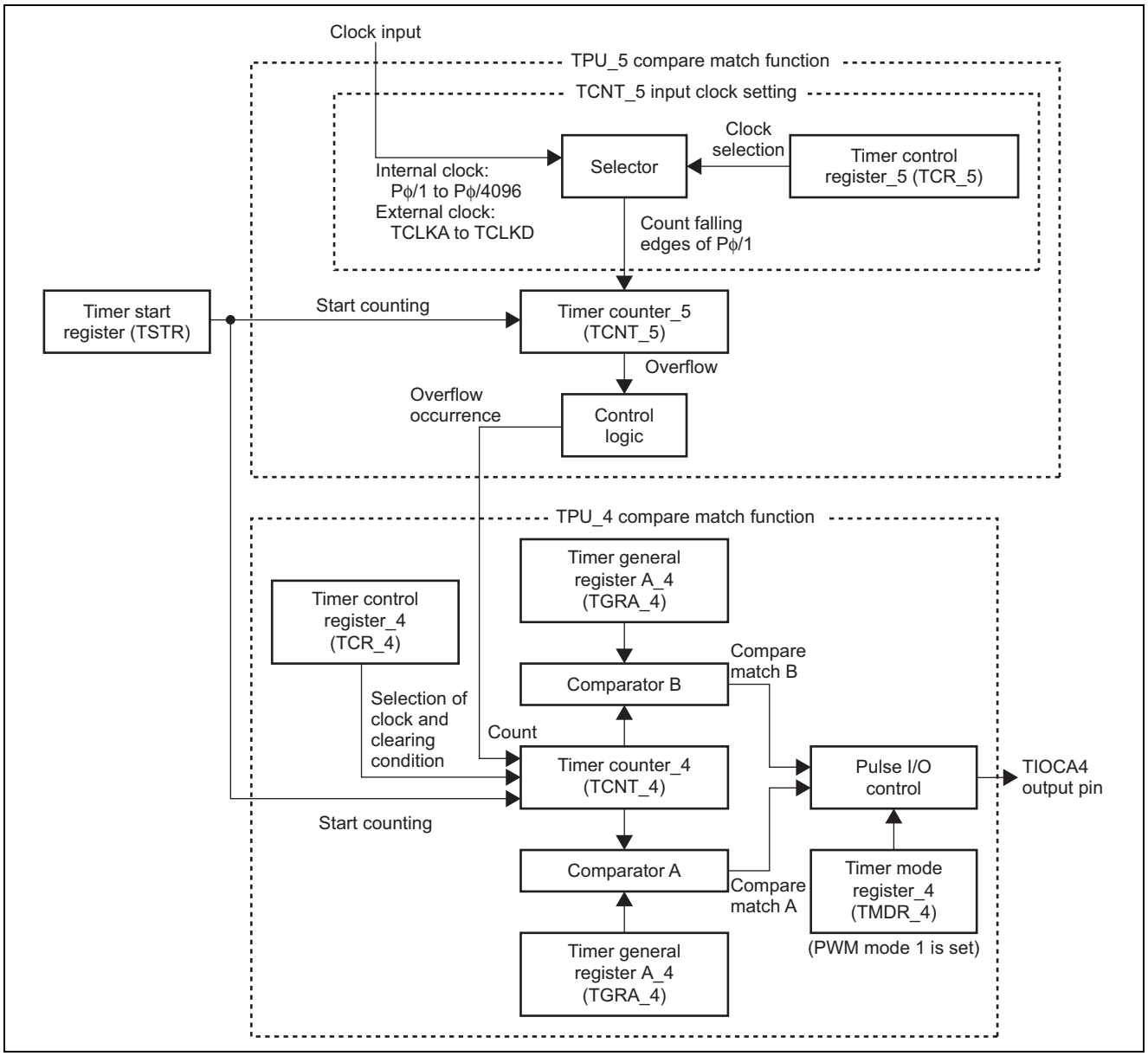


Figure 2 Block Diagram of Long-Period Pulse Output

4. Description of Operation

Figure 3 illustrates the operation of long-period pulse output. The hardware processing and software processing of figure 3 are explained in table 3.

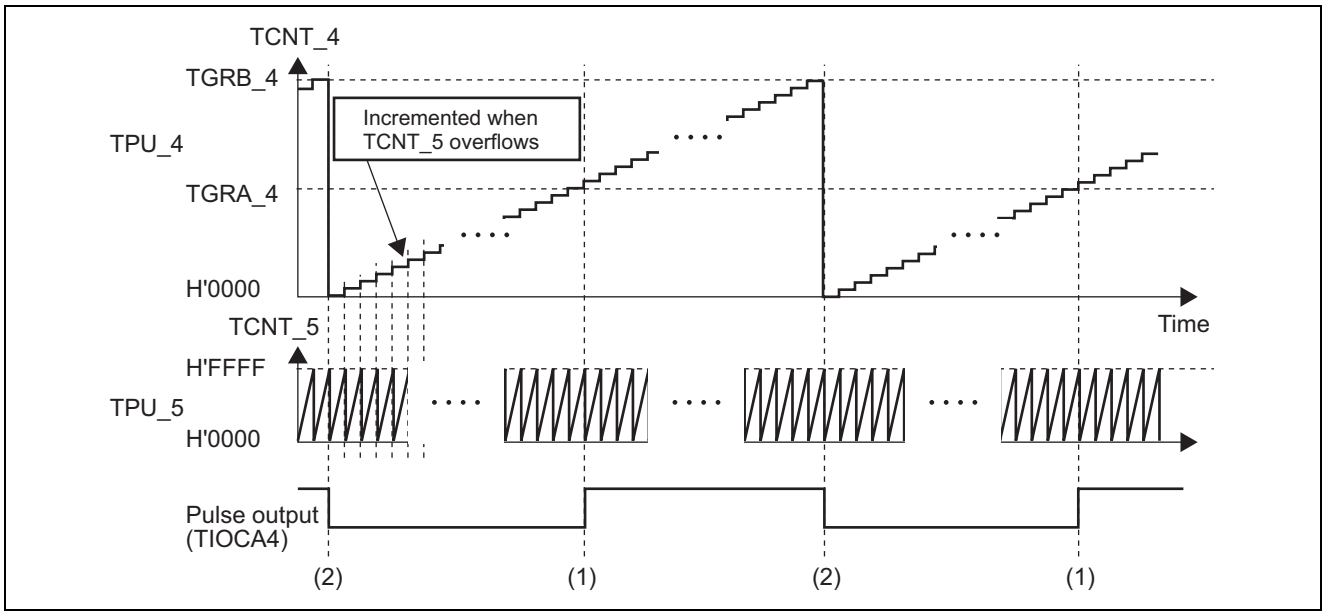


Figure 3 Operation of Long-Period Pulse Output

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	(a) Generate compare match A of TPU_4. (b) Output 1 from the TIOCA4 pin.	No processing
(2)	(a) Generate compare match B of TPU_4. (b) Clear TCNT_4. (c) Output 0 from the TIOCA4 pin.	No processing

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Makes settings for toggle output generation by compare match A and outputs pulses.

5.2 Vector Table

Table 5 Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main

5.3 Formulas for Calculation of Pulse Output Values

The pulse period and low-level width of the pulse are calculated by the formulas below.

When Pϕ = 24 MHz and TGRB_4 = H'03FF,

$$\text{Pulse period} = \frac{(\text{TGRB\_4} + 1) \times \text{TCNT\_3 overflow count}}{P\phi}$$

$$= \frac{(\text{H'3FF} + 1) \times \text{H'10000}}{24\ \text{MHz}}$$

$$= 2.79 \approx 2.8\ \text{ms}$$

When Pϕ = 24 MHz and TGRA_4 = H'00FF,

$$\text{Low-level width} = \frac{(\text{TGRA\_4} + 1) \times \text{TCNT\_3 overflow count}}{P\phi}$$

$$= \frac{(\text{H'FF} + 1) \times \text{H'10000}}{24\ \text{MHz}}$$

$$= 0.69 \approx 0.7\ \text{ms}$$

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

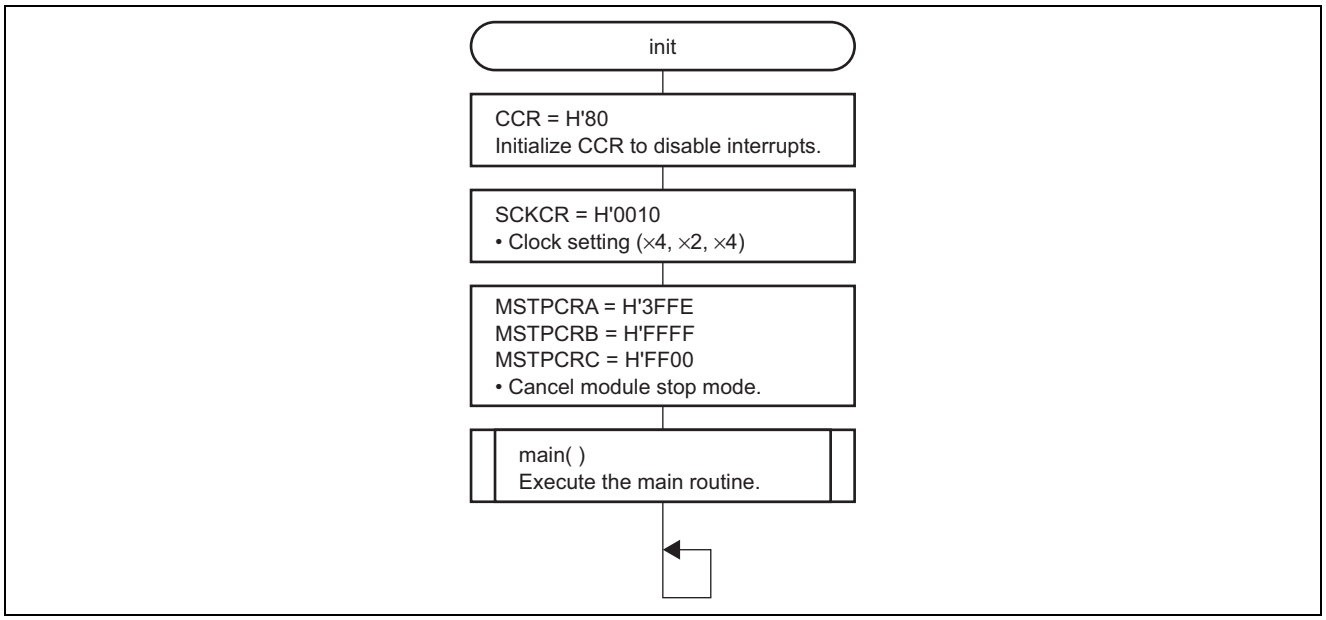
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart



5.4.2 main Function

(1) Functional overview

Main routine which sets up the cascade connection of TPU_4 and TPU_5.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port function control register 9 (PFCR9) Address: H'FFFBC9

Bit	Bit Name	Setting	R/W	Function
6	TPUMS4	0	R/W	TPU I/O Pin Multiplex Function Select Selects the TIOCA4 function. 0: Specifies P25 as the output compare output or input capture input pin 1: Specifies P24 as the input capture input pin and P25 as the output compare output pin

- Timer control register_4 (TCR_4) Address: H'FFFEE0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	1	R/W	These bits select the TCNT_4 counter clearing condition.
5	CCLR0	0	R/W	010: TCNT_4 is cleared by TGRB_4 compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	1	R/W	Timer Prescaler 2 to 0
1	TPSC1	1	R/W	These bits select the TCNT_4 counter clock.
0	TPSC0	1	R/W	111: TCNT_5 overflow/underflow signal

- Timer mode register_4 (TMDR_4) Address: H'FFFEE1

Bit	Bit Name	Setting	R/W	Function
3	MD3	0	R/W	Modes 3 to 0
2	MD2	0	R/W	These bits set the timer operating mode.
1	MD1	1	R/W	0010: PWM mode 1*
0	MD0	0	R/W	Note: * When TPU_4 is set in PWM mode 1, TGRA_4 and TGRB_4 are used in pair to generate PWM output on the TIOCA4 pin.

- Timer I/O control register_4 (TIOR_4) Address: H'FFFEE2

Bit	Bit Name	Setting	R/W	Function
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	1	R/W	These bits specify the function of TGRB_4.
5	IOB1	0	R/W	0101: TGRB_4 functions as an output compare register.
4	IOB0	1	R/W	In PWM mode 1, the TIOCA4 pin outputs 0 on compare match.
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of TGRA_4.
1	IOA1	1	R/W	0010: TGRA_4 functions as an output compare register.
0	IOA0	0	R/W	The TIOCA4 pin outputs 0 as the initial output and outputs 1 on compare match.

- Timer counter_4 (TCNT_4) Address: H'FFFEE6
  Function: 16-bit readable/writable counter
  Setting: H'0000

- Timer general register A_4 (TGRA_4) Address: H'FFFEE8
  Function: Used as an output compare register.
  Setting: H'0100

- Timer general register B_4 (TGRB_4) Address: H'FFFEEA
  Function: Used as an output compare register.
  Setting: H'0300

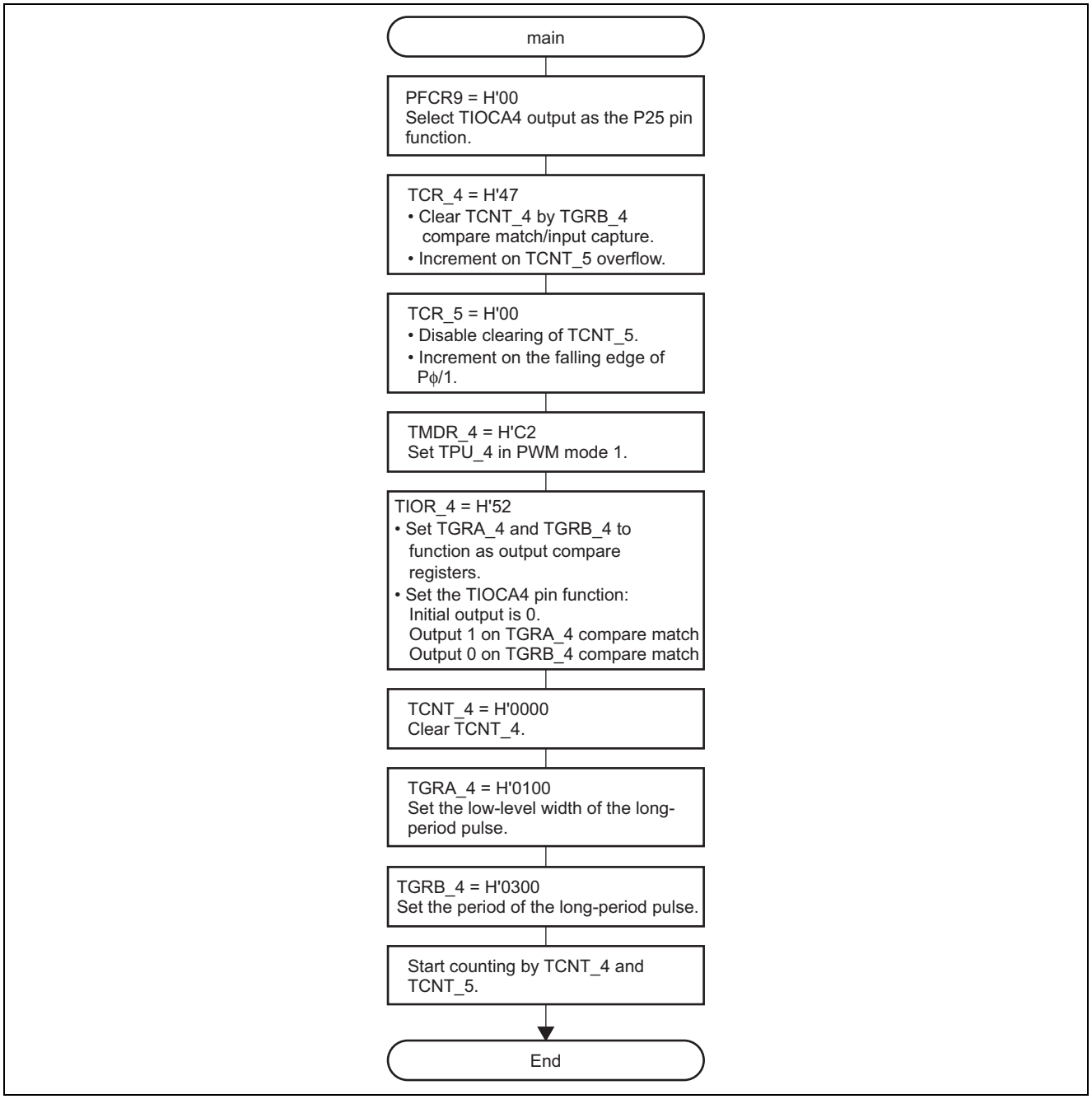
- Timer start register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	1	R/W	These bits start or stop the operation of the corresponding
3	CST3	1	R/W	TCNT.
2	CST2	0	R/W	0: Stops counting by TCNT_5 to TCNT_0
1	CST1	0	R/W	1: Starts counting by TCNT_5 to TCNT_0
0	CST0	0	R/W	

- Timer control register_5 (TCR_5) Address: H'FFFFF0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT_5 counter clearing condition.
5	CCLR0	0	R/W	000: Clearing of TCNT_5 is disabled
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT_5 counter clock.
0	TPSC0	0	R/W	000: Internal clock Pϕ/1

(5) Flowchart


main
PFCR9 = H'00
Select TIOCA4 output as the P25 pin function.
TCR_4 = H'47
• Clear TCNT_4 by TGRB_4 compare match/input capture.
• Increment on TCNT_5 overflow.
TCR_5 = H'00
• Disable clearing of TCNT_5.
• Increment on the falling edge of Pϕ/1.
TMDR_4 = H'C2
Set TPU_4 in PWM mode 1.
TIOR_4 = H'52
• Set TGRA_4 and TGRB_4 to function as output compare registers.
• Set the TIOCA4 pin function:
Initial output is 0.
Output 1 on TGRA_4 compare match
Output 0 on TGRB_4 compare match
TCNT_4 = H'0000
Clear TCNT_4.
TGRA_4 = H'0100
Set the low-level width of the long-period pulse.
TGRB_4 = H'0300
Set the period of the long-period pulse.
Start counting by TCNT_4 and TCNT_5.
End

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Revision Record

		Description	
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1.00	Sep.11.06	—	First edition issued

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