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April 1st, 2010
Renesas Electronics Corporation

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# R8C/Tiny Series

## General-purpose Program for Example for Initial Setting Assembler

### 1. Abstract

This program is an example of initial settings accomplished by using the directive commands of the assembler.

### 2. Introduction

The program shown here consists of the following:

1. Map file information output
2. Global symbol name specification
3. Numeric symbol definition
4. RAM area allocation
5. Bit symbol definition
6. Initial setup program
   - Interrupt stack pointer setting
   - FB register setting
   - SB register setting
   - INTB register setting
   - RAM clear
7. Peripheral I/O interrupt vector table
8. Nonmaskable interrupt fixed vector table

The following shows the range of the FB and SB relative addresses in this program.

<table>
<thead>
<tr>
<th>FB</th>
<th>380H to 47FH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-128</td>
</tr>
<tr>
<td></td>
<td>↑</td>
</tr>
<tr>
<td></td>
<td>-400H</td>
</tr>
<tr>
<td></td>
<td>↓</td>
</tr>
<tr>
<td></td>
<td>+ 127</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SB</th>
<th>480H to 57FH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>480H</td>
</tr>
<tr>
<td></td>
<td>↓</td>
</tr>
<tr>
<td></td>
<td>+ 255</td>
</tr>
</tbody>
</table>

This program can also be used when operating other microcomputers within the R8C/10 group, provided they have the same vector table as the R8C microcomputers. However, some functions may have been modified. Refer to the User’s Manual for details. Use functions covered in this Application Note only after careful evaluation.
3. Flowchart

- RESET
  - Set interrupt stack pointer (ISP) address
  - Set frame base register (FB) address
  - Set static base register (SB) address
  - Set interrupt table register (INTB) address
  - Clear RAM
  - Interrupt enabled

EXIT
4. The example of a reference program

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

; R8C Program Collection No. 30
; CPU : R8C/Tiny

FUNCTION

; Title: Initial settings using assembler's directive commands

Outline:
(1) Assemble control
(2) Address control
(3) Link control
(4) List control
(5) Branch instruction optimization control

Notes:

; Map file information output

; .VER 'Ver1.02' ; 'Ver1.02' is output when generating map file

; Global symbol name specification

; [Global symbol specification]

; .GLB RUTINE ; Externally referenced symbol
; .GLB MAIN ; Public symbol

; [Global bit symbol specification]

; .BTGLB P3_0 ; Externally referenced symbol
; .BTGLB P0_7 ; Public symbol

; Numeric symbol definition

; VramTOP .EQU 000400H ; Declares start address of RAM
; VramEND .EQU 0006FFH ; Declares last address of RAM
; Vistack .EQU 000600H ; Interrupt stack pointer
; VproTOP .EQU 00D000H ; Declares start address of program
; VECTOR_ADR .EQU 00FE00h ; Declares start address of variable vector table
; FIX_VECTOR .EQU 00FFDCh ; Declares fixed interrupt vector address

; CNT125ms .EQU 125 ; Sets 125 in CNT125ms

; AUTOchar .EQU -8 ; Sets -8 in AUTOchar

; .FORM 45,160 ; [List output control instruction]
; ; Specifies 45 lines, 160 columns per page of list file
.LIST ON ; [List output control]
;
.PAGE 'RAM' ; [List page break and title specification]
.SECTION MEMORY,DATA ; [Section name specification]
; Declarers DATA attribute section of section name "MEMORY"
; Outputs assembler list
.ORG VramTOP ; [Absolute address setting]
; Sets location to 400H
;----------------------------------------------------------;
; RAM area allocation
;----------------------------------------------------------;
;
CHAR: .BLKB 10 ; Allocates 10-byte area
;
;
SHORT: .BLKW 10 ; Allocates 20-byte area
;
;
ADDR: .BLKA 10 ; Allocates 30-byte area
;
;
LONG: .BLKL 10 ; Allocates 40-byte area
;
;
SFLOAT: .BLKF 10 ; Allocates 40-byte area
;
;
DFLOAT: .BLKD 10 ; Allocates 80-byte area
;
;
CHECK: .BLKW 10 ;
;
;----------------------------------------------------------;
; Bit symbol definition
;----------------------------------------------------------;

BIT4 .BTEQU 4,CHAR ; Sets bit 4 of displacement CHAR to BIT4
MSB .BTEQU 15,SHORT ; Sets bit 15 of displacement SHORT to MSB
PO_7 .BTEQU 7,3E0H ; Sets bit 7 at address 3E0 to P0_7
;
; .SECTION PROG,CODE ; Declares CODE attribute section of section name "PROG"
.ORG VproTOP ; [Branch instruction optimize specification]
.OPTJ OFF ; Does not optimize branch instruction after this line
; .FB VramTOP ; [Assumption of FB register value]
; .SB VramTOP+80H ; [Assumption of SB register value]
; .FBSYM SHORT ;
; .SBSYM CHECK ;
;----------------------------------------------------------;
; Program start
;----------------------------------------------------------;
R8C/Tiny Series
General-purpose Program for Example for Initial Setting Assembler

RESET:
LDC  #Vstack,ISP ; Sets interrupt stack pointer
LDC  #VramTOP,FB ; Sets frame base register
LDC  #VramTOP+80H,SB ; Sets static base register
LDINTB #VECTOR_ADDR ; Sets interrupt table register
MOV.W #0,R0 ; Sets store data (0)
MOV.W #((VramEND+1)-VramTOP)/2,R3 ; Sets number of transfers performed
MOV.W #VramTOP,A1 ; Sets address where to start storing
SSTR.W ; Executes clearing of RAM
FSET I ; Enables interrupt

===============================================================
; Main program ;
===============================================================
MAIN:
MOV.W #1234H,SHORT
MOV.W #5678H,CHECK
JSR ROUTINE
BSET P0_7

; (Here is your program.)

ROUTINE:

; (Here is your program.)

RTS

NOTUSE:

; (Here is your program.)

RTS

.PAGE  'VECTOR'
.SECTION  UIINTER,ROMDATA ; Declares FOMDATA attribute section of section name "UIINTER"
.org  VECTOR_ADR
;-------------------------------;
; Peripheral I/O interrupt vector table ;
;-------------------------------;
.word  NOTUSE ; BRK instruction (vector 0)
.org  (VECTOR_ADDR+52)
.word  NOTUSE ; Key input interrupt (vector 13)
General-purpose Program for Example for Initial Setting Assembler

```
.word NOTUSE ; A-D (vector 14)
.org (VECTORADR+68)
.word NOTUSE ; UART0 transmit (vector 17)
.word NOTUSE ; UART0 receive (vector 18)
.word NOTUSE ; UART1 transmit (vector 19)
.word NOTUSE ; UART1 receive (vector 20)
.word NOTUSE ; INT2 (vector 21)
.word NOTUSE ; Timer X (vector 22)
.word NOTUSE ; Timer Y (vector 23)
.word NOTUSE ; Timer Z (vector 24)
.word NOTUSE ; INT1 (vector 25)
.word NOTUSE ; INT3 (vector 26)
.word NOTUSE ; Timer C (vector 27)
.org (VECTORADR+116)
.word NOTUSE ; INT0 (vector 29)
.org (VECTORADR+128)
.word NOTUSE ; vector 32 (for user or MR30)
.word NOTUSE ; vector 33 (for user or MR30)
.word NOTUSE ; vector 34 (for user or MR30)
.word NOTUSE ; vector 35 (for user or MR30)
.word NOTUSE ; vector 36 (for user or MR30)
.word NOTUSE ; vector 37 (for user or MR30)
.word NOTUSE ; vector 38 (for user or MR30)
.word NOTUSE ; vector 39 (for user or MR30)
.word NOTUSE ; vector 40 (for user or MR30)
.word NOTUSE ; vector 41 (for user or MR30)
.word NOTUSE ; vector 42 (for user or MR30)
.word NOTUSE ; vector 43 (for user or MR30)
.word NOTUSE ; vector 44 (for user or MR30)
.word NOTUSE ; vector 45 (for user or MR30)
.word NOTUSE ; vector 46 (for user or MR30)
.word NOTUSE ; vector 47 (for user or MR30)

.SECTION INTER,ROMDATA ; Declares FOMDATA attribute section of section name "INTER"
.ORG FIX_VECTOR ; Sets location to FFFDCH
.LWORD NOTUSE ; FFFDC to F Undefined instruction
.LWORD NOTUSE ; FFFE0 to 3 Overflow
.LWORD NOTUSE ; FFFE4 to 7 BRK instruction
.LWORD NOTUSE ; FFFE8 to B Address coincidence
.LWORD NOTUSE ; FFFEC to F Single stepping
.LWORD NOTUSE ; FFFF0 to 3 Watchdog timer
.LWORD NOTUSE ; FFFF4 to 7 Debugger
.LWORD NOTUSE ; FFFF8 to B NMI
.LWORD RESET ; FFFFC to F Reset
```

; End of assemble direction

;-----------------------------------------;
; REJ05B0391-0100Z/Rev.1.00
December 2003
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5. Reference

SOFTWARE MANUAL
R8C/Tiny Series SOFTWARE MANUAL
(Acquire the most current version from Renesas web-site)

6. Web-site and contact for support

Renesas Web-site

http://www.renesas.com/jpn

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Mail to: support_apl@renesas.com
<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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</thead>
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<tr>
<td>1.00</td>
<td>Dec.29, 2003</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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