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# R8C/13 Group

## Flash Rewrite Using EW1 Mode (Data "FFh" Search)

## 1. Abstract

This application note shows a data flash rewrite program using EW1.
In this application note, Block A and Block B in flash memory are shown as data flash.

## 2. Introduction

An example described in this document supports the following microcomputer.

Microcomputer : R8C/13 Group

This program can also be used when operating other microcomputers within the R8C/Tiny series, provided they have the same SFR (Special Function Registers) and data flash as the R8C/13 microcomputers. However, some functions may have been modified. Refer to the User's Manual for details.

Use functions covered in this Application Note only after careful evaluation.

## 3. Description of Application Example

### 3.1 Flash Memory Overview

A flash memory has two rewrite modes; CPR rewrite mode and standard serial I/O mode.
A CPU rewrite mode is used in this application note.

**Table 1. Overview of Flash Memory Performance**

| Item | | Performance |
|---|---|---|
| Flash Memory Operation Mode | | 2 Modes (CPU Rewrite Mode, Standard Serial I/O Mode) |
| Erase Block | | See **Figure 1 R8C/13 Memory Map** |
| Program Method | | Byte Unit |
| Erase Method | | Block Erase |
| Program, Erase Control Method | | Program and erase controlled by software command |
| Protect Method | | Blocks 0 and 1 protected by the FMR02 bit in the FMR0 register |
| | | Individual protects to Block 0 and 1 by the FMR15 and 16 bits in the FMR1 register |
| Number of Commands | | 5 commands |
| Program and Erase Endurance (Block Erase Endurance) | Block 0 and Block 1 (Program Area) | 100 times |
| | Block A and Block B (Data Area) | 10,000 times |
| ROM Code Protect | | Applicable for Standard Serial I/O Mode |

**Table 2. Overview of Flash Memory Rewrite Mode**

| Flash Memory Rewrite Mode | CPU Rewrite Mode | Standard Serial I/O Mode |
|---|---|---|
| Function | User ROM area is rewritten by executing software commands from the CPU<br>EW0 Mode : Rewritable in any area other than flash memory<br>EW1 Mode : Rewritable in flash memory | User ROM area is rewritten by using a dedicated serial programmer<br>Standard Serial I/O Mode 1: Clock Synchronous Serial I/O<br>Standard Serial I/O Mode 2: UART |
| Area can be rewritten | User ROM Area | User ROM Area |
| Operation Mode | Single Chip Mode | Boot Mode |
| ROM Programmer | - | Serial Programmer |

## 3.2 Memory Map

A user ROM area built in R8C/13 consists of 4 blocks; block A, B, 0 and 1. Figure 1 shows a memory map.
In this application note, a data flash ROM area of block A and B is used.

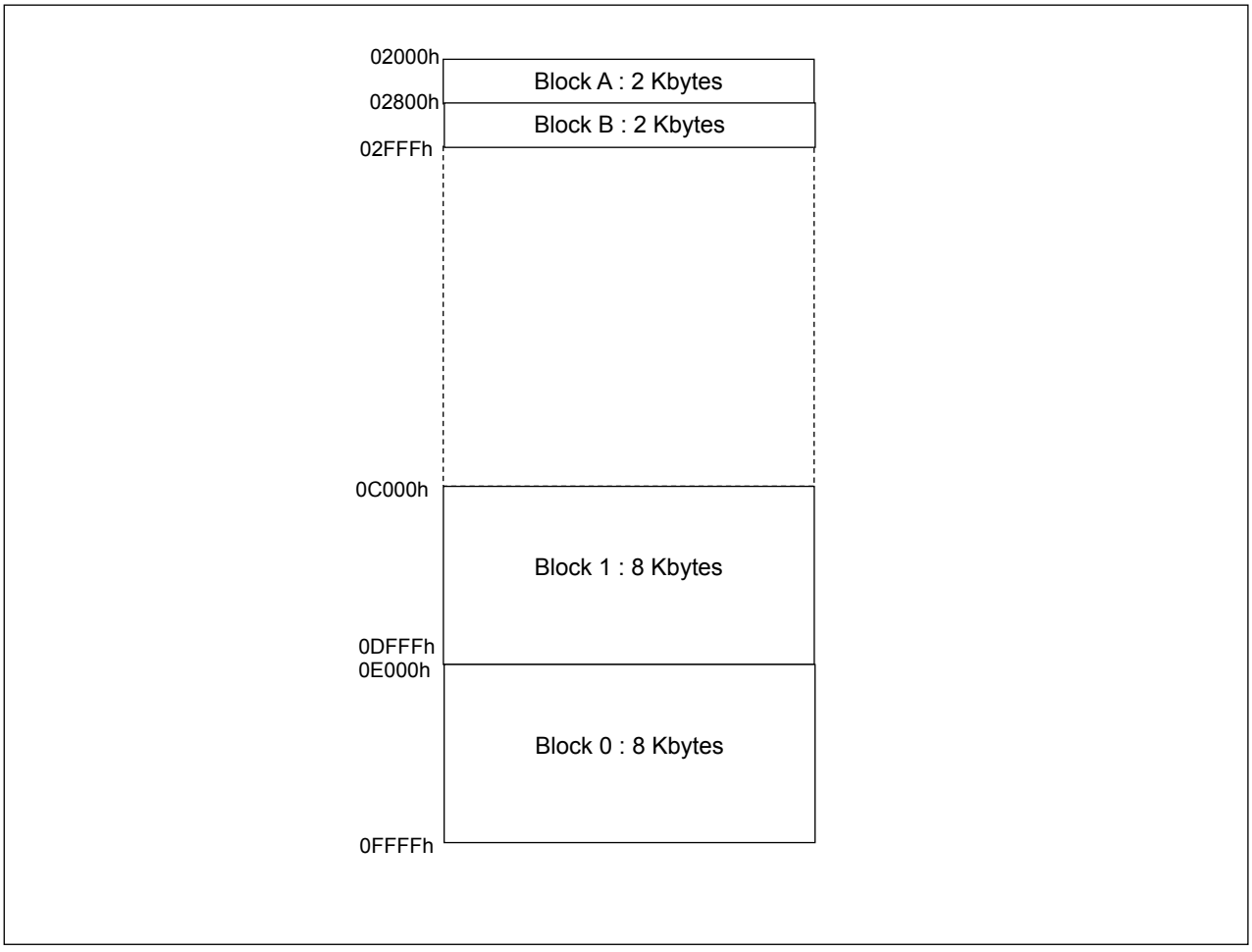



**Figure 1. R8C/13 Memory Map**

## 3.3 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly without using a ROM programmer, etc Execute the program and the Block Erase commands only on each block in the user ROM area.
In CPU rewrite mode, the user ROM area can be operated in either erase write 0 mode (EW0 mode) and erase write 1 mode (EW1 mode). Table 3 shows the difference between EW0 mode and EW1 mode.
EW1 mode is used in this application note.

**Table 3. EW0 Mode and EW1 Mode**

| Item | EW0 Mode | EW1Mode |
|---|---|---|
| Operation Mode | Single Chip Mode | Single Chip Mode |
| Area where rewrite control program can be placed | User ROM Area | User ROM Area |
| Area where rewrite control program can be executed | Rewrite control program needs to be transferred to any area other than the flash memory (e.g., RAM) | The rewrite control program can be executed in the user ROM area |
| Area which can be rewritten | User ROM Area | User ROM Area<br>(This excludes blocks with the rewrite control program) |
| Software Command Restriction | None | ·Program and Block Erase<br>(Execution disabled to blocks with the rewrite control program)<br>·Read status register command execution disabled |
| Modes after Programming or Erasing | Read Status Register Mode | Read Array Mode |
| CPU Status during Auto Write and Auto Erase | Operation | Maintains Hold State<br>(I/O ports maintain the state before the command is executed) |
| Flash Memory Status Detection | · Read the FMR00, FMR06 and FMR07 bits in the FMR0 register by a program<br>· Execute the read status register command and read the SR7, SR5 and SR4 bits in the SRD register | Read the FMR00, FMR06 and FMR07 bits in the FMR0 register by a program |

### 3.3.1 EW0 Mode

The microcomputer enters CPU rewrite mode by setting the FMR01 bit in the FMR0 register to “1” (CPU rewrite mode enabled) and is ready to accept software commands. EW0 mode is selected by setting the FMR11 bit in the FMR1 register to “0”. The software commands control programming and erasing. The FMR0 register or the SRD register indicates whether a programming or erasing operation is completed.

### 3.3.2 EW1 Mode

EW1 mode is selected by setting the FMR11 bit to “1” (EW1 mode) after the FMR01 bit is set to “1” (CPU rewrite mode enabled). The FMR0 register indicates whether a programming or erasing operation is completed. In EW1 mode, do not execute the software command in the read status register.

## 3.4 Associated Register Configuration

Figure 2 shows the required registers to control flash memory

### Flash Memory Control Register 0

| b7 b6 b5 b4 b3 b2 b1 b0 | Symbol | Address | After reset |
|---|---|---|---|
| 0 0 | FMR0 | 01B7h | XX00 0001b |

| Bit Symbol | Bit Name | Function | RW |
|---|---|---|---|
| FMR00 | RY/$\overline{BY}$ Status Flag | 0 : Busy (During writing or erasing)<br>1 : Ready | RO |
| FMR01 | CPU Rewrite Mode Select Bit(1) | 0 : CPU rewrite mode disabled<br>1 : CPU rewrite mode enabled | RW |
| FMR02 | Block 0 and 1 Rewrite Enable Bit(2) | 0 : Rewrite Disabled<br>1 : Rewrite Enabled | RW |
| FMSTP | Flash Memory Stop Bit(3,5) | 0 : Starts flash memory<br>1 : Stops the flash memory<br>(Enters low-power consumption state and flash memory is reset) | RW |
| ——— (b5-b4) | Reserved Bit | Set to “0”. | RW |
| FMR06 | Program Status Flag(4) | 0 : Completed successfully<br>1 : Teminated by error | RO |
| FMR07 | Erase Status Flag(4) | 0 : Completed successfully<br>1 : Teminated by error | RO |

NOTES :
1. When setting this bit to “1”, set to “1” immediately after setting it first to “0”. Do not generate an interrupt between setting the bit to “0” and setting it to “1”. Set the microcomputer in read array mode before writing to this bit.
2. Set the FMR01 bit to “1” immediately after setting it first to “0” while the FMR01 bit is set to “1” (CPU rewrite mode enabled). Do not generate an interrupt between setting the this bit to “0” and setting it to “1”.
3. Set this bit by a program in a space other than the flash memory.
4. This bit is set to “0” by executing the clear status command.
5. This bit is enabled when the FMR01 bit is set to “1” (CPU rewrite mode enabled). The FMSTP bit is set to “1” when the FMR01 bit is set to “0” (CPU rewrite mode disabled) and the FMSTP bit is set to “1”. The flash memory does not enter low-power consumption state nor is reset.

### Flash Memory Control Register 1

| b7 b6 b5 b4 b3 b2 b1 b0 | Symbol | Address | After reset |
|---|---|---|---|
| 1 0 0 0 | FMR1 | 01B5h | 1000 000Xb |

| Bit Symbol | Bit Name | Function | |
|---|---|---|---|
| ——— (b0) | Reserved Bit | When read, its content is indeterminate. | RO |
| FMR11 | EW1 Mode Select Bit(1,2) | 0 : EW0 mode<br>1 : EW1 mode | RW |
| ——— (b4-b2) | Reserved Bit | Set to “0”. | RW |
| FMR15 | Block 0 Rewrite Disabled Bit(2,3) | 0 : Rewrite enabled<br>1 : Rewrite disabled | RW |
| FMR16 | Block 1 Rewrite Disabled Bit(2,3) | 0 : Rewrite enabled<br>1 : Rewrite disabled | RW |
| ——— (b7) | Reserved Bit | Set to “1”. | RW |

NOTES :
1. Set the FMR01 bit to “1” immediately after setting it first to “0” while the FMR01 bit is set to “1” (CPU rewrite mode enabled). Do not generate an interrupt between setting the this bit to “0” and setting it to “1”.
2. When setting the FMR01 bit to “0” (CPU rewrite mode disabled), this bit is set to “0”.
3. When the FMR01 bit is set to “1” (CPU rewrite mode enabled), the FMR15 and FMR16 bits are written. When setting this bit to “0”, set this bit to “0” immediately after setting it first to “1”. When setting this bit to “1”, set this bit to “1”.

**Figure 2. Associated Register**

## 3.5 Software Command

The software commands are described below. Read or write the command code and data in 8-bit unit.

**Table 4. Software Commands**

| Software Commands | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|
| | Mode | Address | Data ($D_7$ to $D_0$) | Mode | Address | Data ($D_7$ to $D_0$) |
| Read Array | Write | × | FFh | | | |
| Read Status Flag | Write | × | 70h | Read | × | SRD |
| Clear Status Flag | Write | × | 50h | | | |
| Program | Write | WA | 40h | Write | WA | WD |
| Block Erase | Write | × | 20h | Write | BA | D0h |

SRD : Status Register ($D_7$ to $D_0$)

WA : Address to be written (The address specified in the first bus cycle is the same address specified in the second bus cycle)

WD : 8-bit write data

BA : Highest -order block address

× : An even address in the user ROM area

### 3.5.1 Read Array Command

The read array command reads the flash memory.

By writing “FFh” in the first bus cycle, read array mode is entered. Content of a specified address can be read in 8-bitunit after the next bus cycle. The microcomputer remains in read array mode until another command is written. Therefore, contents from multiple addresses can be read consecutively.

### 3.5.2 Read Status Register Command

The read status register command reads the SRD register.

By writing “70h” in the first bus cycle, the SRD register can be read in the second bus cycle. Read an address in the user ROM area. In EW1 mode, do not execute this command.

### 3.5.3 Clear Status Register Command

The clear status register command reads the SRD register.

By writing “50h” in the first bus cycle, the FMR06 to FMR07 bits in the FMR0 register and the SR4 to SR5 bits in the SRD register are set to “0”.

### 3.5.4 Program

The program command writes 1-byte data to the flash memory.
By writing “40h” in the first bus cycle and data to the write address in the second bus cycle, an auto programming operation (data program and verify) start. Set the address value specified in the first bus cycle to the same address as the write address specified in the second bus cycle.
The FMR00 bit in the FMR0 register indicates whether an auto programming operation is completed. The FMR00 bit is set to“0” during auto programming and “1” when an auto programming operation is completed.
After an auto programming is completed, the FMR06 bit in the FMR0 register indicates whether an auto programming operation is completed. Do not write additions to the programmed address. When the FMR02 bit in the FMR0 register is set to “0” (rewrite disabled) or the FMR02 bit is set to “1” (rewrite enabled) and the FMR15 bit in the FMR1 register is set to “1” (rewrite disable), the program command on the block0 can not be acknowledged. When the FMR16 bit is set to “1” (rewrite disabled), the program command on the block1 can not be acknowledged. In EW1 mode, do not execute this command to any address at which the rewrite control program is located.

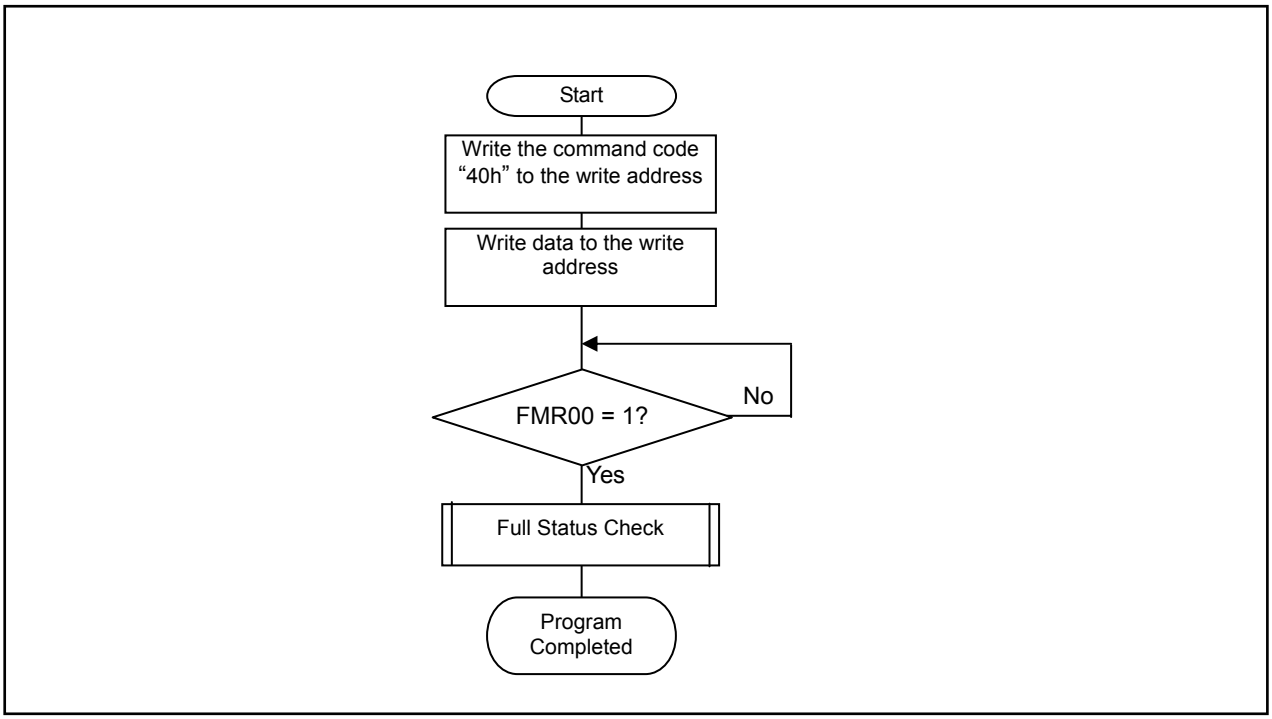



**Figure 3. Program Flow Chart**

### 3.5.5 Block Erase

By writing “20h” in the first bus cycle and “D0h” in the second bus cycle to the highest-order address of a block, an auto erasing operation (erase and erase verify) starts in the specified block. The FMR00 bit in the FMR0 register indicates whether an auto erasing operation is completed. The FMR00 bit is set to “0” during auto erasing operation and “1” when the auto erasing operation is completed.

After the auto erasing operation is completed, the FMR07 bit in the FMR0 register indicates whether the auto erasing operation is completed. When the FMR02 bit in the FMR0 register is set to “0” (rewrite disabled) or the FMR02 bit is set to “1” (rewrite enabled) and the FMR15 bit in the FMR1 register is set to “1” (rewrite disabled), the block erase command on the block0 can not be acknowledged. When the FMR16 bit is set to “1” (rewrite disabled), the block erase command on the block1 can not be acknowledged. Figure 4 shows block erase command when the erase-suspend function is not used. In EW1 mode, do not execute this command on any address at which the rewrite control program is located.

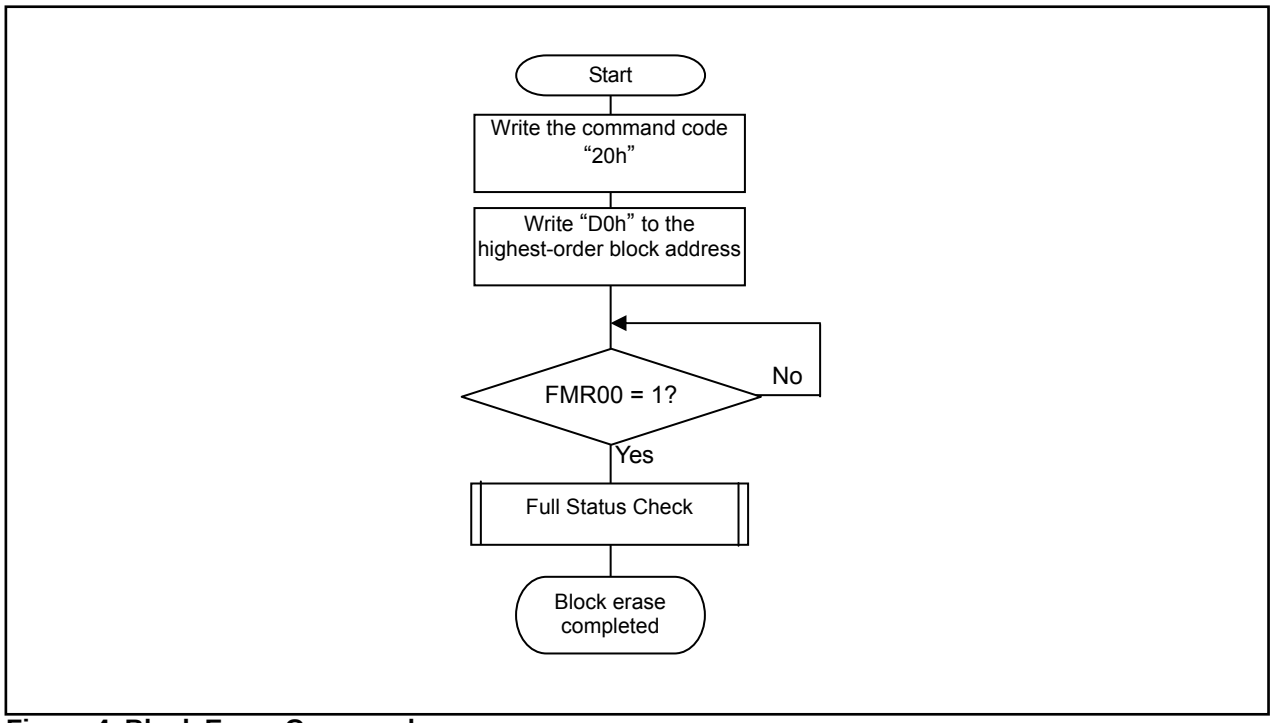



**Figure 4. Block Erase Command**

### 3.5.6 Status Register (SRD Register)

The SRD register indicates the flash memory operation state and whether an erasing or programming operation is completed successfully or in error. The FMR00, FMR06 to FMR07 bits in the FMR0 register indicate the SRD register states. Table 5 shows the SRD register. In EW0 mode, the SRD register can be read in the following cases:

(1) Any given addresses in user ROM area are read after writing the read status register command.

(2) Any given addresses in user ROM area are read when the program or block erase commands is executed until the read array command is executed.

**Table 5. SRD Register**

| Bits in SRD Register | Bits in FMR0 Register | Status Name | Definition | | After Reset |
|---|---|---|---|---|---|
| | | | "0" | "1" | |
| SR7($D_7$) | FMR00 | Sequence Status | Busy | Ready | 1 |
| SR6($D_6$) | - | Reserved Bit | - | - | - |
| SR5($D_5$) | FMR07 | Erase Status | Completed successfully | Completed in error | 0 |
| SR4($D_4$) | FMR06 | Program Status | Completed successfully | Completed in error | 0 |
| SR3($D_3$) | - | Reserved Bit | - | - | - |
| SR2($D_2$) | - | Reserved Bit | - | - | - |
| SR1($D_1$) | - | Reserved Bit | - | - | - |
| SR0($D_0$) | - | Reserved Bit | - | - | - |

$D_0$ to $D_7$ : Data buses are read when the read status register command is executed.
FMR07 (SR5) to FMR06 (SR4) bits are set to "0" by executing the clear status register command.
When the FMR07 bit (SR5) or FMR06 bit (SR4) is set to "1", the program and block erase command can not be acknowledged.

#### ●Sequence Status (SR7, FMR00 bits)

The sequence status indicates the flash memory state. This bit is set to "0" (busy) during an auto programming or auto erasing. It is set to "1" (ready) as soon as these operations are completed.

#### ●Erase Status (SR5, FMR07 bits)

Refer to **3.5.7 Full Status Check**.

#### ●Program Status (SR4, FMR06 bits)

Refer to **3.5.7 Full Status Check**.

### 3.5.7 Full Status Check

If an error occurs, the FMR06 to FMR07 bits in the FMR0 register are set to “1”, indicating a specific error. Therefore, Checking these status (full status check) indicates whether an erasing or programming operation is completed. Table 6 shows the errors and FMR0 register state. Figure 5 shows a flow chart of the full status check and handling procedure for each error.

**Table 6. Errors and FMR0 Register State**

| FMR0 register (SRD register) State | | Error | Error Occurrence Conditions |
|---|---|---|---|
| FMR07(SR5) | FMR06(SR4) | | |
| 1 | 1 | Command sequence error | · Command is written incorrectly<br>· A value other than “D0h” or “FFh” is written in the second bus cycle of the block erase command(1) |
| 1 | 0 | Erase error | · When the block erase command is executed and auto erasing operation is not completed correctly. |
| 0 | 1 | Program error | · When the program command is executed and auto programming operation is not completed correctly. |

NOTES:
1. The flash memory enters read array mode by writing command code “FFh” in the second bus cycle of these commands. The command code written in the first bus cycle becomes disabled.

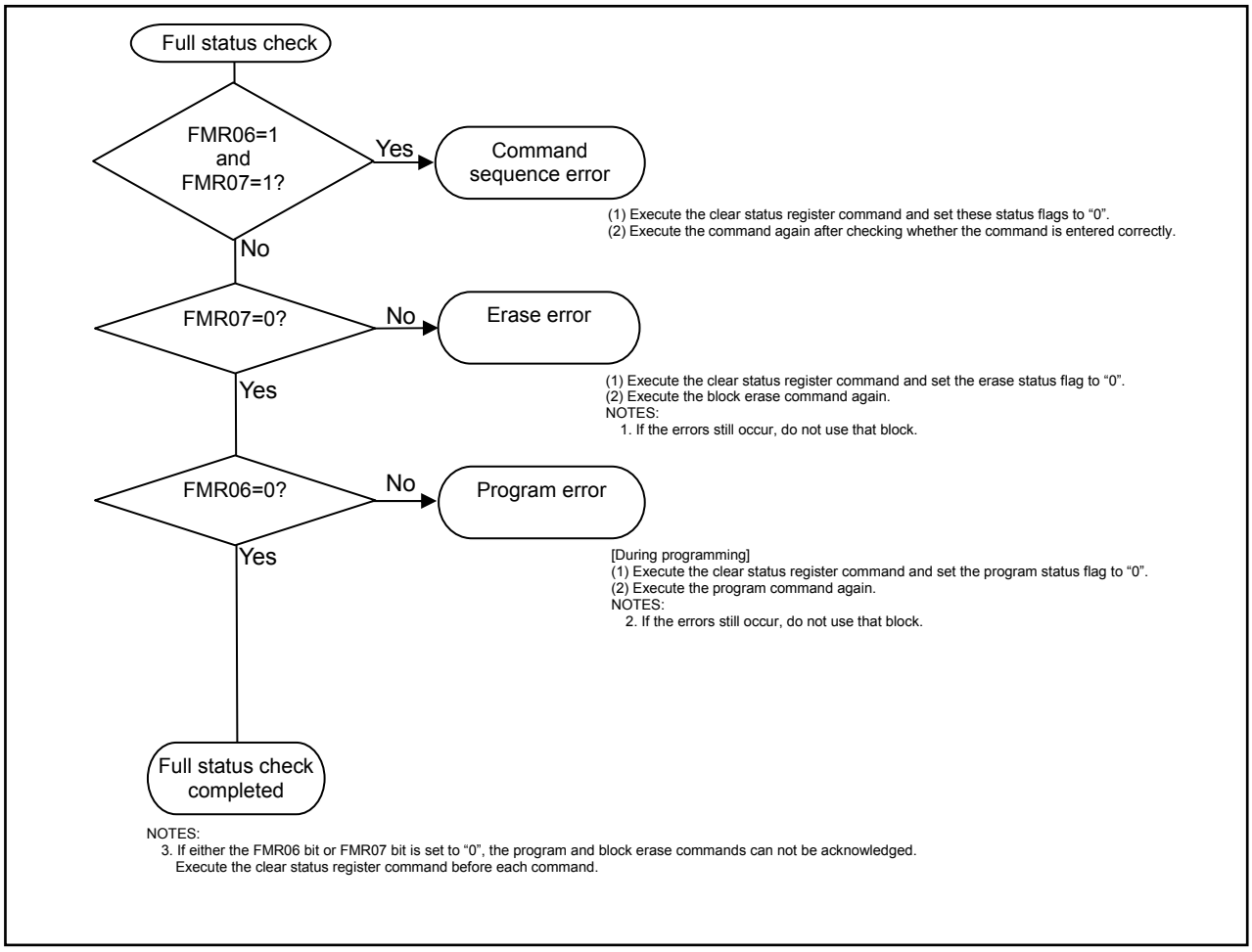



**Figure 5. Full Status Check and Handling Procedure for Each Error**

## 4. Program Overview

Dividing the data flash areas in record-unit and how to write data sequentially are described below.
This application note assumes that one record is made into 128 bytes. The block A, which is divided into 16 records from record 0 to 15, and the block B, which is divided into 16 records from record 16 to 31, are used as data area. Figure 6 shows the connection between data flash and records.

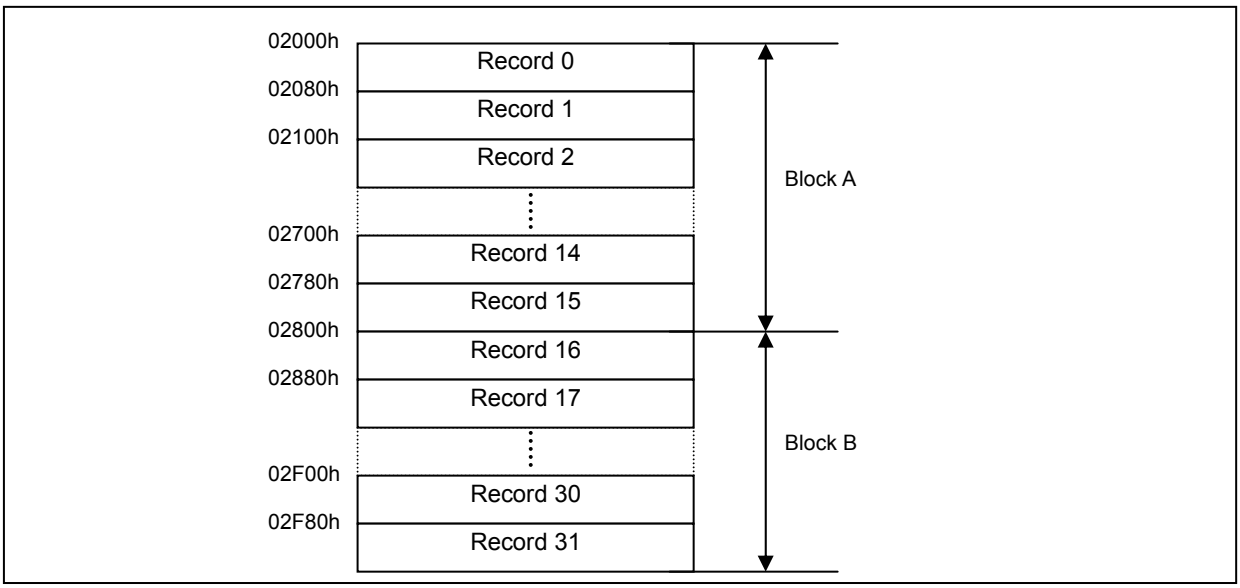



**Figure 6. Connection between Data Flash and Records**

When writing data, write from the record 0 in record-unit. Erase (block erase) all contents in the block B after writing to the record 15 and erase all contents in the block A after writing to the record 31. When writing data for the next step, write to the record 0. The data which is written into the data flash is maintained after turning the power off. Therefore, in this application note, all records (empty records) which contain data of “FFh” are searched after reset start. The following is described how to search empty records.

(1) Set the search pointer to the starting address in the record 0(Figure 7)

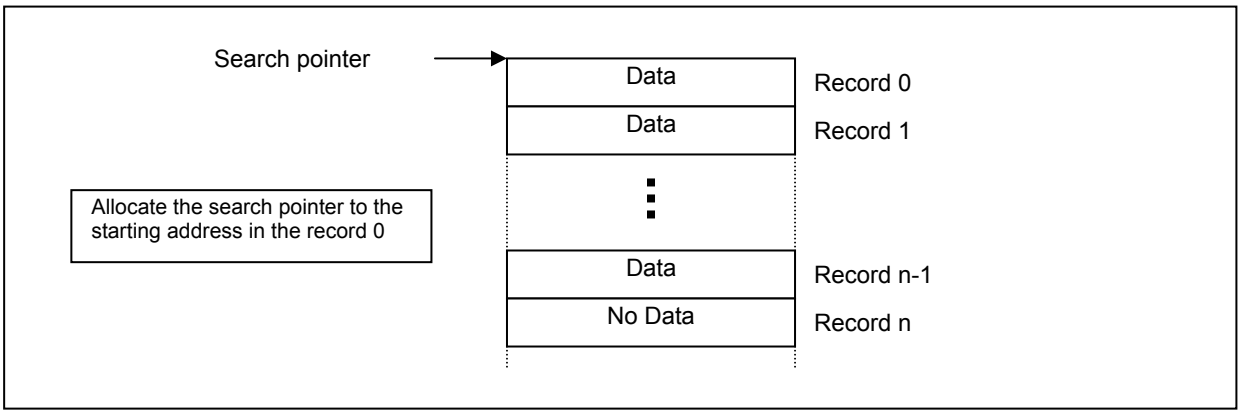



**Figure 7. Allocate the Search Pointer to the Starting Address in the Record 0**

(2) Check whether the records which the search pointer indicates are empty records (ALL“FFh”)

(3) When the records are not empty records, set the search pointer to the starting address of the next record. (Figure 8)

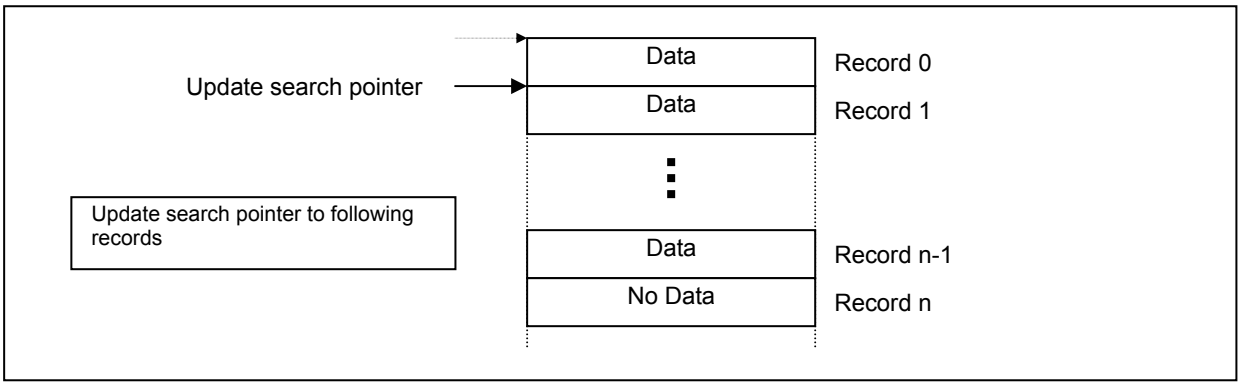



**Figure 8. Update Search Pointer**

(4) Execute (2) and (3) repeatedly until the empty records can be recognized or all records can be checked.

(5) When the empty records are recognized, set the starting address of empty records to the data write address and memorize the block which stores the records as a block select (Figure 9).

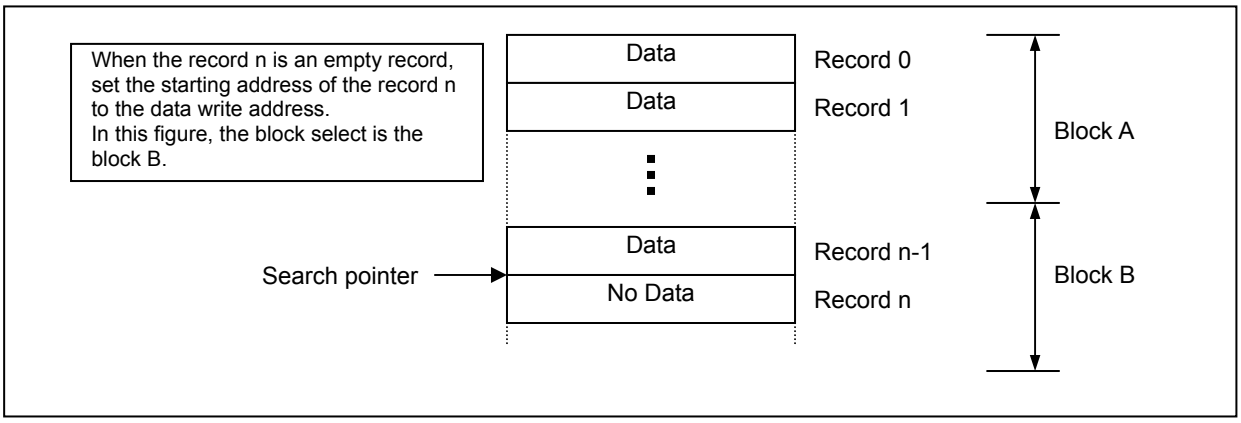



**Figure 9. When the Empty Records are Recognized**

(6) When the empty record are not recognized in the both block A and B, erase the block A and set the starting address of the record 0 to the data write address. The block A is memorized as a block select.

## 4.1 Function Table

| | | | |
|---|---|---|---|
| Declaring | void write_address_init(void) | | |
| Outline | Reset write address to default | | |
| Argument | Argument Type | | Meaning |
| | None | | |
| Use Variable (Global) | Variable Type | | Contents of Use |
| | unsigned char *write_addr | | Initial Setting |
| | unsigned char block_select | | Initial Setting |
| Return Value | Return Value Type | Value | Meaning |
| | None | | |
| Function Description | Search the empty records. Set the write address (write_addr) and block select (block_select) | | |

| | | | |
|---|---|---|---|
| Declaring | unsigned char flash_write(unsigned char *data) | | |
| Outline | Data Write Control | | |
| Argument | Argument Type | | Meaning |
| | unsigned char *data | | Table Starting Address of Write Data |
| Use Variable (Global) | Variable Type | | Contents of Use |
| | unsigned char *write_addr | | Reference/Setting |
| | unsigned char block_select | | Reference/Setting |
| Return Value | Return Value Type | Value | Meaning |
| | unsigned char | COMPLETE | Completed successfully |
| | | PROGRAM_ERR | Write Error(1) |
| | | ERASE_ERR | Erase Error(1) |
| Function Description | Update the write address (write_addr) after writing the reecord data. When the block select has no empty records, erase unused blocks and change the block select (block_select).<br>NOTES: 1. When write or erase error occurs, PROGRAM_ERR+ERASE_ERR is indicated. | | |

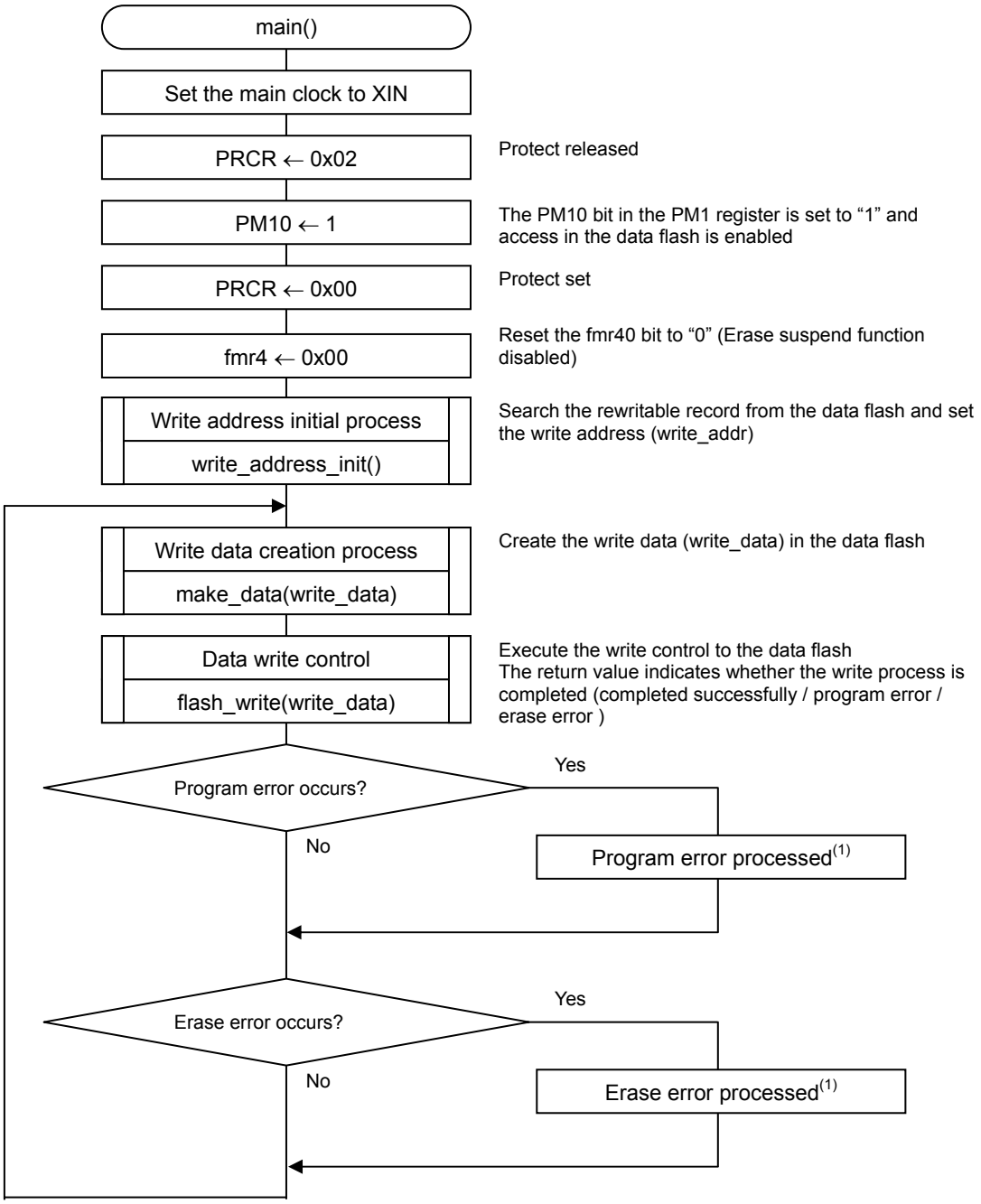
| | | | |
|---|---|---|---|
| Declaring | unsigned char block_erase(unsigned char *ers_addr) | | |
| Outline | Block Erase Process | | |
| Argument | Argument Type | | Meaning |
| | unsigned char *ers_addr | | Starting Address of Erase Block |
| Use Variable (Global) | Variable Type | | Contents of Use |
| | None | | |
| Return Value | Return Value Type | Value | Meaning |
| | unsigned char | COMPLETE | Completed successfully |
| | | ERASE_ERR | Erase Error |
| Function Description | Erase the specified block in EW1 mode | | |

| | | | |
|---|---|---|---|
| Declaring | unsigned char data_write(unsigned char *write_data) | | |
| Outline | Data Write Process | | |
| Argument | Argument Type | | Meaning |
| | unsigned char *write_data | | Table Starting Address of Write Data |
| Use Variable (Global) | Variable Type | | Contents of Use |
| | unsigned char *write_addr | | Reference |
| Return Value | Return Value Type | Value | Meaning |
| | unsigned char | COMPLETE | Completed successfully |
| | | PROGRAM_ERR | Write Error |
| Function Description | Write data for one record from write address (write_addr) in EW1 mode. | | |

| | | |
|---|---|---|
| Declaring | void make_data(unsigned char *write_data) | |
| Outline | Create the write record data in the data flash | |
| Argument | Argument Type | Meaning |
| | unsigned char *data | Table Starting Address of Write Data |
| Use Variable | Variable Type | Contents of Use |
| Return Value | None | |
| | Return Value Value | Meaning |
| | None | |
| Function Description | Create the write record data in the data flash. In this application note, nothing is processed. Add the processes if needed. | |

## 4.2 Flow Chart

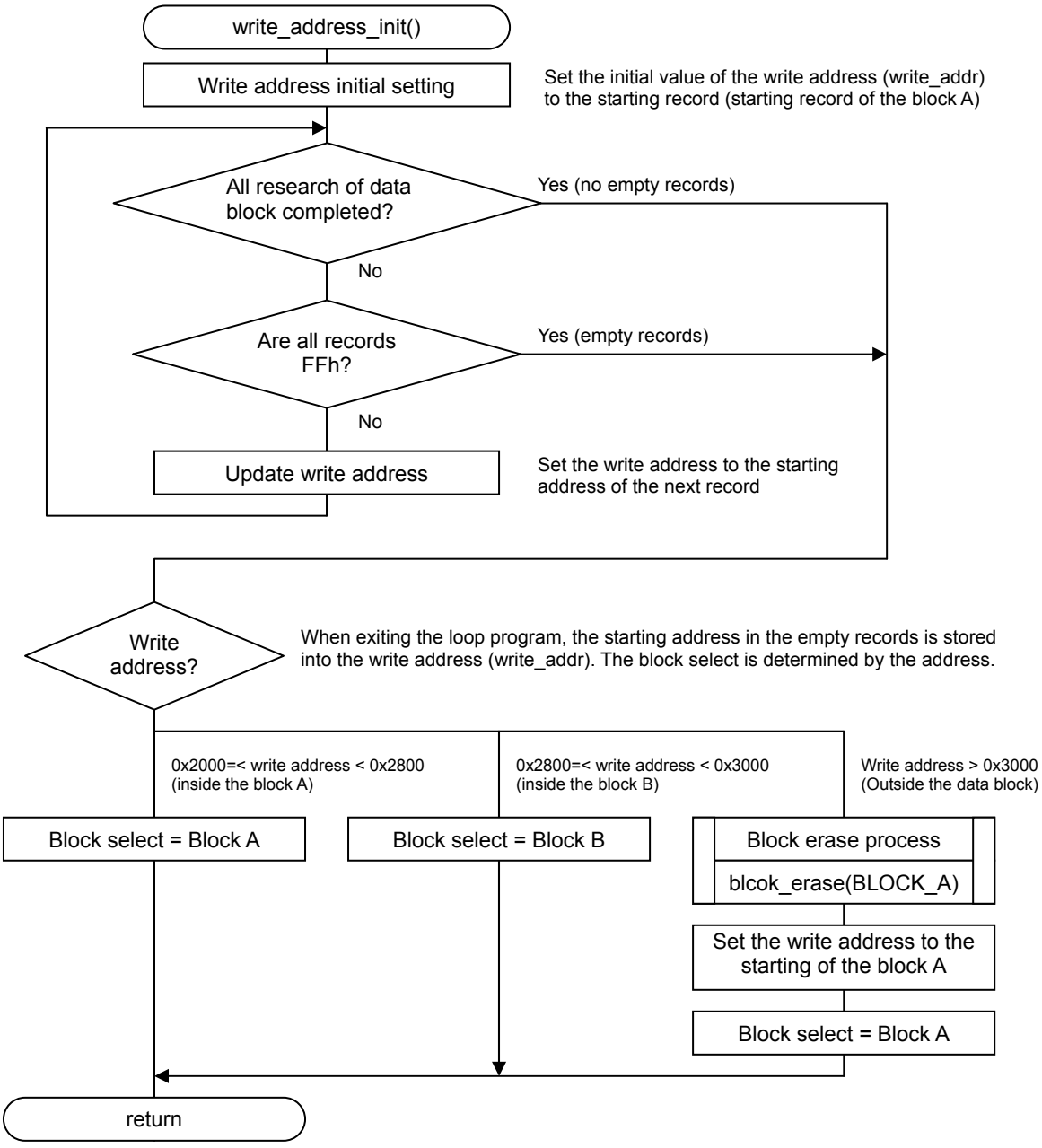
### 4.2.1 Main Function



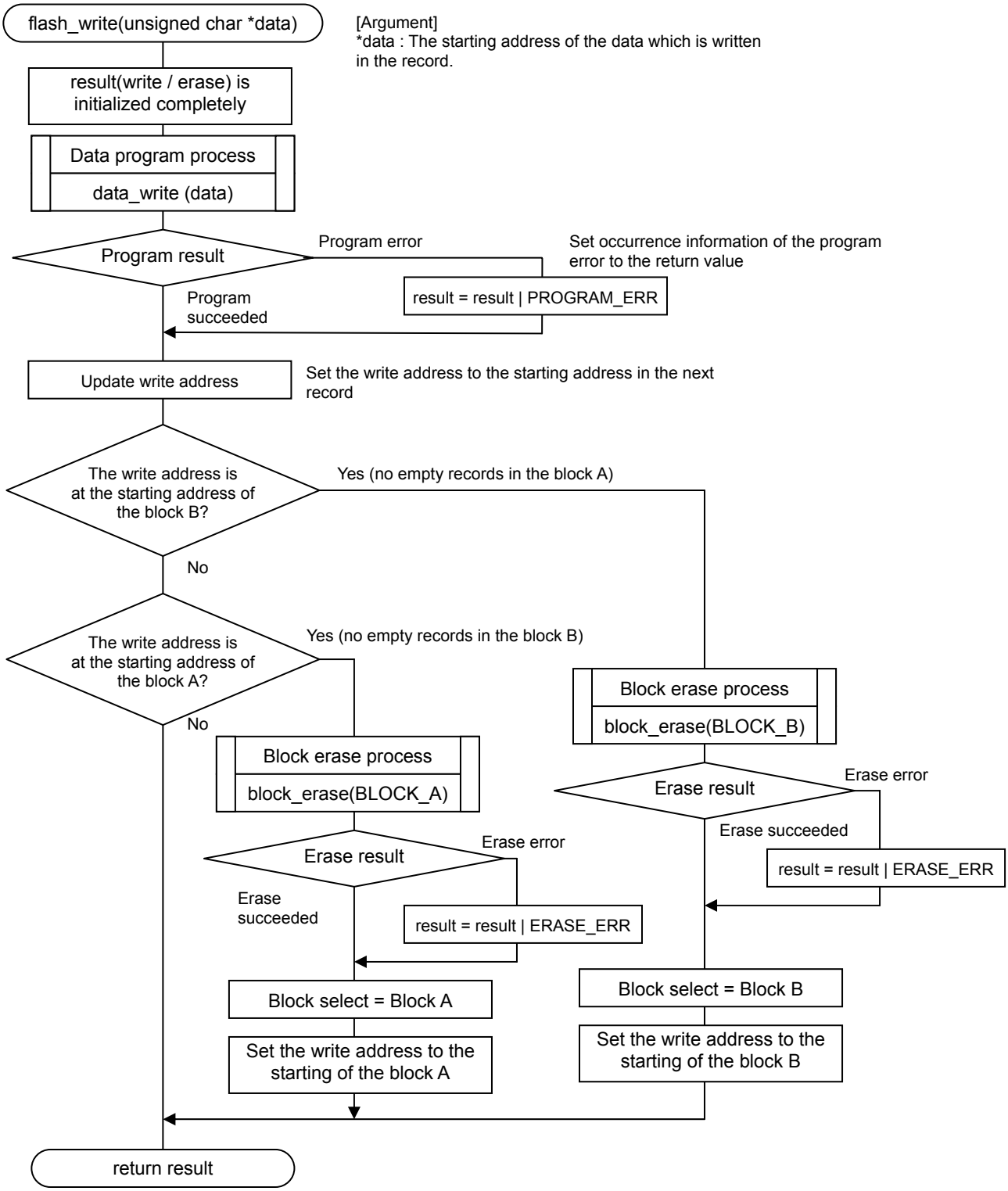

NOTES:

In this application note, error processes are not performed. Process errors if needed.

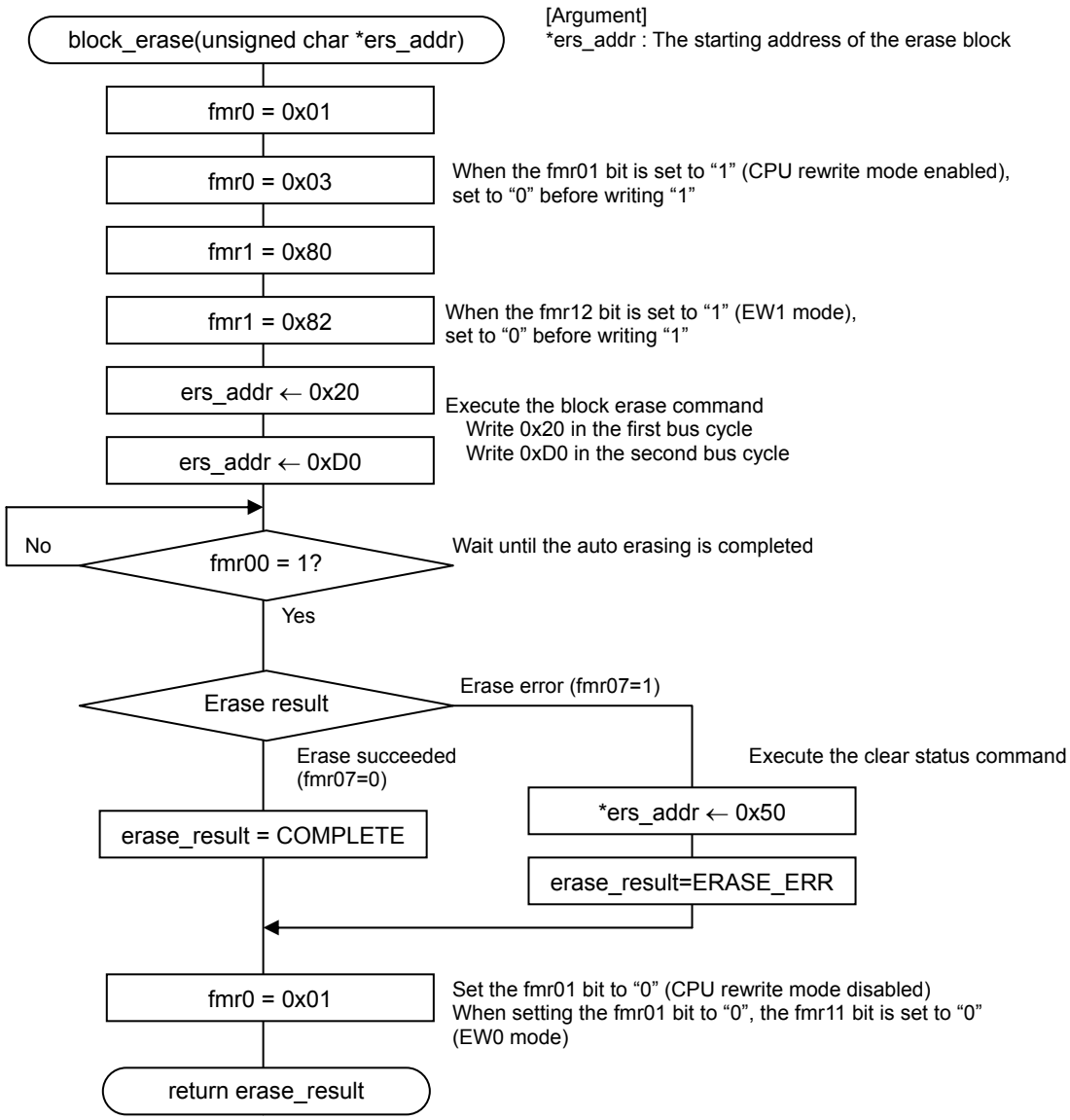
### 4.2.2 Write Address Initial Function



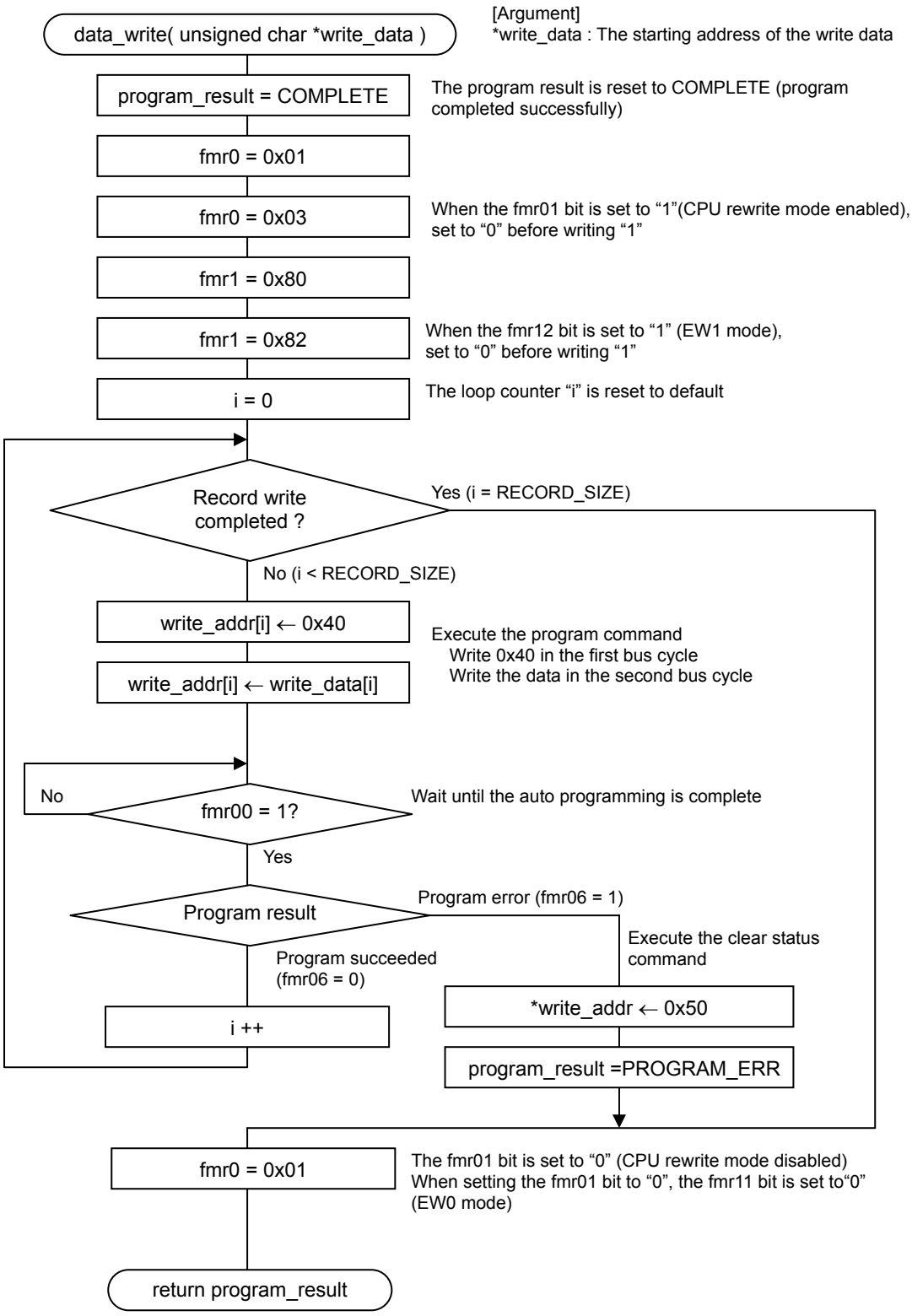
### 4.2.3 Data Write Control Function



### 4.2.4 Block Erase Function



### 4.2.5 Data Program Function



## 5. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu on the top page of the R8C/Tiny Series.

## 6. Reference Documents

Hardware Manual
R8C/13 Group Hardware Manual
(Download the latest version from the Renesas Technology website.)

Technical News/Technical Update
(Download the latest information from the Renesas Technology website.)

## Website and Support

Renesas Website

http://www.renesas.com

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| REVISION HISTORY | R8C/13 Group<br>Flash Rewrite Using EW1 Mode (Data "FFh" Search) |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Mar 22, 2004 | - | First edition issued |
| 1.10 | Aug 23, 2004 | - | Sample Program Comment is revised |
| 1.20 | Apr 01, 2005 | 19 | Sample Programming Code is deleted |
| 2.00 | Jul 24, 2006 | 17,18 | The set value of FMR17 bit (reserved bit) is changed to “1” |

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