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M16C/62P Group

Flash Memory Version CPU Rewrite Mode (EW0 Mode) Sample

1. Abstract

This application note presents an example method for using CPU rewrite mode (EW0 mode) in the flash memory version of microcomputers.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/62P Group

This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/62P microcomputers. However, some functions may have been modified.
Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Explanation of Example Usage

Features of EW0 mode:
In EW0 mode, the CPU rewrite program is transferred into the RAM, and by issuing programming and erasing commands from the CPU rewrite program in the RAM, the user ROM and the data areas can be rewritten. Since while in EW0 mode the CPU continues operating even during a programming or erasing operation, peripheral function interrupts can be accepted during a programming or erasing operation providing that the vectors for those interrupts and the interrupt service routines are located in the RAM.

3.1 CPU Rewrite Mode (EW0 Mode) Execution Flow

Figure 1 shows CPU Rewrite Mode (EW0 Mode) Execution Flow.

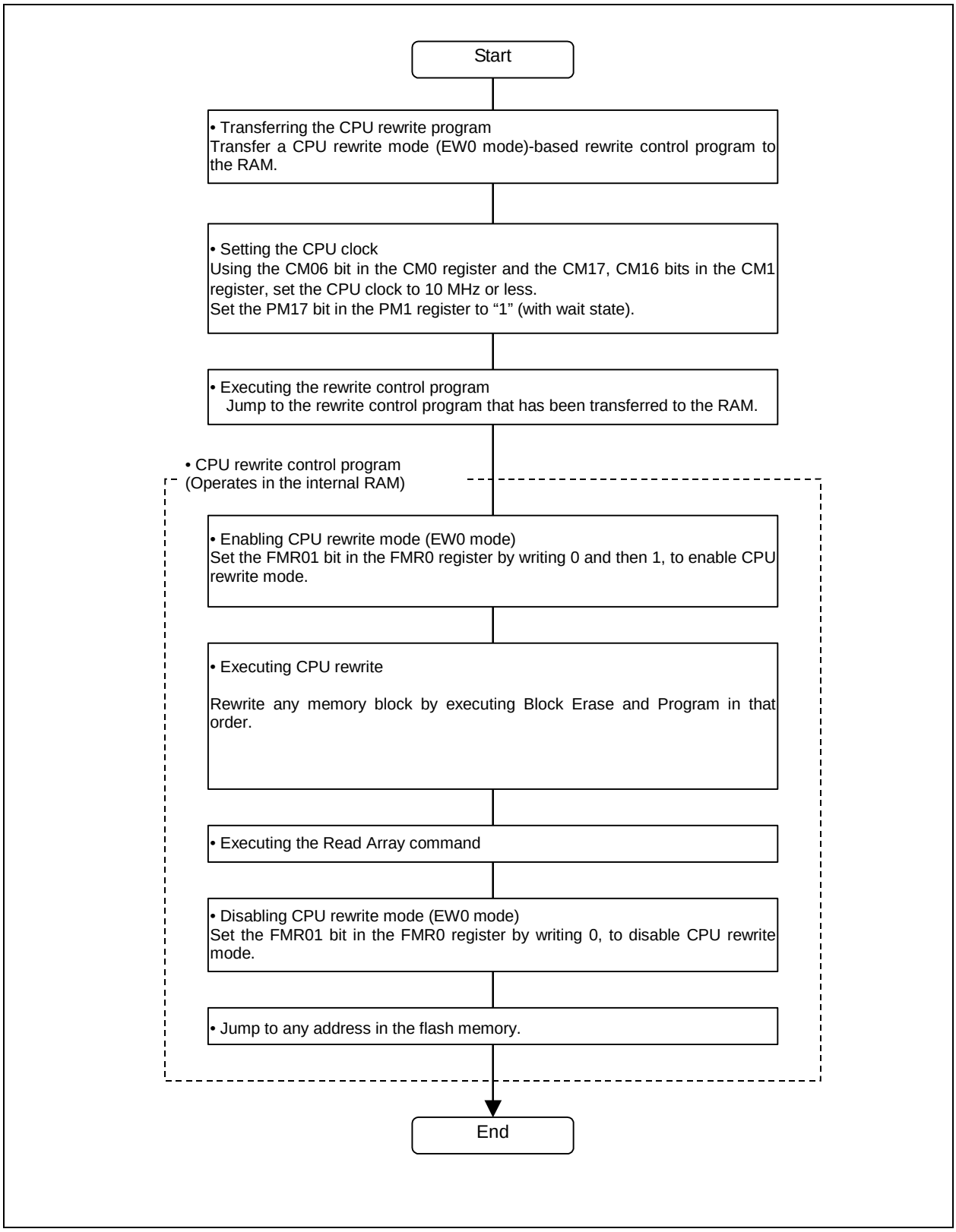
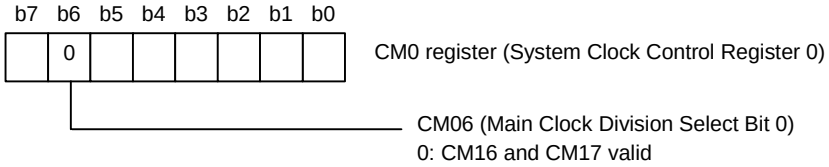


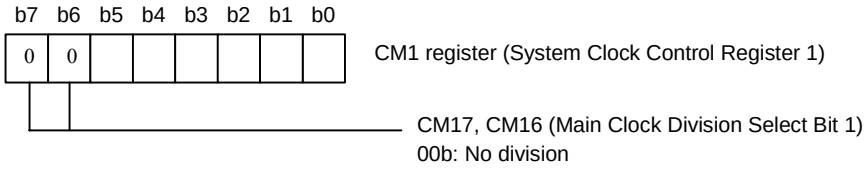
Figure 1 CPU Rewrite Mode (EW0 Mode) Execution Flow

3.2 Set Up Procedure

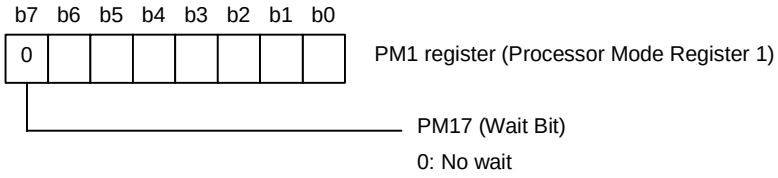
3.2.1 Setting CPU Clock

(1) Setting the main clock divide-by-N value





(2) Setting wait states



3.2.2 Transferring the CPU Rewrite Control Program into RAM

The CPU rewrite control program needs to be run in RAM. Here, the following explains an example for transferring the CPU rewrite control program from the ROM area in which it is stored beginning with the address 0FA000h to an area in RAM.

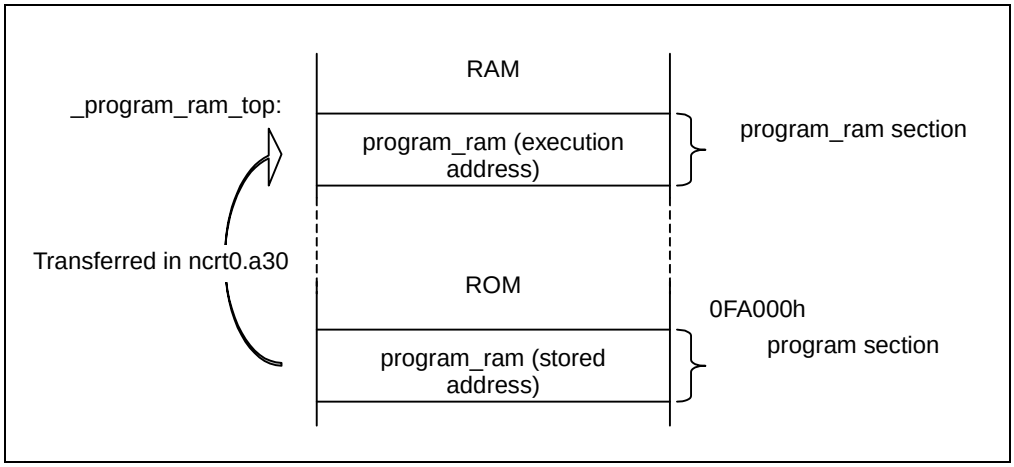


Figure 2 Program Location

(1) Change the Section Name.

Add a section name “program_ram,” and locate the program to be run in RAM in that section. To relocate the program from the program section to the program_ram section, write a process as shown below.

```
void main(void)
{
    /* This program part is located in the program section */
}
```

```
/* The program part following the #pragma SECTION declaration is located in the program_ram section */
#pragma SECTION program program_ram
void low_power(void)
{
    /* This program part is located in the program_ram section */
}
```

(2) Changing sect30.inc

Add the program_ram section to sect30.inc. In the example here, it is located after the heap section. Note also that the program_ram_top label is used when transferring the program.

```
;------------------------------------------------------------
;       heap section
;------------------------------------------------------------
        .section   heap,DATA
heap_top:
        .blkb      HEAPSIZE
```

```
;------------------------------------------------------------
; RAM program area
;------------------------------------------------------------
        .section   program_ram,ALIGN
_program_ram_top:
        .glb       _program_ram_top
```

Add here.

(3) Transferring the Program

Add a process for transferring the program into RAM in the startup routine (ncrt0.a30).

```
;======================================================================
; Initialize standard I/O
;----------------------------------------------------------------------
.if __STANDARD_IO__ != 1
        .glb       _init
        .call      _init,G
        jsr.a      _init
.endif
```

```
;======================================================
; Program Ram initialize
;   _from_addr is defined by as30 option "-D_from_addr=0fa000h"
;------------------------------------------------------------
      N_BCOPY _from_addr,_program_ram_top,program_ram
;
```

Add here

```
;=====================================================
; Call main() function
;---------------------------------------------------------------------
        ldc     #0h,fb    ; for debuger

        .glb    _main
        jsr.a   _main
```

(4) Specifying the Program Storage Location

To run the program transferred into RAM, it is necessary to specify in the linker (ln30) that the program storage address (in ROM) and execution address (in RAM) be located separately.

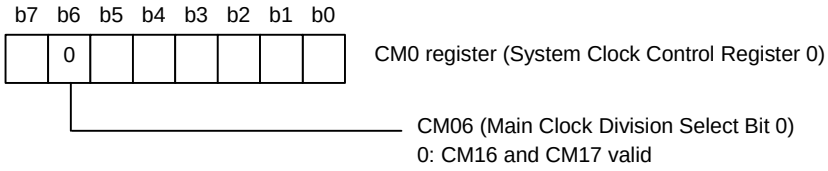
```
ln30 –LOC program_ram=0FA000
```

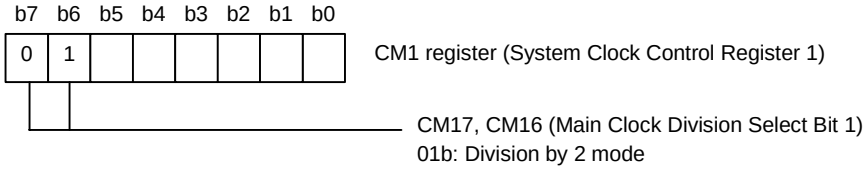
In the above option, the program_ram section is stored beginning with the address 0FA000h.

3.2.3 Processing in the CPU Rewrite Control Program

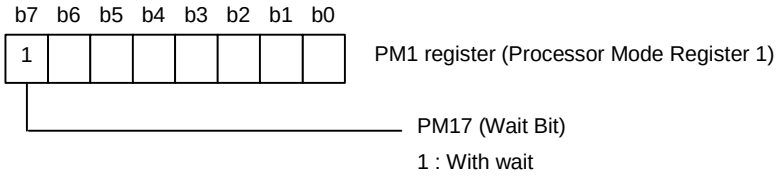
(1) Set the CPU clock to 10MHz or less.

Setting the main clock divide-by-N value

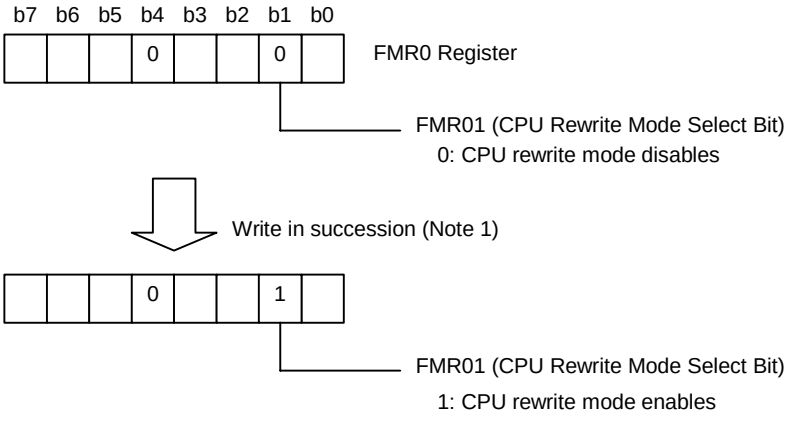




Setting wait states



(2) Enable the CPU rewrite mode.



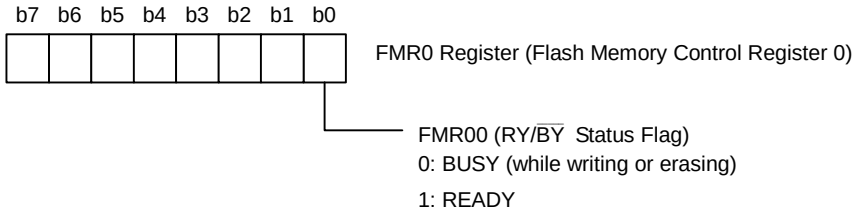
Note: To set the FMR01 bit to “1”, write “0” and then “1” to the FMR01 bit in succession. Make sure no interrupts or DMA transfers occur before the CPU writes “1” after writing “0”.
Make sure writes to the FMR01 bit is performed in other than the internal flash memory.
Also make sure this write operation is performed while the $\overline{\text{NMI}}$ pin is in the high state.
Set this bit to “0” after read array command.

(3) Block erase processing

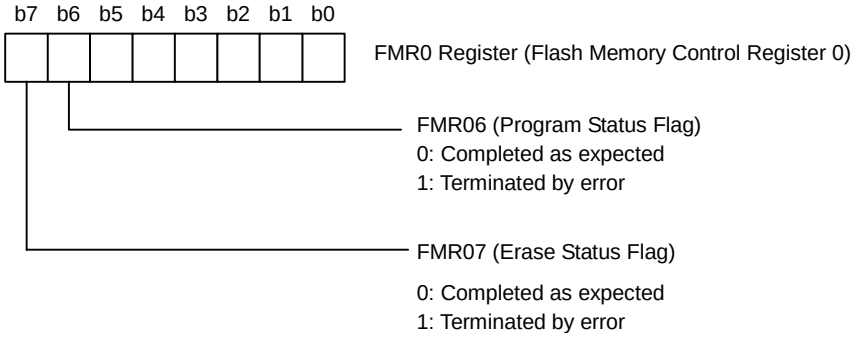
- Executing the Block Erase command
  Write “0020h” and then “00d0h” in succession to the most significant address (Note 1) of the memory block to be block-erased.

  Note 1: If block 5 is block-erased, write to the address F7FFEh.

- Waiting for Block Erase to complete
  Wait until the FMR00 bit in the FMR0 register is set to “1” (ready).



- Status check
  Check the FMR06 and FMR07 bits in the FMR0 register to see if an erase error has occurred. If an error is found to have occurred during the erase operation, write “0050h” (Clear Status command) to the address to which the Block Erase command was written, to stop CPU rewrite processing.



(4) Programming process
Program the entire area of the relevant memory block one word at a time, by following the procedure described below.

- Executing the Program command
  Write “0040h” (Program command) and then the program data to the address to be programmed.

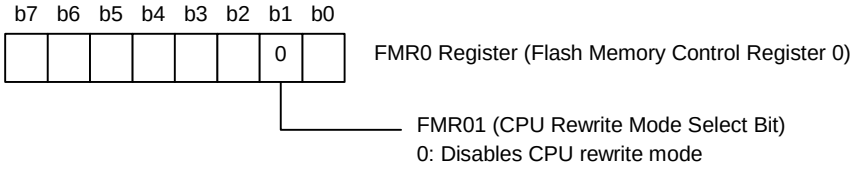
- Waiting for Program to complete
  Wait until the FMR00 bit in the FMR0 register is set to “1” (ready).

- Status check
  Check the FMR06 and FMR07 bits in the FMR0 register to see if a programming error has occurred. If an error is found to have occurred during the programming operation, write “0050h” (Clear Status command) to the address to which the Program command was written, to stop CPU rewrite processing.

(5) Disable CPU rewrite mode.

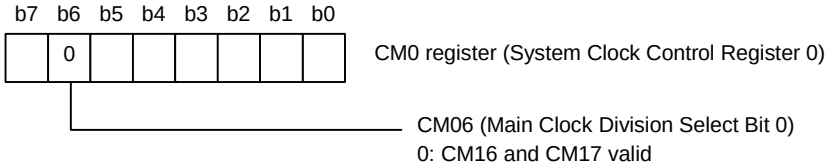
- Executing the Read Array command
  Write “00FFh” (Read Array command) to the most significant address of the relevant memory block.

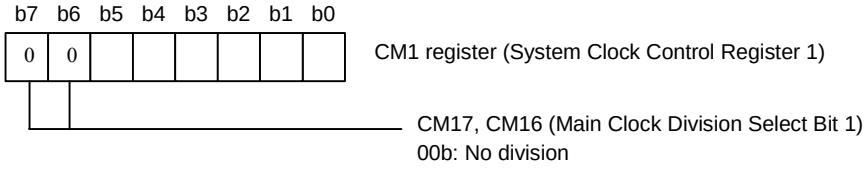
- Disable CPU rewrite mode



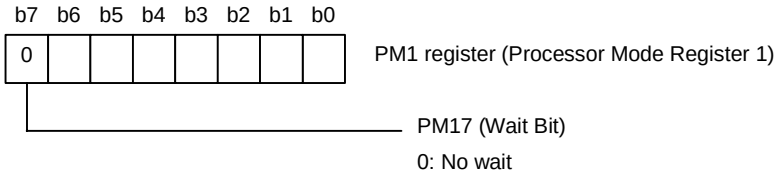
(6) Restore the CPU clock to the original one.

- Setting the main clock divide-by-N value





- Setting wait states



(7) Return to the program in the flash memory.

3.3 Precautions in CPU Rewrite Mode (EW0 Mode)

The following describes the precautions to be observed when using CPU rewrite mode (EW0 mode). (Please consult the manual to get the latest information.)

(1) Operating Speed

Before entering CPU rewrite mode (EW0 or EW1 mode), set the CM11 bit in the CM1 register to "0" (main clock), select 10 MHz or less for CPU clock using the CM06 bit in the CM0 register and CM17 to CM16 bits in the CM1 register. Also, set the PM17 bit in the PM1 register to "1" (with wait state).

(2) Instructions inhibited against use

The following instructions cannot be used in EW0 mode because the flash memory's internal data is referenced: UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

(3) Interrupts (EW0 Mode)

- Any interrupt which has a vector in the relocatable vector table can be used providing that its vector is transferred into the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts can be used because the FMR0 register and FMR1 register are initialized when one of those interrupts occurs. The jump addresses for those interrupt service routines should be set in the fixed vector table.
  Because the rewrite operation is halted when a $\overline{\text{NMI}}$ or watchdog timer interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.
- The address match interrupt cannot be used because the flash memory's internal data is referenced.

(4) Interrupts (EW1 Mode)

- Make sure that any interrupt which has a vector in the variable vector table or address match interrupt will not be accepted during the auto program or auto erase period.
- Avoid using watchdog timer interrupts.
- The $\overline{\text{NMI}}$ interrupt can be used because the FMR0 register and FMR1 register are initialized when this interrupt occurs. The jump address for the interrupt service routine should be set in the fixed vector table.
  Because the rewrite operation is halted when a $\overline{\text{NMI}}$ interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.

(5) How to Access

To set the FMR01, FMR02, or FMR11 bit to “1”, write “0” and then “1” in succession. This is necessary to ensure that no interrupts or DMA transfers will occur before writing "1" after writing “0”. Also only when $\overline{\text{NMI}}$ pin is “H” level.

(6) Writing in the User ROM Area (EW0 Mode)

If the power supply voltage drops while rewriting any block in which the rewrite control program is stored, a problem may occur that the rewrite control program is not correctly rewritten and, consequently, the flash memory becomes unable to be rewritten thereafter. In this case, standard serial I/O or parallel I/O mode should be used.

(7) Writing in the User ROM Area (EW1 Mode)

Avoid rewriting any block in which the rewrite control program is stored.

(8) DMA Transfer

In EW1 mode, make sure that no DMA transfers will occur while the FMR00 bit in the FMR0 register = 0 (during the auto program or auto erase period).

(9) Writing Command and Data

Write the command code and data at even addresses.

(10) Wait Mode

When shifting to wait mode, set the FMR01 bit to “0” (CPU rewrite mode disabled) before executing the WAIT instruction.

(11) Stop Mode

When the microcomputer enters stop mode, execute the instruction which sets the CM10 bit to "1" (stop mode) after setting the FMR01 bit to "0" (CPU rewrite mode disabled) and disabling the DMA transfer.

(12) Low power dissipation mode, on-chip oscillator low power dissipation mode

If the CM05 bit is set to “1” (main clock stop), the following commands must not be executed.

- Program
- Block erase
- Erase all unlocked blocks
- Lock bit program

4. Sample Programming Code

The following shows an example program for using CPU rewrite mode (EW0 mode) to back up the internal RAM (addresses 1800h–2BFFh) to the block 5 (addresses F0000h–F7FFFh) as triggered by an $\overline{\text{INT0}}$ interrupt request generated. In this example program, block 5 is block-erased and then programmed (to save the RAM area).

Memory map:

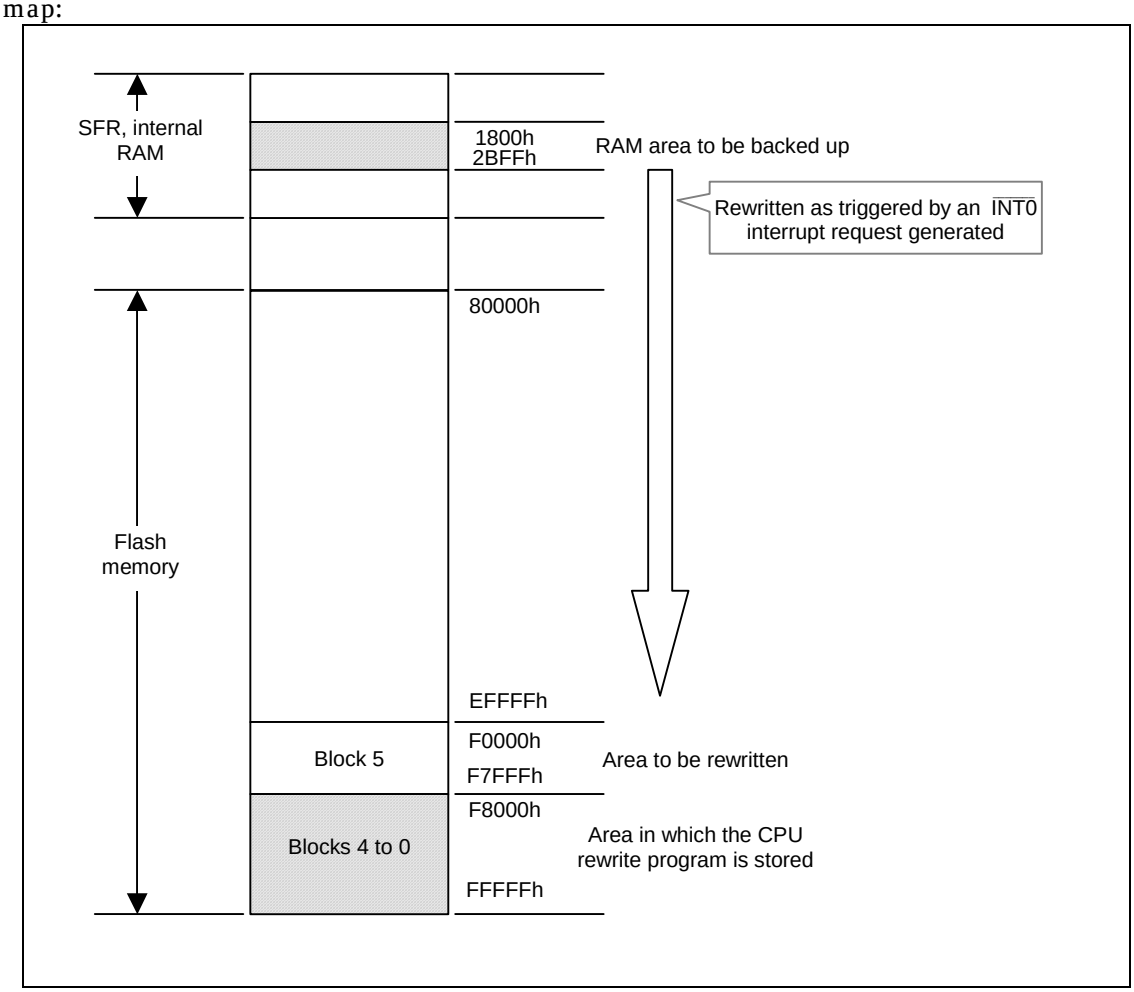


Figure 3 Memory Map

Operating Conditions:
(1) VCC1=VCC2=5V
(2) XIN=16MHz
(During CPU rewrite mode, the device must be operated with 4 MHz by setting the CM06 bit in the CM0 register and the CM16, CM17 bits in the CM1 register, and PM17 bit in the PM1 register.)

Amount of memory used:
The CPU rewrite program transferred into RAM requires 312 bytes of memory when it is compiled without optimization options.

4.1 Processing Flow

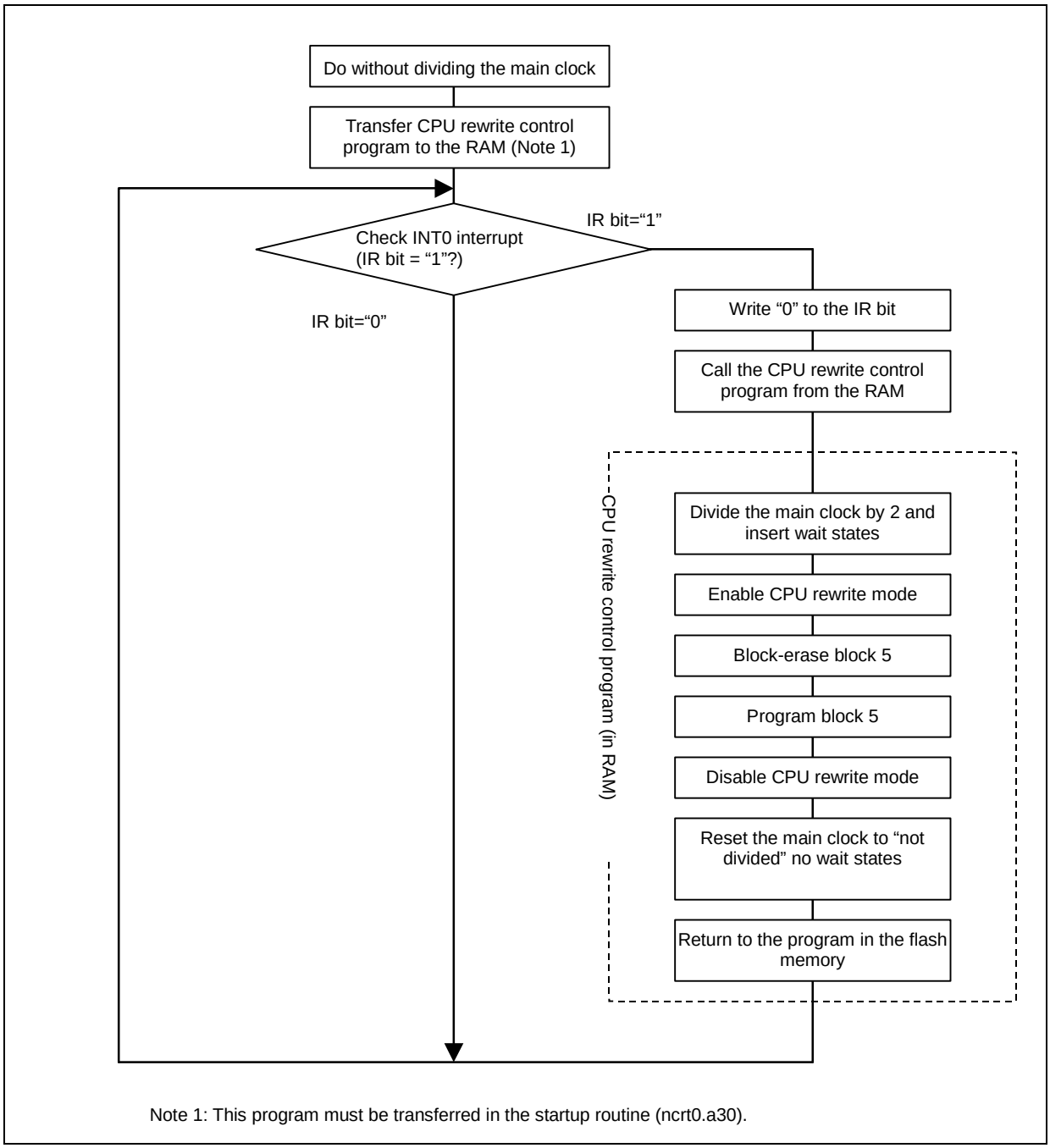


Figure 4 Sample Program Processing Flow

5. Reference

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