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H8SX Family

Flash Memory Reprogramming in the User Boot Mode for H8SX/1657F

Introduction

This application note describes the reprogramming of flash memory (the user MAT) via a clock synchronous communications interface in the use boot mode of H8SX/1657F, and mainly concerns the slave side. That is, unless otherwise specified, the descriptions are related to the slave side.

Target Device

H8SX/1657F

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1. Specification

1.1 Outline

Specifications, which are highly reliable for users to reprogram the on-chip flash memory, are provided for H8SX/1657F. The use starts by downloading the erasing or programming module to the RAM and then calls subroutines to erase/program the flash memory.

In this sample task, data for reprogramming are placed in the flash memory on the master side and sent to the slave side by clock synchronous communications. The following procedure is then applied to reprogram the flash memory on the slave side. A sample configuration for on-board reprogramming is illustrated in figure 1, and the connections for clock synchronous communications between the master and slave are illustrated in figure 2.

- Power-on resets are applied, and the slave boots up in the user boot mode and the master boots up in the user mode.
- When master side switch 0 (SW0) is turned on, the master side sends the erase command to the slave side, and the slave side erases its own flash memory.
- The master side sends the data to be reprogrammed from its own flash memory to the slave side. The data for reprogramming are transferred in clock synchronous mode via serial communications interface (SCI) 0. The data is transmitted from the master side and received on the slave side.
- The slave programs the received data for reprogramming to its own flash memory.
- On both the master and slave sides, PD7 is low and PD6 is high while the flash memory is being reprogrammed, and PD7 is high and PD6 is low on completion of reprogramming.

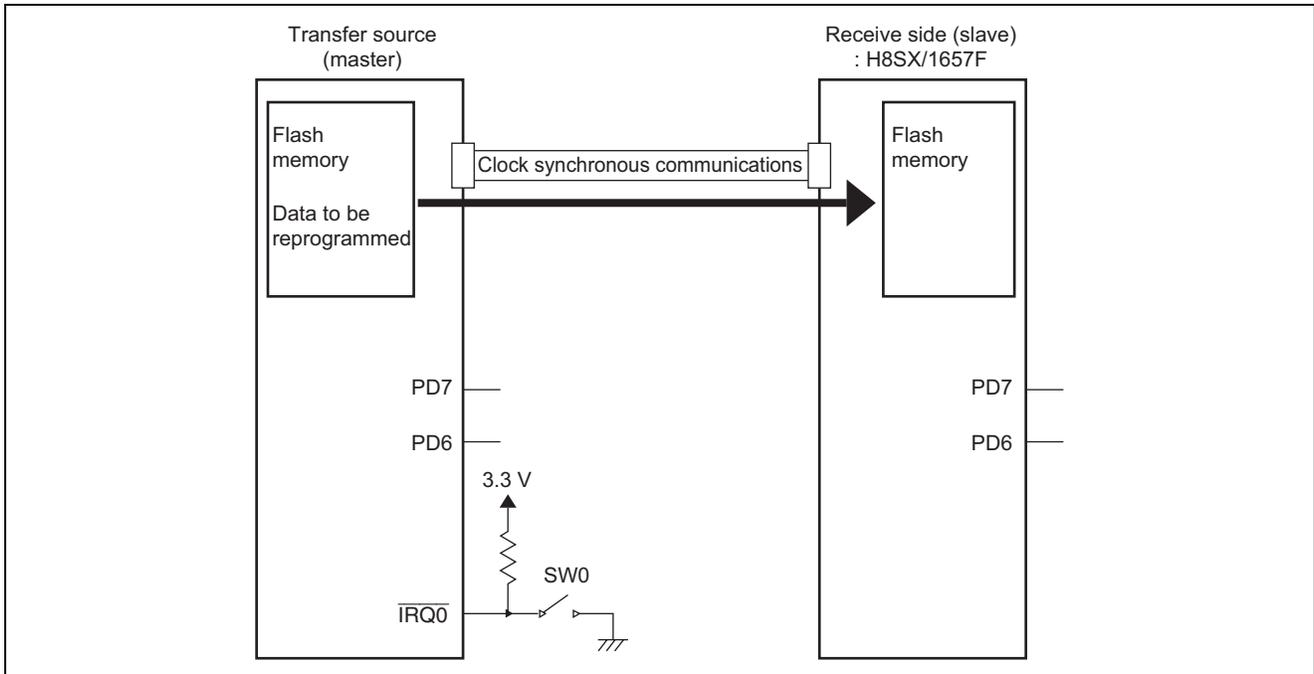


Figure 1 Sample Configuration for On-Board Reprogramming

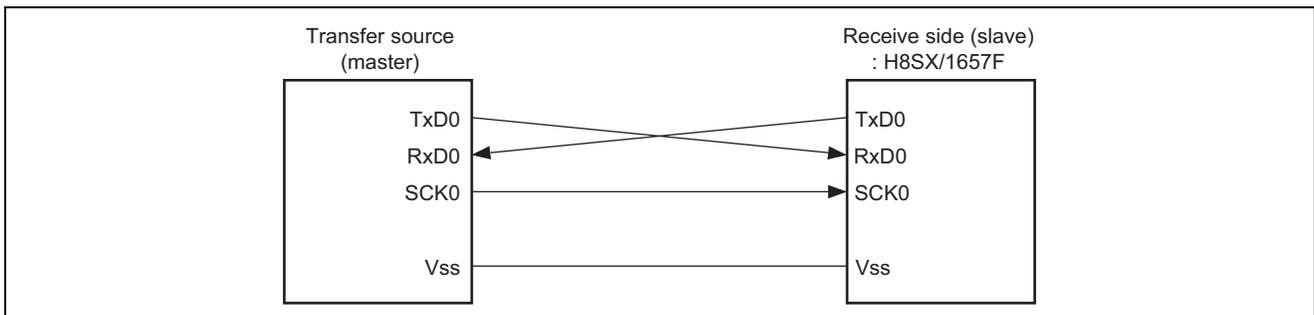


Figure 2 Connections for Clock Synchronous Communications between the Master and Slave

1.2 User Boot Mode

Set the mode pin for the user boot mode (MD1 = 0, MD0 = 1), and performs a start from reset.

The RAM transfer program, clock synchronous communications program, and programming/erasing procedure program must be written to the user MAT in advance.

1.3 Specification for Communications

The specification for communications between the master and slave in this sample task are listed below.

1.3.1 Type of Communications

Table 1 Type of Communications

Item	Setting
Transfer rate	2.5 Mbps
Type	Clock synchronous communications
Data bit	8 bits (1 byte)

1.3.2 Communications Command

Table 2 Communications commands

Command Name	Constant Name	Command Data
Erase	ERASE	H'11
Write	WRITE	H'12
Read status	STATUSREAD	H'13
128-byte transmission request	TRS128	H'14

1.3.3 State Indicator

Table 3 State Indicator

Statue Name	Constant Name	Status Data
Normal	OK	H'00
Erase command error	ER_ECMD	H'C1
Erase download error	ER_EDWNLD	H'C2
Erase initialization error	ER_EINIT	H'C3
Erase error	ER_ERASE	H'C4
Program command error	ER_WCMD	H'A1
Program download error	ER_WDWNLD	H'A2
Program initialization error	ER_WINIT	H'A3
Program error	ER_WRITE	H'A4

1.3.4 Specifying Blocks to be Erased

The erase command “ERASE” is sent from the master to the slave and is immediately followed by an indicator of the block numbers of blocks to be erased. The communications format for block erasure is given in table 4. Block settings are made in a 4-byte (32-bit) unit where bits 19 to 0 correspond to blocks 19 to 0. Since bits 31 to 20 are not used, always set them to 0. An example of the data transmitted to erase block 19 is given in table 5.

Table 4 Correspondence of Blocks to be Erased

Bit	Erased Block	Setting	Description
31 to 20	No used	0 fixed	Not used. Set 0.
19 to 0	EB19 to EB0	0/1	0: The corresponding block is not erased. 1: The corresponding block is erased.

Table 5 Example of Data for Transmission to Erase Block 19

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte
Item	Erase Command (ERASE)	Erase block			
Byte	H'11	H'00	H'08	H'00	H'00
Bit	0 0 0 1 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	MSB	LSB MSB	LSB MSB	LSB MSB	LSB MSB

Note: The data is transmitted in byte units, with the LSB first.

1.4 Memory Map

The memory map for this sample task is given as figure 3.

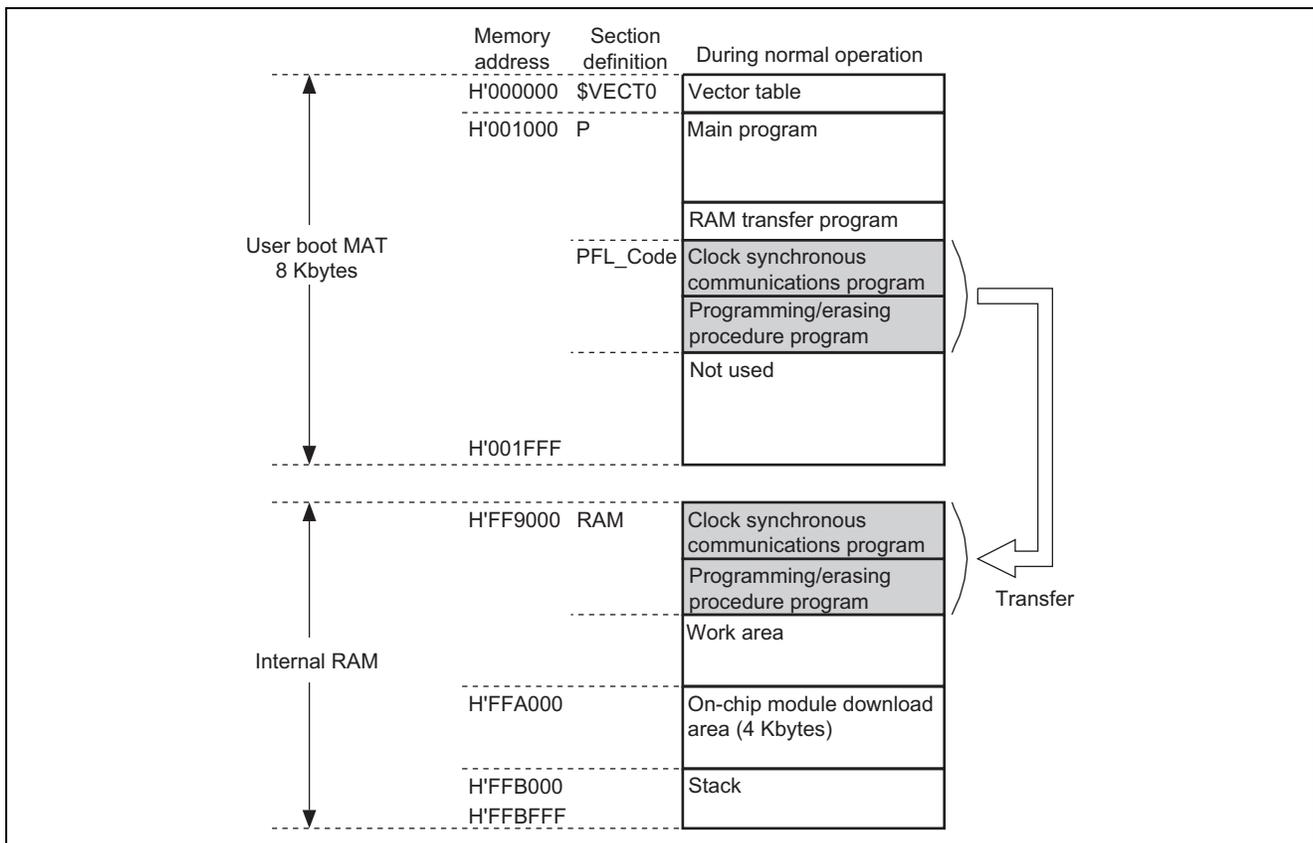


Figure 3 Memory Map

2. Applicable Conditions

Table 6 Applicable Conditions

Item	Description
Operating Frequency	Input clock: 17.5 MHz System clock (I ϕ): 35 MHz Peripheral module clock (P ϕ): 35 MHz External bus clock (B ϕ): 35 MHz
Operating mode	Mode 1 (MD2 = 0, MD1 = 0, MD0 = 1)
On-board programming mode	User boot mode
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 7 Section Setting

Address	Section Name	Description
H'001000	P	Program area
	PFL_Code	Areas for storing programming/erasing procedure program
H'FF9000	RAM	Area for transferring programming/erasing procedure program

3. Description of Functions Used

3.1 User Boot Mode

3.1.1 User MAT and User Boot MAT

The on-chip flash memory consists of the two memory units (memory MATs) listed in table 8. Both are allocated to the same address. The user boot mode is an arbitrary boot program that suits the user system, and the user MAT can be programmed/erased.

When the CPU's operating mode setting is for the user boot mode and it is started from a reset, processing starts from the execution start address contained in the reset vector. At this time the target memory MAT is the user boot MAT (FMATS = H'AA). If the user MAT is actually to be erased/programmed, the user boot MAT must be replaced by the user MAT in the memory map when the erasing/programming is to be done. This switching should be executed by code in RAM.

Table 8 Memory MATs

Memory MAT	Activation	Amount of Memory Used
User MAT	Activates when a power-on reset is performed in the user mode.	768 Kbytes
User Boot MAT	Activates when a power-on reset is performed in the user boot mode.	8 Kbytes

3.1.2 Downloading the On-Chip Program

Programming/erasing of the flash memory on this LSI is done by first downloading the on-chip module for either programming/erasing to the on-chip RAM and then running the individual program.

The destination address for downloading is determined by the setting of the download destination specification register (FTDAR). For the RAM address map after downloading, refer to figure 4. As the figure shows, the on-chip RAM area is the destination for downloading of programming/erasing programs. The corresponding program must be downloaded to the RAM area indicated by FTDAR prior to the required processing.

During programming/erasing, take care to ensure that the download area does not overlap with an area in use by the user.

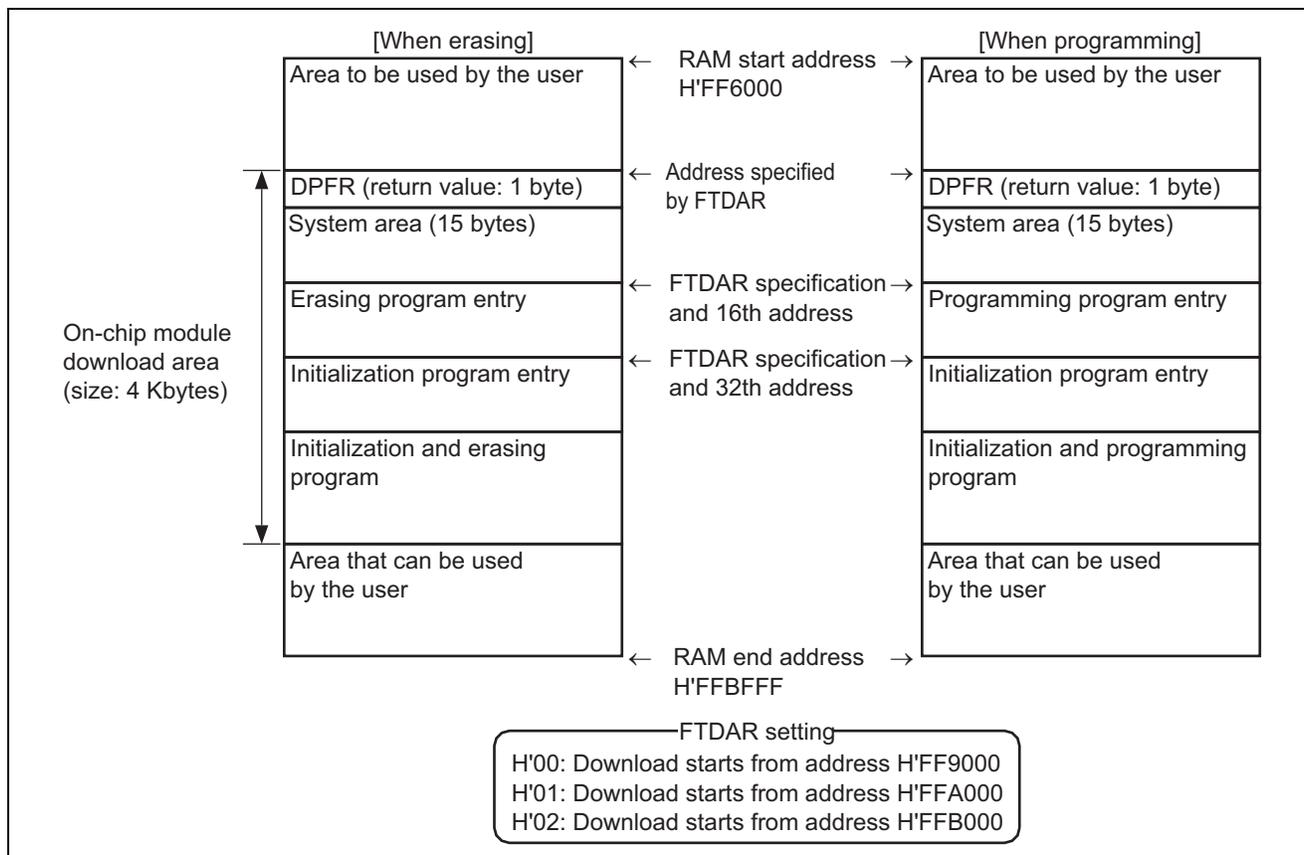


Figure 4 Normal Operation

3.2 Block Configuration

Erase blocks of the user MAT are listed in table 9.

Table 9 User MAT Erase Blocks

Block	Unit of Erasure	Addresses
EB0	4 Kbytes	H'000000 to H'000FFF
EB1	4 Kbytes	H'001000 to H'001FFF
EB2	4 Kbytes	H'002000 to H'002FFF
EB3	4 Kbytes	H'003000 to H'003FFF
EB4	4 Kbytes	H'004000 to H'004FFF
EB5	4 Kbytes	H'005000 to H'005FFF
EB6	4 Kbytes	H'006000 to H'006FFF
EB7	4 Kbytes	H'007000 to H'007FFF
EB8	32 Kbytes	H'008000 to H'00FFFF
EB9	64 Kbytes	H'010000 to H'01FFFF
EB10	64 Kbytes	H'020000 to H'02FFFF
EB11	64 Kbytes	H'030000 to H'03FFFF
EB12	64 Kbytes	H'040000 to H'04FFFF
EB13	64 Kbytes	H'050000 to H'05FFFF
EB14	64 Kbytes	H'060000 to H'06FFFF
EB15	64 Kbytes	H'070000 to H'07FFFF
EB16	64 Kbytes	H'080000 to H'08FFFF
EB17	64 Kbytes	H'090000 to H'09FFFF
EB18	64 Kbytes	H'0A0000 to H'0AFFFF

3.3 Serial Communications Interface

The SCI operates in the clock synchronous mode. It is used for command-related communications between the master and slave to transfer the data for reprogramming.

4. Description of Operation

4.1 User MAT Reprogramming Procedure

User MAT reprogramming procedure in the user boot mode is given in figure 5. In the user boot mode, the user boot MAT is accessible in the flash memory area, but the user MAT is hidden behind it. Therefore, user MAT must be chosen on the occasion of a reprogramming to user MAT. During programming of the user MAT, the user boot MAT is hidden, and the user MAT is being programmed, so the procedure program must be executed from an area other than the flash-memory area. After programming, the memory MATs are switched back to their initial mapping.

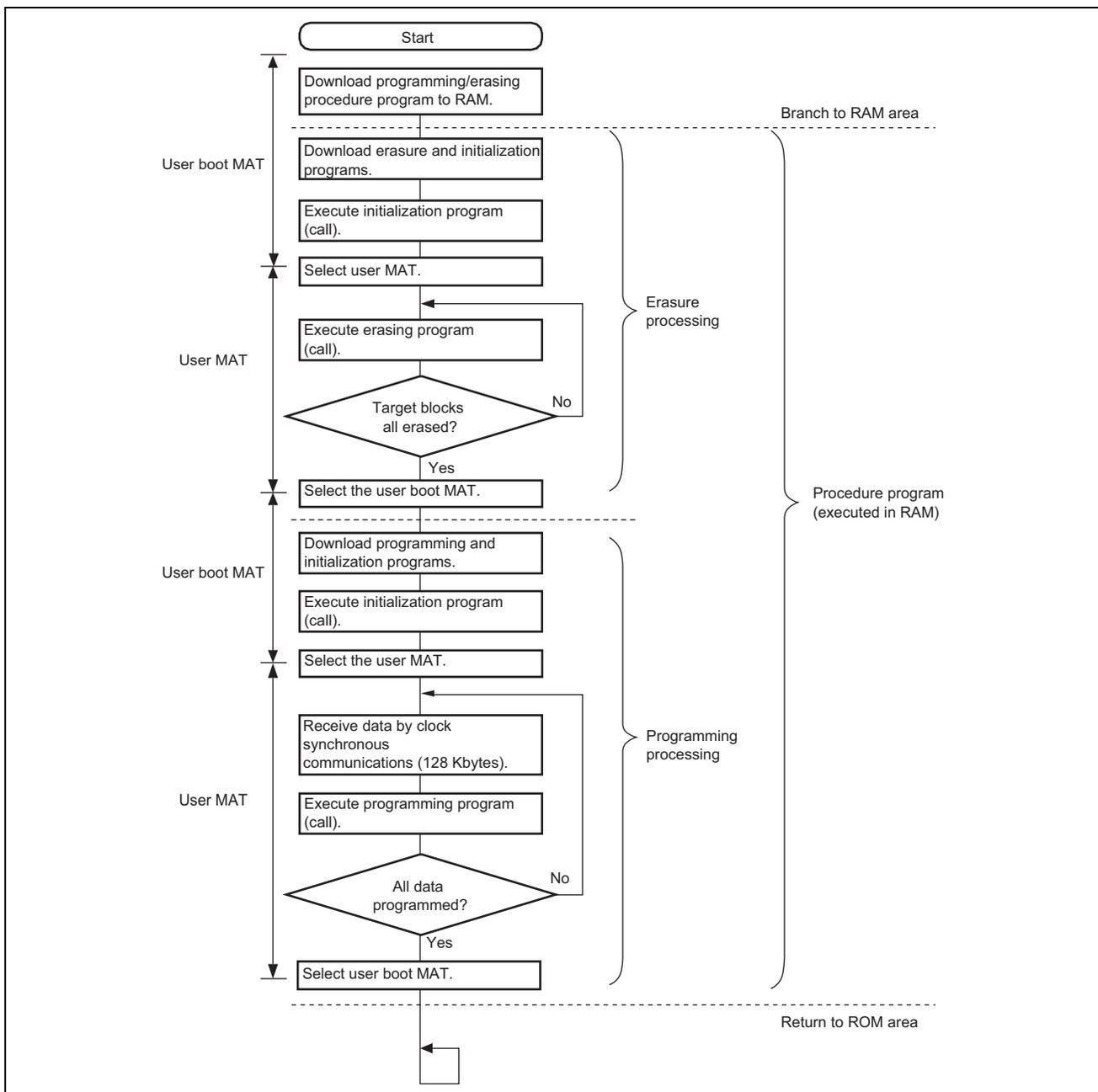


Figure 5 User MAT Reprogramming Procedure

4.2 Operational Overview

4.2.1 Start of On-Board Reprogramming

- (1) A power-on reset is applied to the slave side with the mode pins set for the user boot mode, the RAM transfer program in the user boot mode MAT on the slave side is activated, and the programming/erasing procedure program is transferred to the on-chip RAM.
- (2) Here, PD7 is low and PD6 is high on the slave side.

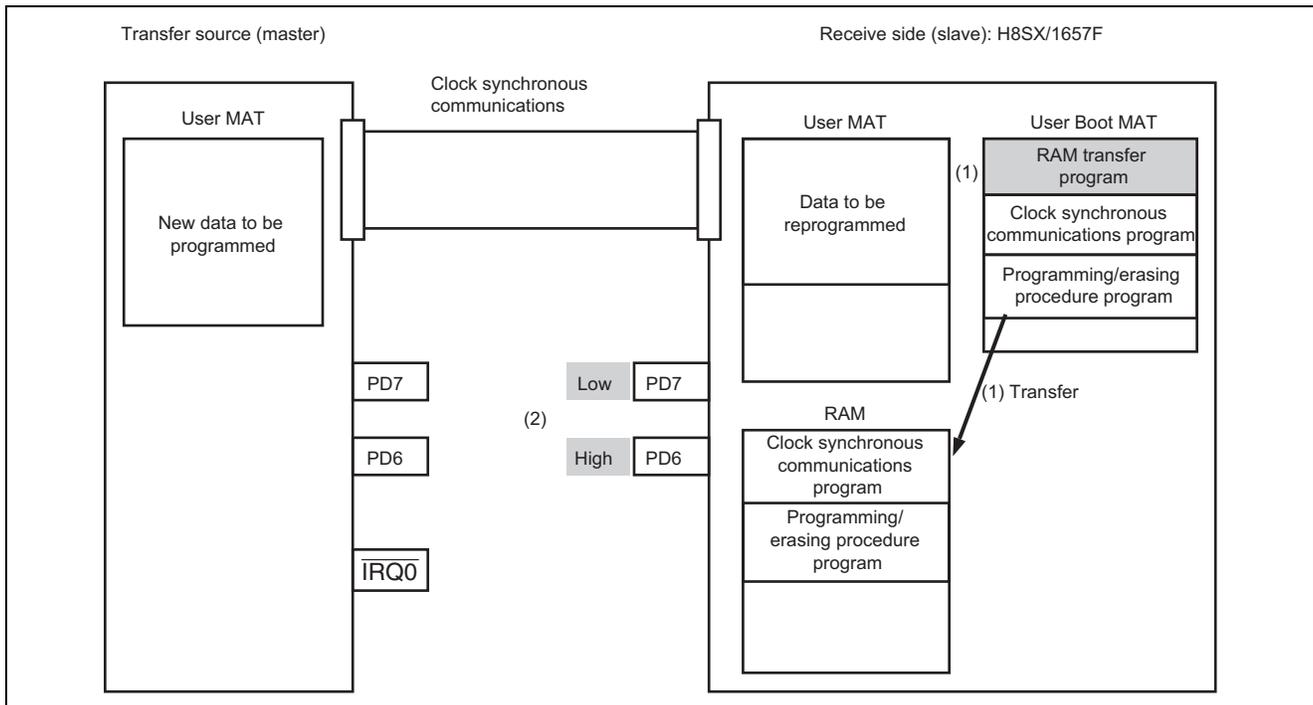


Figure 6 Start of On-Board Reprogramming

4.2.2 Activating the Programming/Erasing Procedure Program

- (1) After the transfer programs have been loaded to RAM, control branches to the programming/erasing procedure program in RAM.

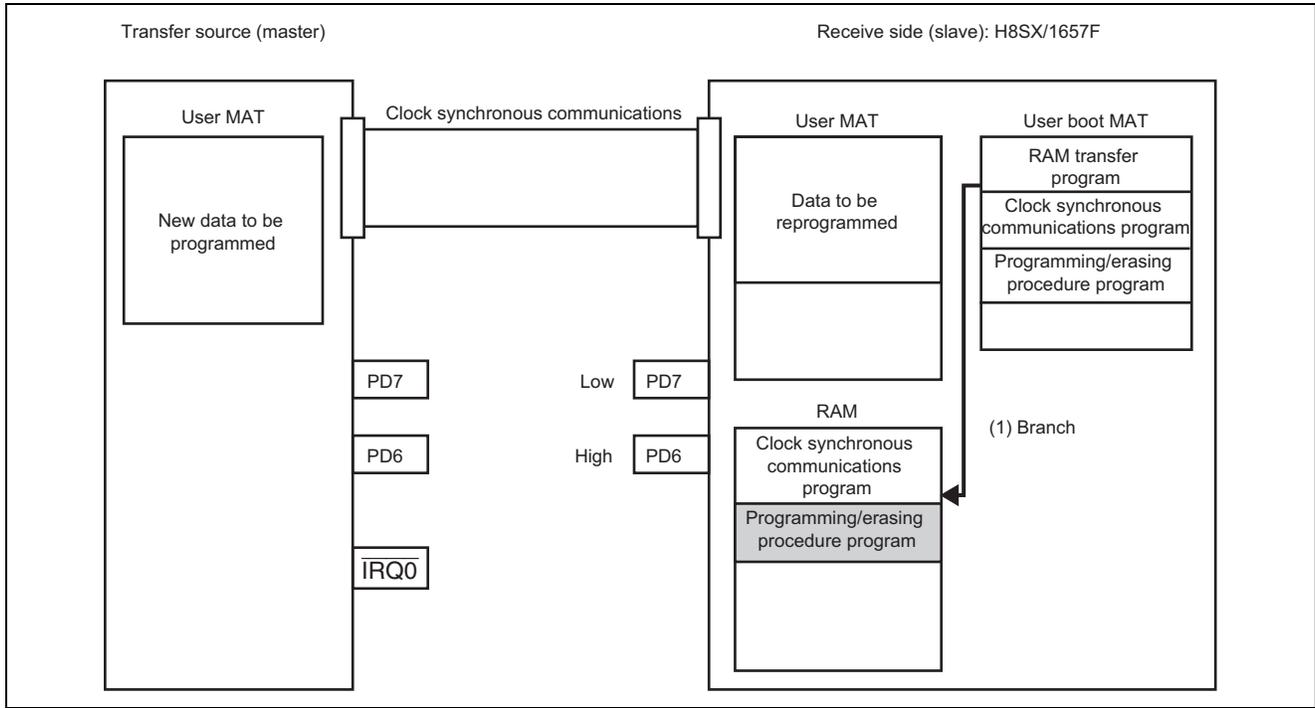


Figure 7 Activation of Programming/Erasing Procedure Program

4.2.3 Erasing User MAT

- (1) When a low level input on the $\overline{\text{IRQ0}}$ pin as a trigger, the master sends the erasing command, "ERASE".
- (2) At this time, PD7 is low and PD6 is high on the master side.
- (3) Registers for controlling the flash memory are set (both the EPVB bit of the FECS register and the SCO bit of the FCCS register to 1), and the initialization program and erasure program are downloaded.
- (4) The initialization program is executed.
- (5) The erasing program is executed, and the target block for erasure on the user MAT is erased.

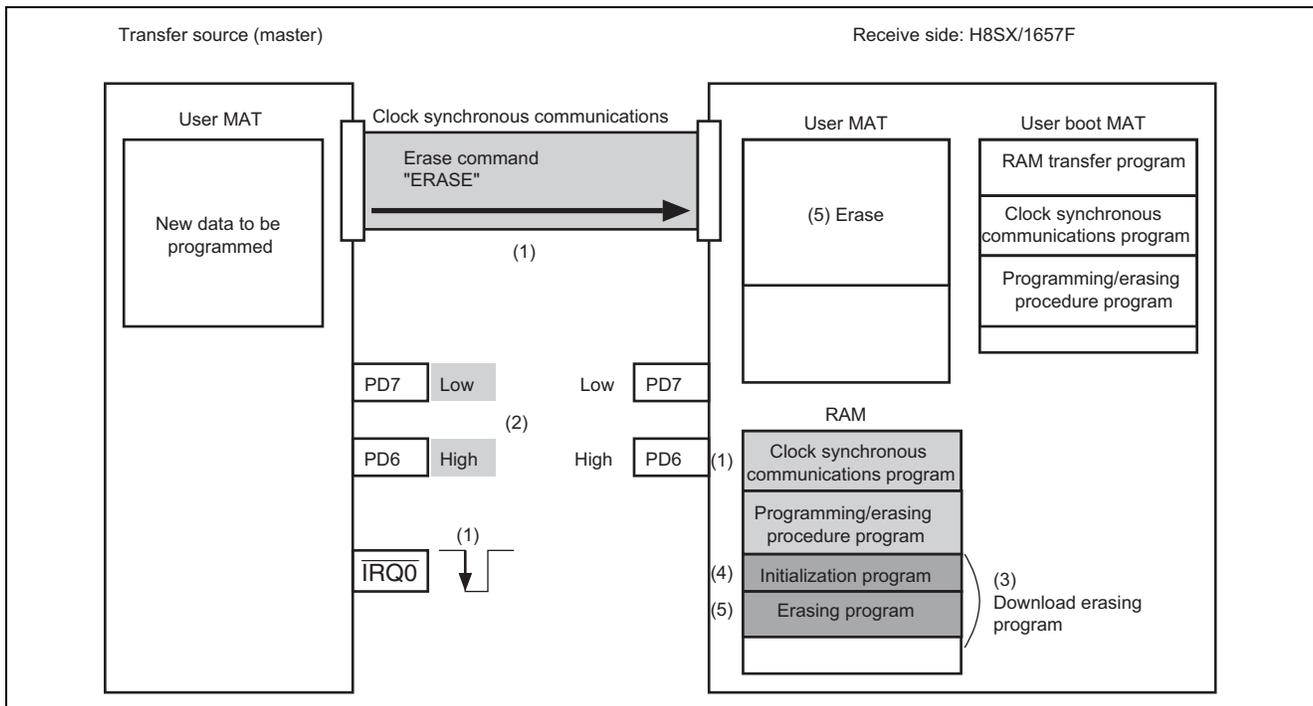


Figure 8 Erasing User MAT

4.2.4 Programming User MAT

- (1) The master sends the programming command "WRITE".
- (2) Registers for controlling the flash memory are set (Both the PPVS bit of the FPCS register and the SCO bit of the FCCS register to 1), and initialization program and the programming program are downloaded.
- (3) The initialization program is executed.
- (4) The following a. and b. are repeated until all data on the master side is programmed on the slave side.
 - a. The receive side (slave) receives 128 bytes of new data from the transfer source (master).
 - b. The receive side (slave) executes the programming program, and writes 128 bytes of data to the user MAT.
- (5) On completion of programming, PD7 is high and PD6 is low on both the master and slave sides.

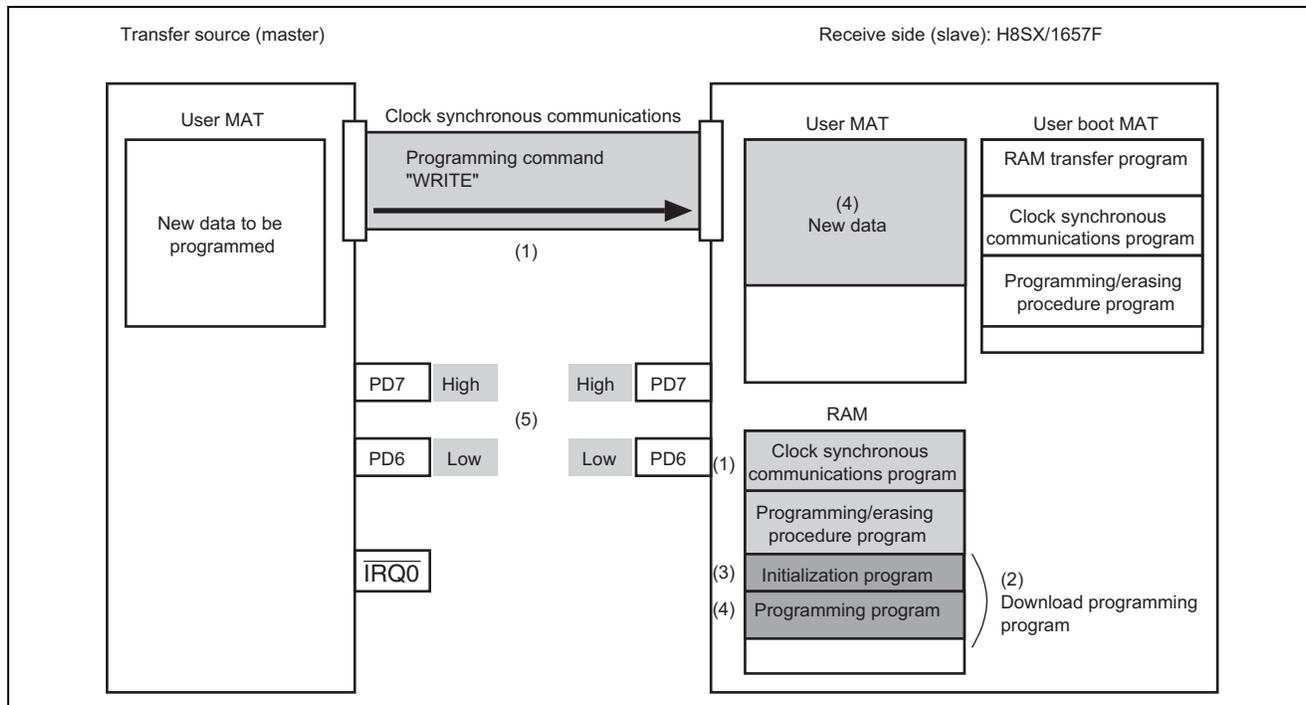


Figure 9 Programming User MAT

4.3 Sequence Diagram

4.3.1 Erasure Processing

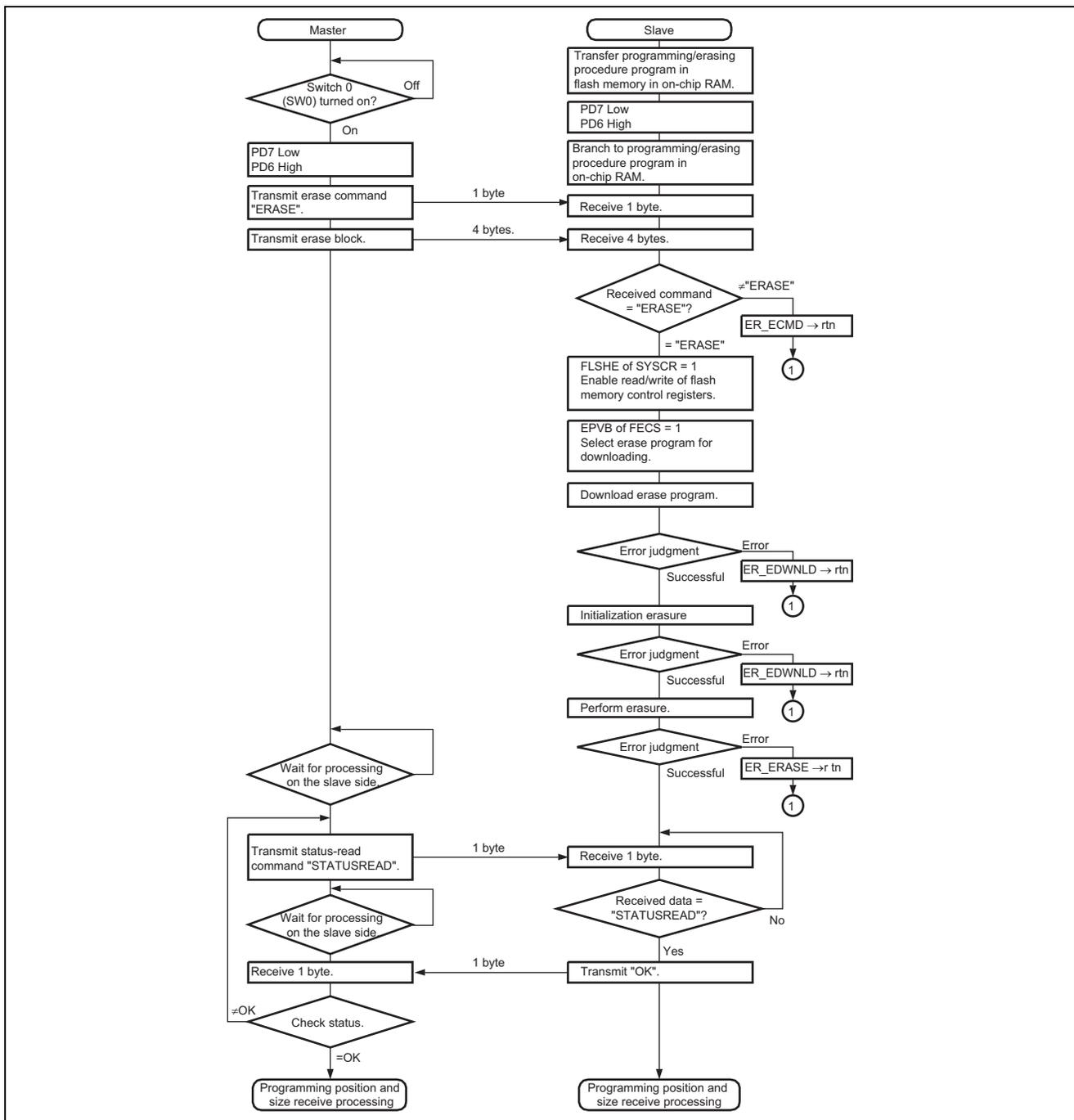


Figure 10 Erasure Processing

4.3.2 Processing to Receive the Position and Range for Programming

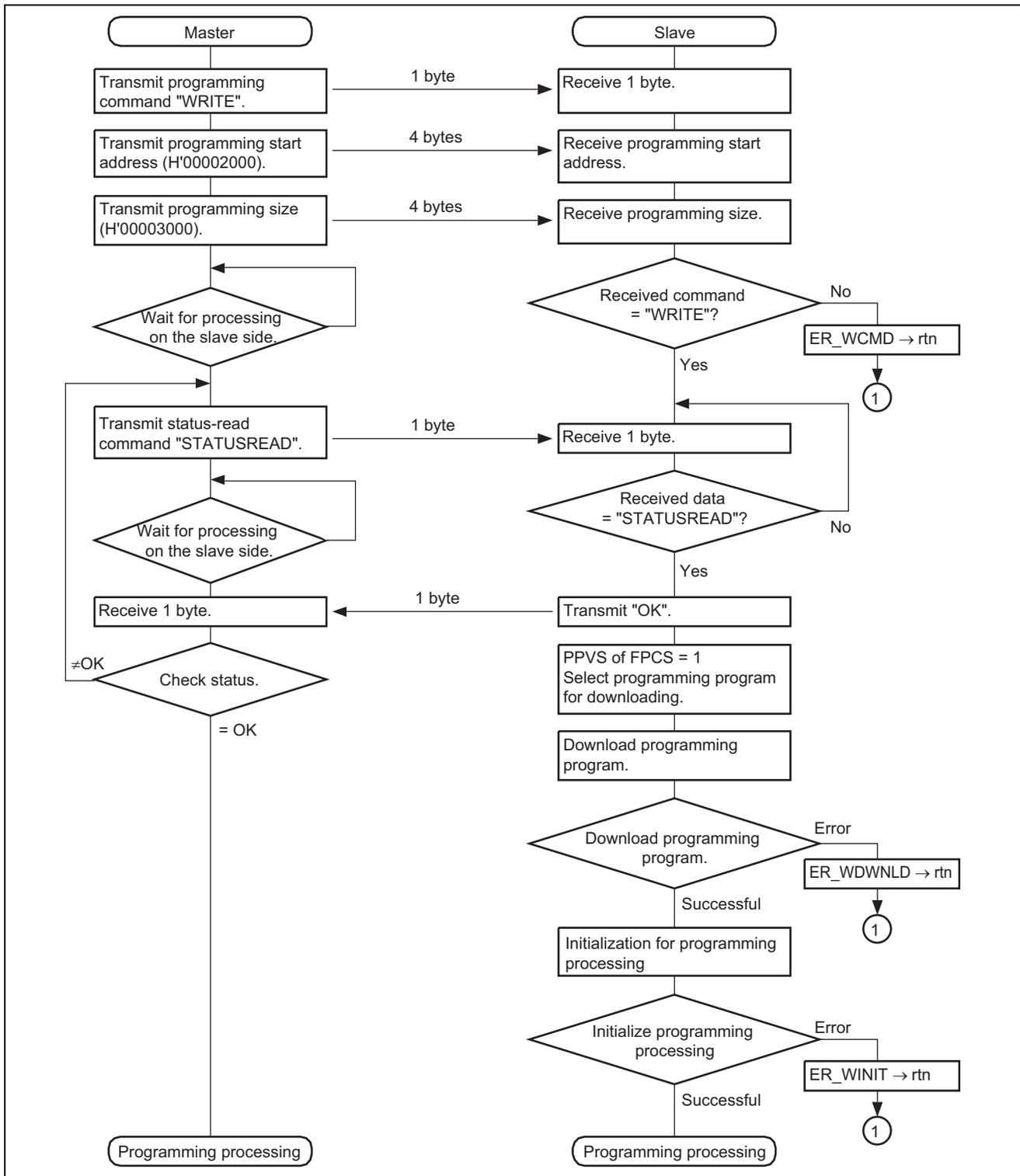


Figure 11 Processing to Receive the Position and Range for Programming

4.3.3 Programming Processing

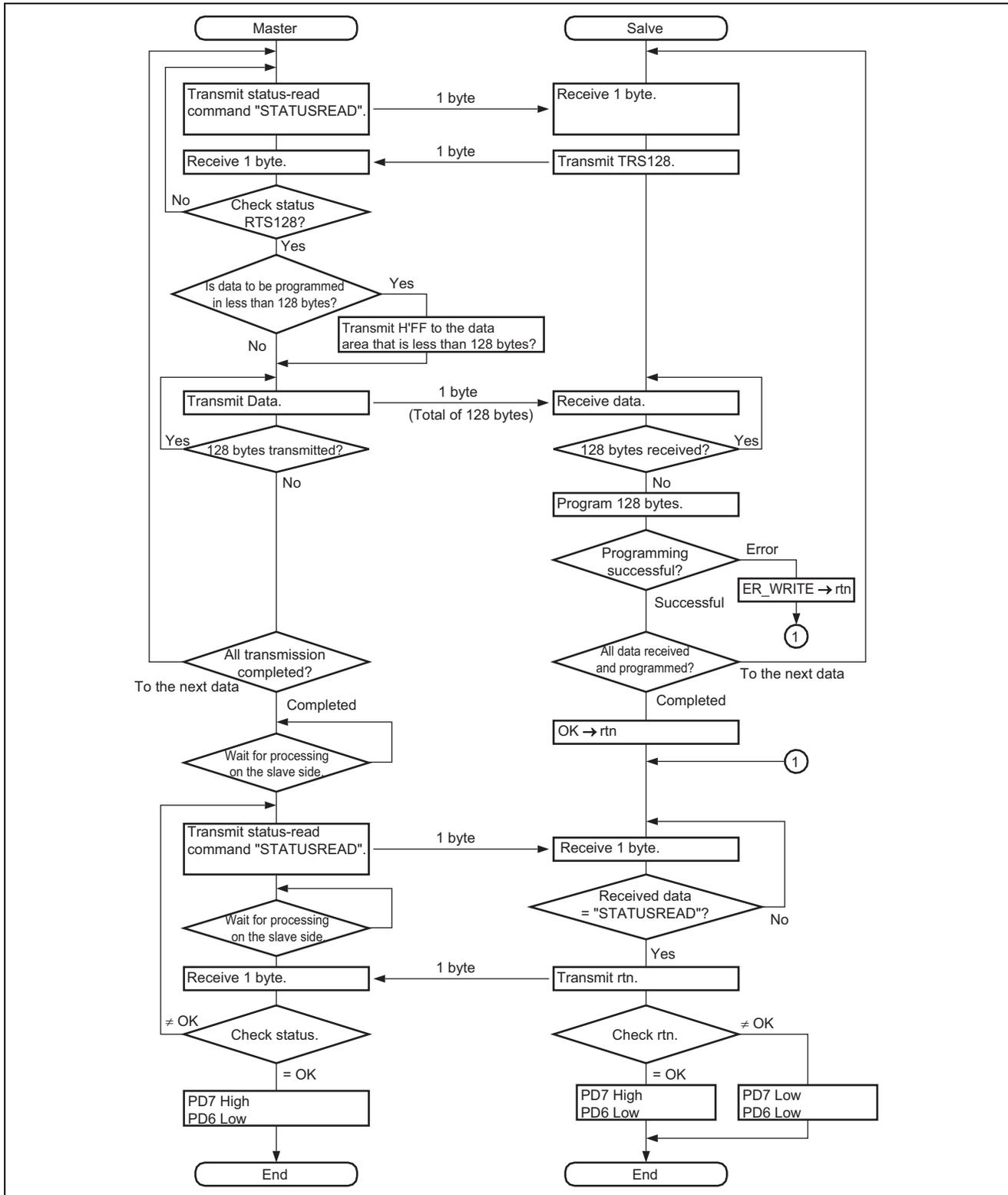


Figure 12 Programming Processing

5. Description of Software for Initialization Program on the Receive Side (Slave)

5.1 List of Functions

The initialization program (main.c) on the receive side is used to transfer the programming/erasing procedure program to the on-chip RAM. A list of functions used in the initialization program on the receive side is given in table 10, and the hierarchical structure of calls is given in figure 13.

Table 10 Functions in the Initialization Program on the Receive Side (Slave)

Function Name	Description
init	Initialization routine Releases from the module stop mode, makes clock settings, and calls the main function.
main	Main routine Transfers the programming/erasing procedure from the user MAT to the on-chip RAM.
copyfzram	Transfers the programming/erasing procedure program from the user MAT to the on-chip RAM.
flew_main	Programming/erasing procedure program in the user MAT.

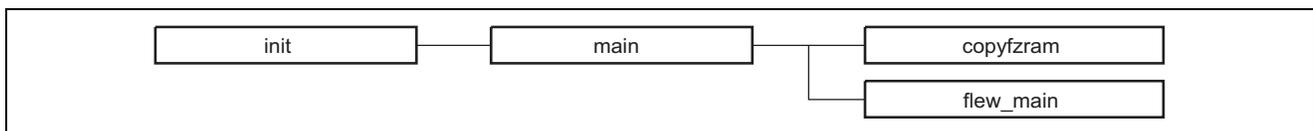


Figure 13 Initialization Program on the Slave Side

5.2 Description of Functions

5.2.1 init Function

1. Functional overview

Initialization routine, releases the module stop mode, sets the clock, and calls the main function.

2. Arguments

None

3. Return value

None

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD1 and MD0; see table 11). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latch is released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD1 and MD0.

Table 11 Values of bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
1	0	0	1	1	1	0	1
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (I ϕ) Select
9	ICK1	0		These bits select the frequency of the system clock provided to the CPU, DMAC, and DTC. 000: Input clock \times 2
8	ICK0	1		
6	PCK2	0	R/W	Peripheral Module Clock (P ϕ) Select
5	PCK1	0		These bits select the frequency of the peripheral module clock. 001: Input clock \times 2
4	PCK0	1		
2	BCK2	0	R/W	External Bus Clock (B ϕ) Select
1	BCK1	0		These bits select the frequency of the external bus clock. 001: Input clock \times 2
0	BCK0	1		

- MSTPCRA, MSTPCRB, and MSTPCRC control the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 releases the module from module stop state.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping the operation of bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode 1: Enables all-module-clock-stop mode
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

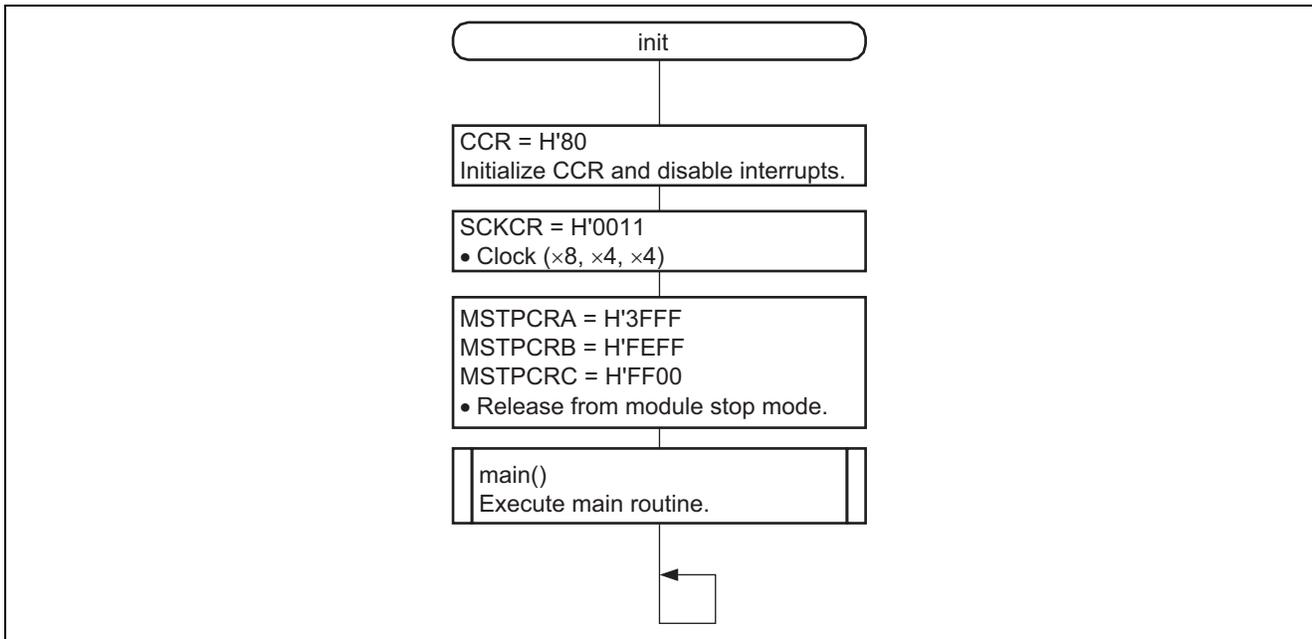
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
11	MSTPB11	0	R/W	Serial communications interface_3 (SCI_3)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
10	MSTPC10	1	R/W	Synchronous serial communications unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communications unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communications unit 0 (SSU_0)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.2.2 main Function

1. Functional overview

- Branches to programming/erasing procedure program

2. Arguments

None

3. Return value

None

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port D data direction register (PDDDR) Number of bits: 8 Address: H'FFFB8C

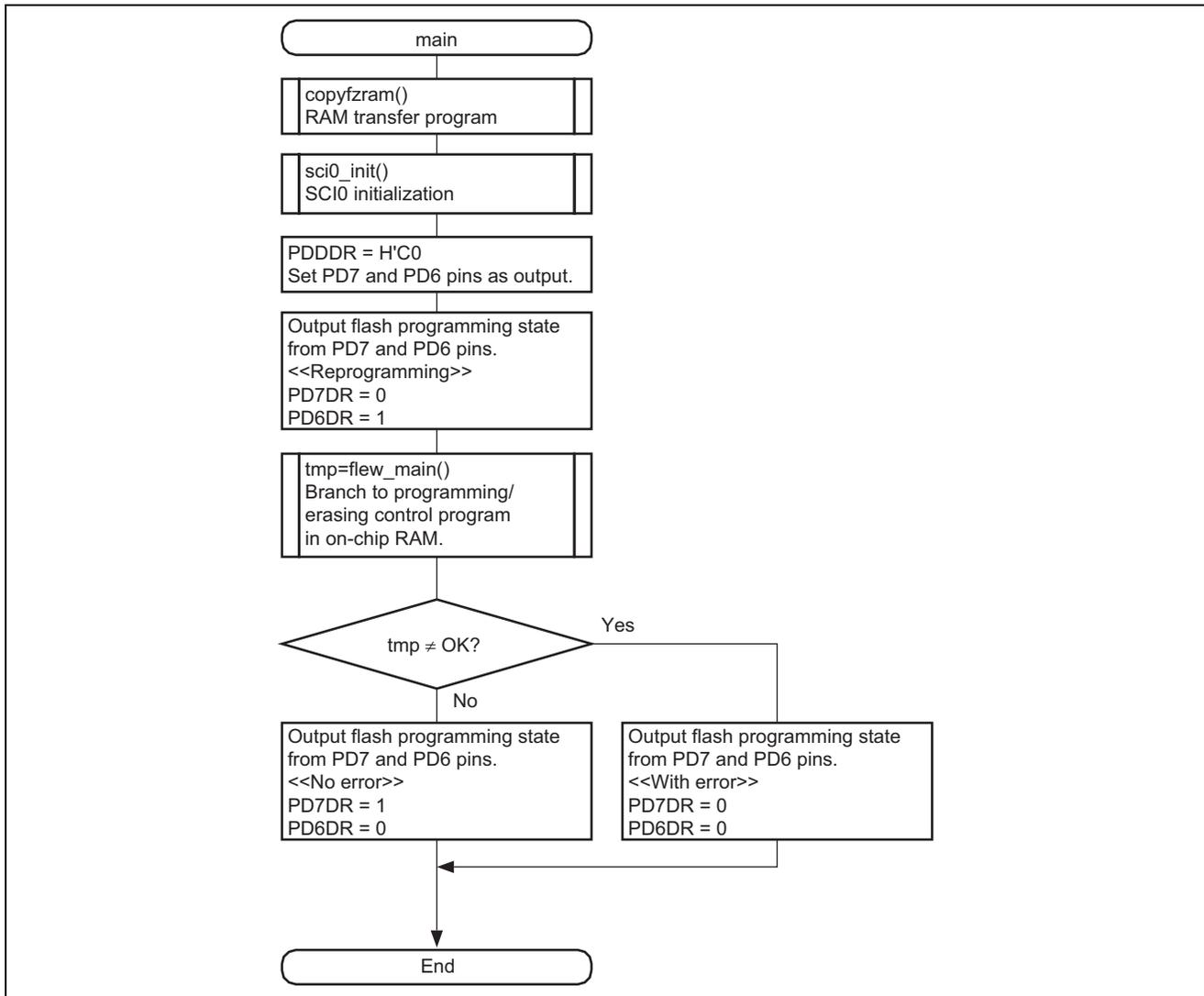
Bit	Bit Name	Setting	R/W	Description
7	PD7DDR	1	R/W	0: Sets PD7 as an input pin. 1: Sets PD7 as an output pin.
6	PD6DDR	1	R/W	0: Sets PD6 as an input pin. 1: Sets PD6 as an output pin.

- Port D data register (PDDR) Number of bits: 8 Address: H'FFF5C

In this sample task, the PD7 and PD6 pins are used for output pins of flash reprogramming.

Bit	Bit Name	Setting	R/W	Description
7	PD7DR	Undefined	R/W	0: PD7 pin is set to a low level. 1: PD7 pin is set to a high level.
6	PD6DR	Undefined	R/W	0: PD6 pin is set to a low level. 1: PD6 pin is set to a high level.

5. Flowchart



5.2.3 copyfzram Function

1. Functional overview

Transfers the programming/erasing procedure program to the on-chip RAM.

2. Arguments

None

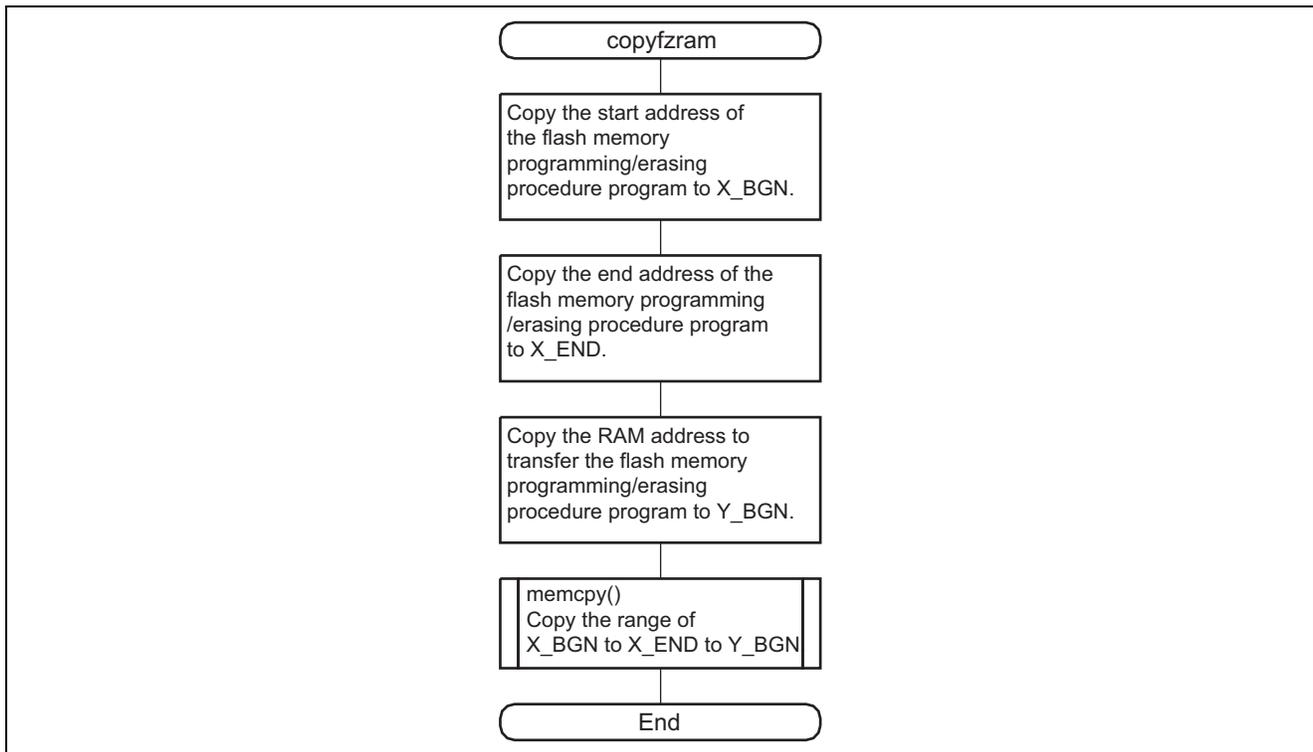
3. Return value

None

4. Internal registers used

None

5. Flowchart



5.2.4 flew_main Function

1. Functional overview

Calls the main routine of the programming/erasing procedure program.

6. Description of Software for Programming/Erasing Procedure Program on the Slave Side

6.1 List of Functions

Programming/erasing procedure program (fwrite.c) performs erasing block units, receives flash memory programming data, and performs programming to flash memory. A list of functions for the routines used in the programming/erasing procedure program is given in table 12. The hierarchical structure is shown in figure 14.

Table 12 List of Functions for Programming/Erasing Procedure Program

Function Name	Description
flew_main	Main processing of flash memory erasing/programming
erase_process	Erases flash memory
write_process	Programs flash memory
download	Downloads on-chip modules
fw_init	Initialization before flash memory erasing and programming

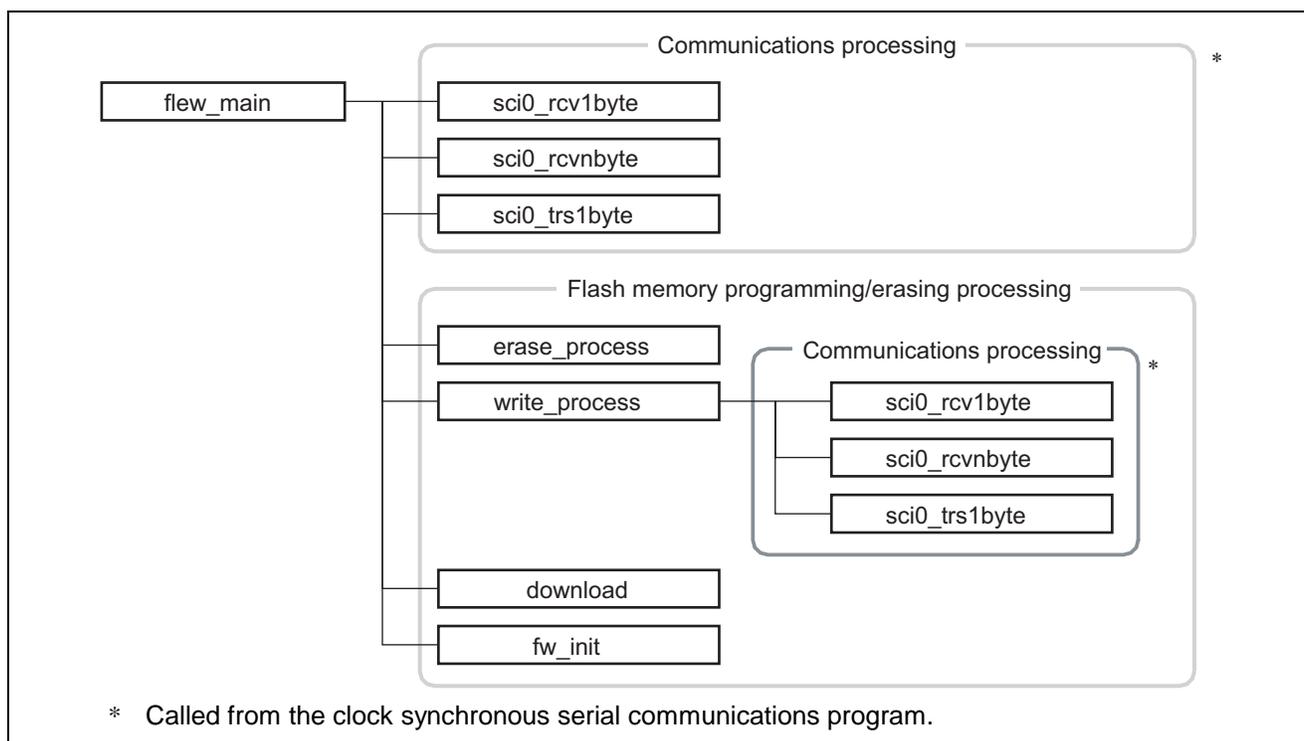


Figure 14 Programming/Erasing Procedure Program

6.2 Description of Functions

6.2.1 flew_main Function

1. Functional overview

Main processing of flash memory erasing/programming

2. Arguments

None

3. Return value

Type	Description
unsigned char	Error status

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System control register (SYSCR) Number of bits: 16 Address: H'FFFDC2

Bit	Bit Name	Setting	R/W	Description
7	FLSHE	1	R/W	Flash Memory Control Register Enable Controls accesses by the CPU to the flash memory control registers. Setting this bit to 1 enables read from/write to the flash memory control registers. Clearing this bit to 0 disables the flash memory control registers. At this time, the contents of the flash memory control registers are retained. 0: Disables the flash memory control registers. 1: Enables the flash memory control registers.

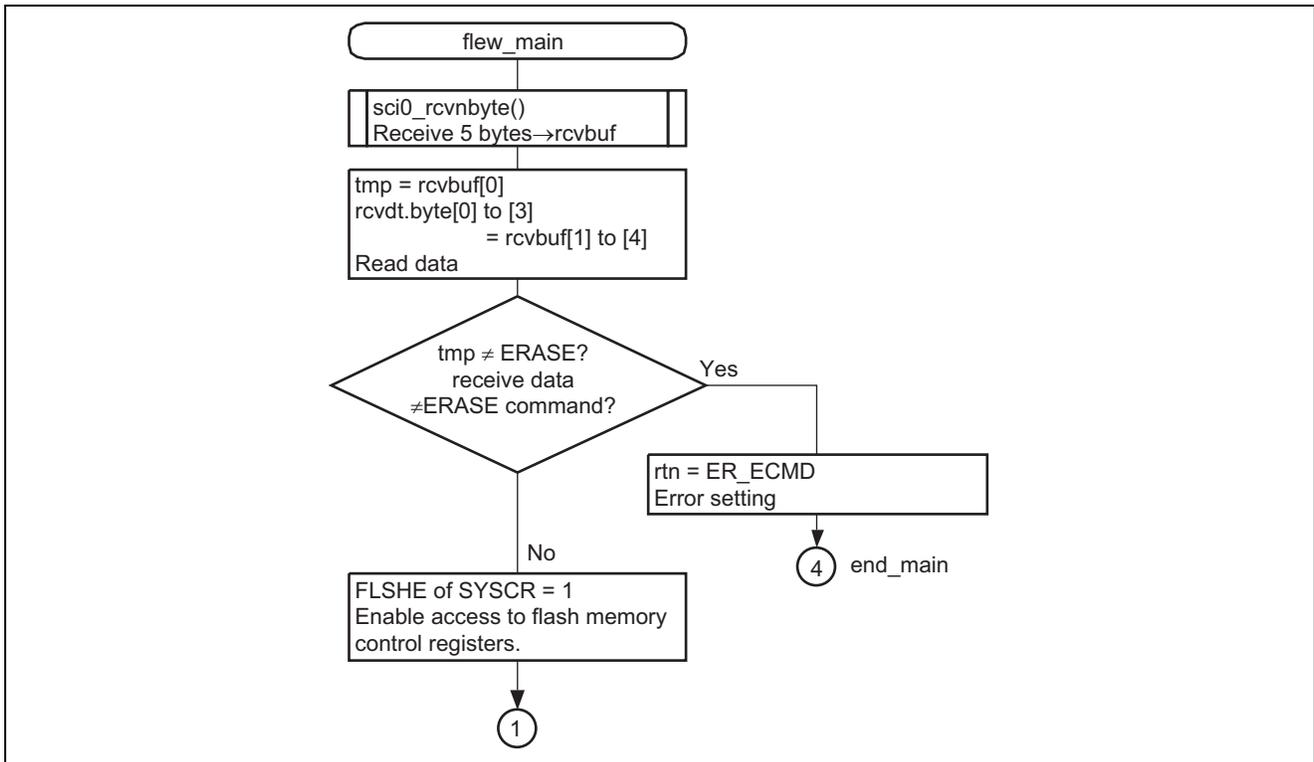
- Flash program code select register (FPCS) Number of bits: 8 Address: H'FFFDE9

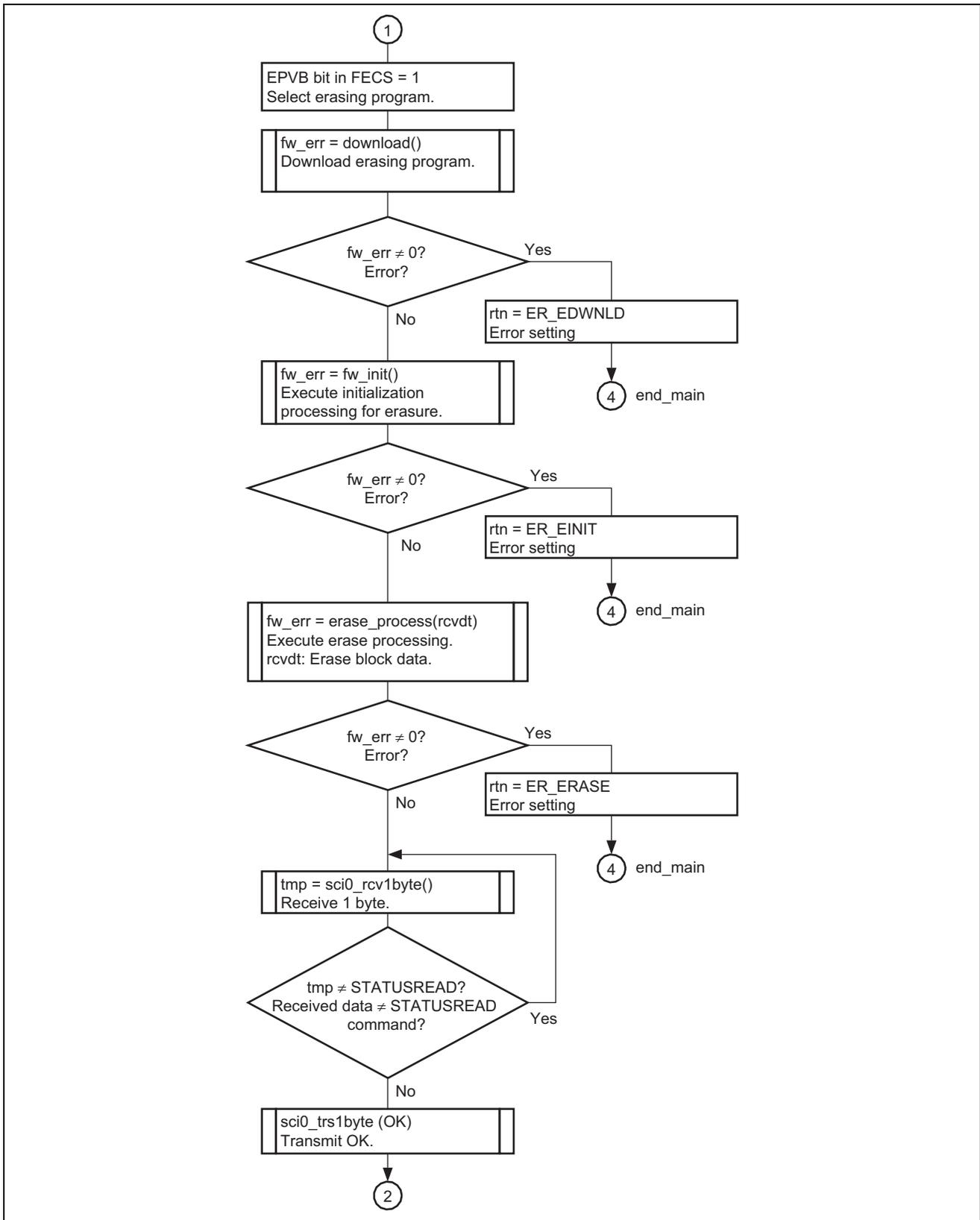
Bit	Bit Name	Setting	R/W	Description
0	PPVS	1	R/W	Program Pulse Verify Selects the programming program to be downloaded. 0: Does not select programming program. [Clearing condition] • Completion of transfer 1: Selects programming program.

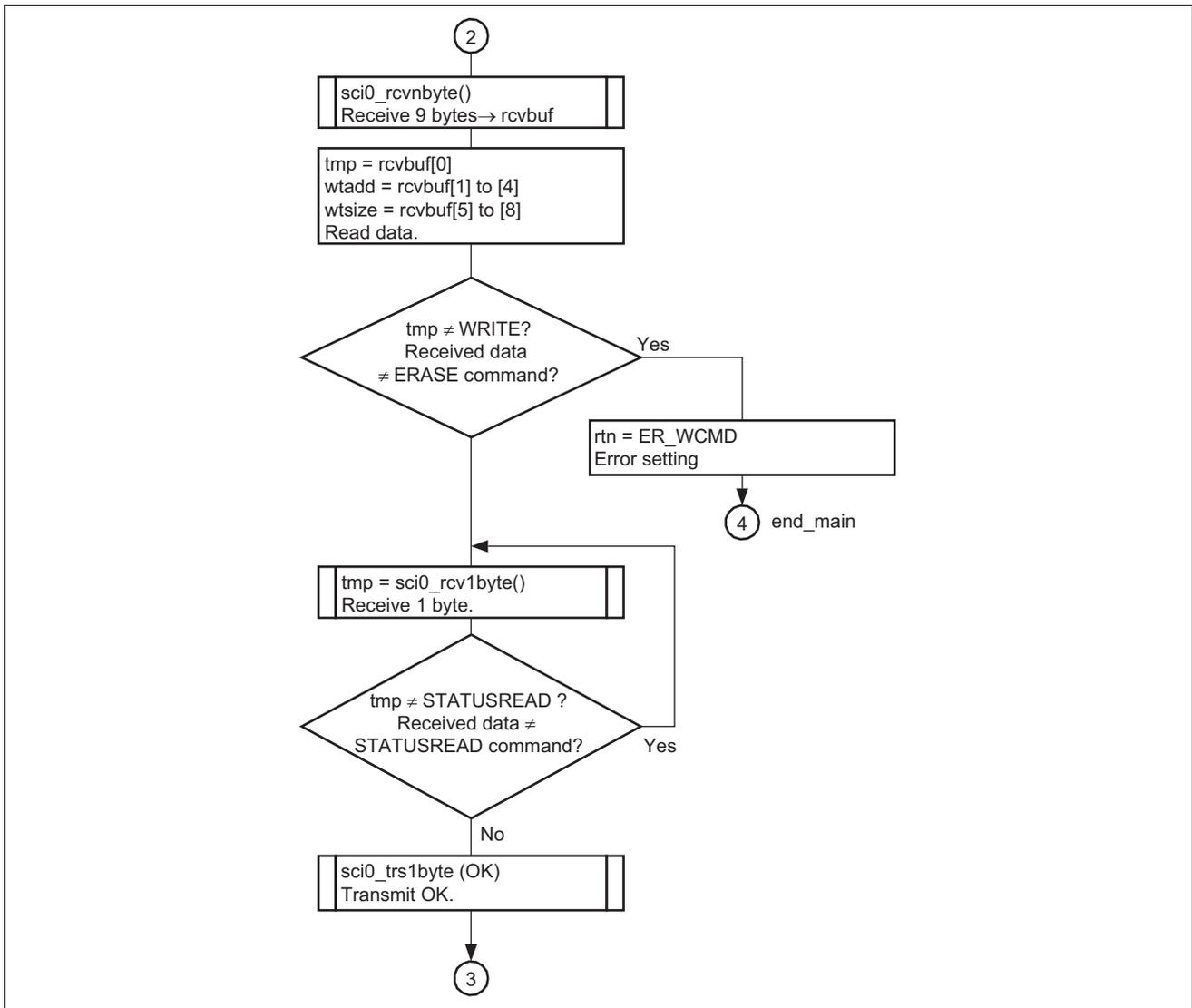
- Flash erase code select register (FECS) Number of bits: 8 Address: H'FFFDEA

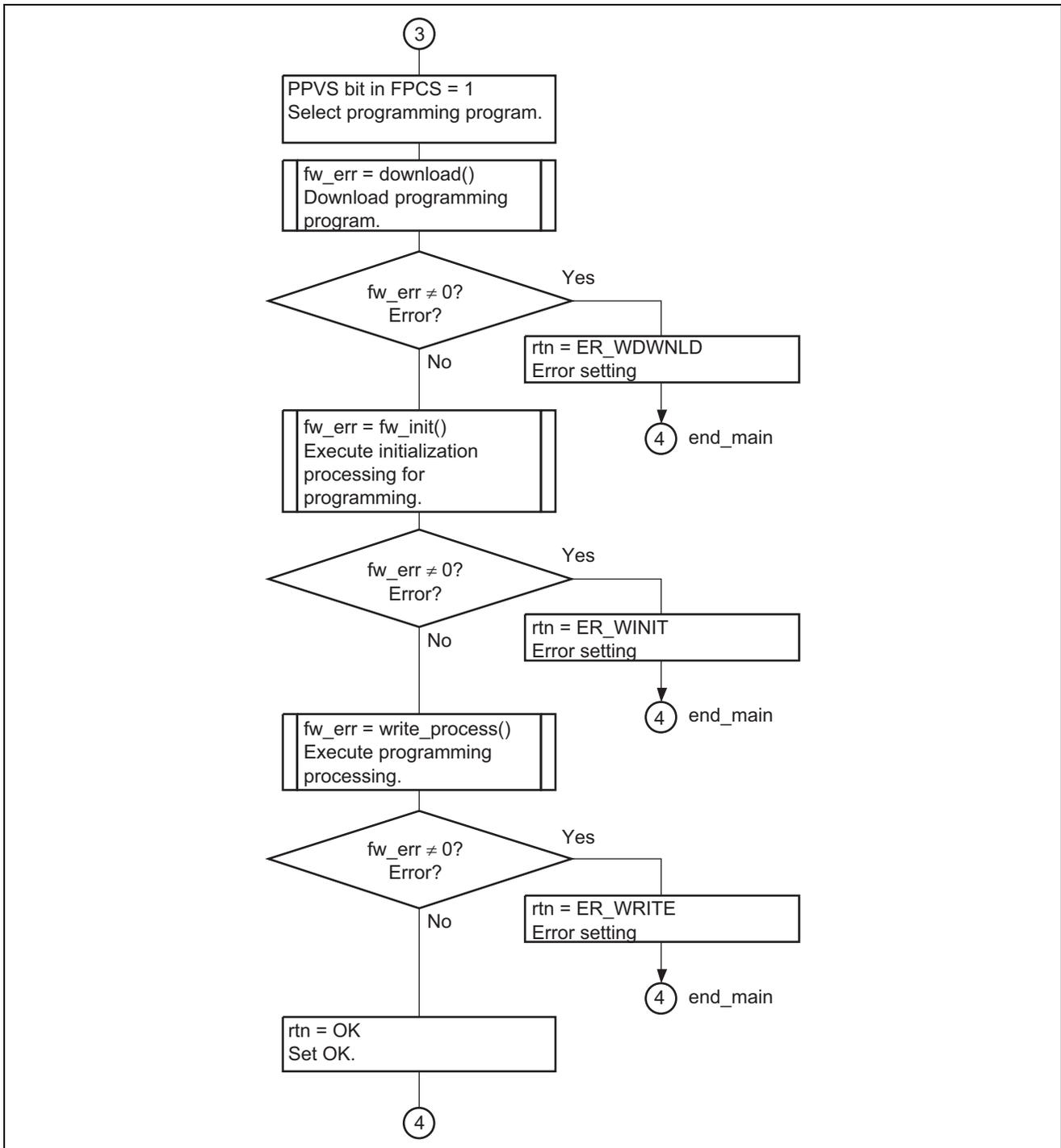
Bit	Bit Name	Setting	R/W	Description
0	EPVB	1	R/W	Erase Pulse Verify Block Selects the erasing program to be downloaded. 0: Does not select erasing program. [Clearing condition] • Completion of transfer 1: Selects erasing program.

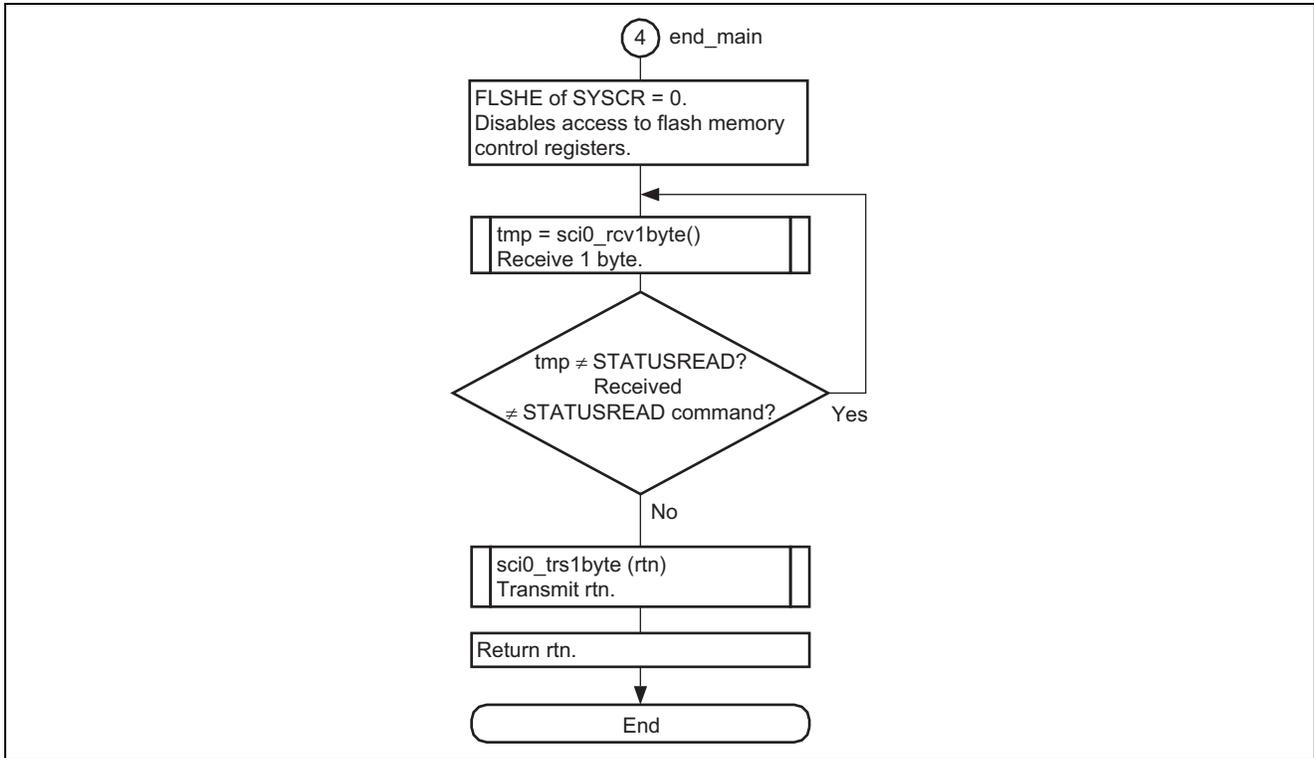
5. Flowchart











6.2.2 erase_process Function

1. Functional overview

Erase flash memory.

2. Arguments

Type	Variable Name	Description
unsigned long	ERASEBLK	Erases block.

3. Return value

Type	Description
unsigned char	Flash pass and fail parameter (FPFR) Return value of the erase result.

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Flash key code register (FKEY) Number of bits: 8 Address: H'FFFDEC

Bit	Bit Name	Setting	R/W	Description
7	K7	0	R/W	Key Code
6	K6	1	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM. Only When H'5A is written, programming/erasing of the flash memory can be executed.
5	K5	0	R/W	
4	K4	1	R/W	
3	K3	1	R/W	
2	K2	0	R/W	
1	K1	1	R/W	When a value other than H'5A is written, even if the programming/erasing program is executed,
0	K0	0	R/W	programming/erasing cannot be performed. H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.) H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'5A, the software protection state is entered.) H'00: Initial value

- Flash MAT select register (FMATS) Number of bits: 8 Address: H'FFFEAD

Bit	Bit Name	Setting	R/W	Description
7	MS7	0	R/W	MAT Selection
6	MS6	0	R/W	The memory MATs can be switched by writing a value to FMATS.
5	MS5	0	R/W	
4	MS4	0	R/W	When H'AA is written to FMATS, the user boot MAT is selected. When a value other than H'AA is written, the user MAT is selected. In the user boot mode:
3	MS3	0	R/W	
2	MS2	0	R/W	H'AA: The user boot MAT is selected. A value other than H'AA: The user MAT is selected.
1	MS1	0	R/W	
0	MS0	0	R/W	

- Flash pass and fail parameter (FPFR)
(CPU general register R0L)

Return value of the erase results

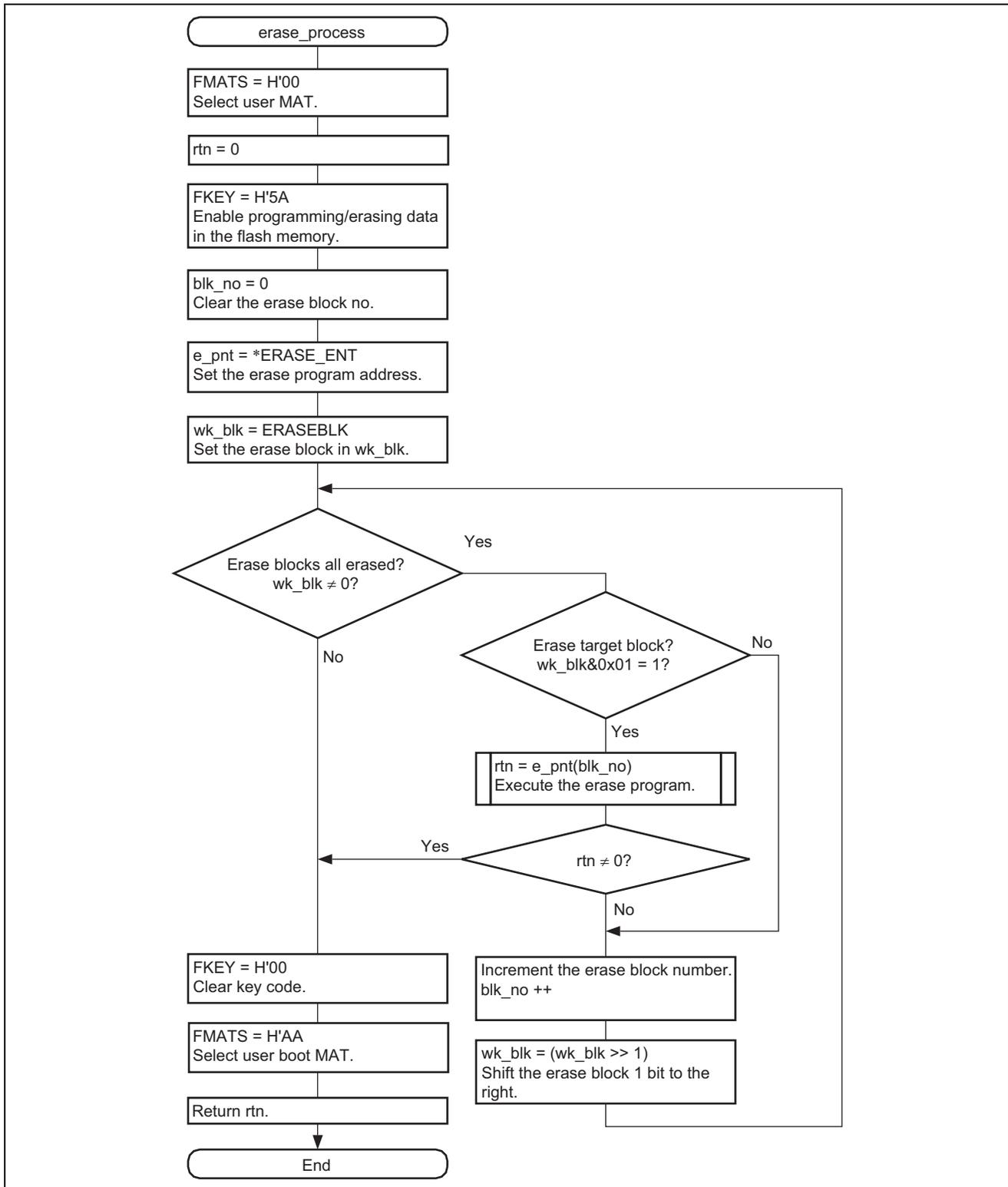
Bit	Bit Name	Setting	R/W	Description
6	MD	Undefined	R/W	Erasing Mode Related Setting Error Detect Detects the error protection state and returns the result. When the error protection state is entered, this bit is set to 1. Whether the error protection state is entered or not can be performed with the FLER bit of the FCCS register. 0: Normal operation (FLER = 0) 1: Error protection state, and programming cannot be performed (FLER = 1)
5	EE	Undefined	R/W	Erasing Execution Error Detect Writes 1 to this bit when the specified data could not be written because the user MAT was not erased. If this is set to 1, there is a high possibility that the user MAT has been written partially. In this case, after removing the error factor, erase the user MAT. 0: Erasure has ended normally. 1: Erasure has ended abnormally.
4	FK	Undefined	R/W	Flash Key Register Error Detect Checks the FKEY value (H'A5) before programming starts, and returns the results. 0: FKEY setting is normal (H'5A). 1: FKEY setting is abnormal (a value other than H'5A).
3	EB	Undefined	R/W	Erase Block Selection Error Detect Checks whether the specified erase block number is in the block range of user MAT and returns the result. 0: Setting of erase block number is normal. 1: Setting of erase block number is abnormal.
0	SF	Undefined	R/W	Success/Fail Indicates the erasure results. 0: Erasure ended normally (no error). 1: Erasure ended abnormally (error occurred).

- Flash erase block select parameter (FEBS)
(CPU general register ER0)

Sets the erase block number in the range from 0 to 19. Number 0 corresponds to block EB0 and number 19 corresponds to block EB19. An error occurs when a number other than 0 to 19 is set.

Setting: blk_no

5. Flowchart



6.2.3 write_process Function

1. Functional overview

Programs flash memory.

2. Arguments

Type	Variable Name	Description
unsigned long	fladr	Reprogramming start address
unsigned long	flsize	Reprogramming size

3. Return value

Type	Description
unsigned char	Flash pass and fail parameter (FPFR) Return value of the programming result.

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Flash key code register (FKEY) Number of bits: 8 Address: H'FFFDEC

Bit	Bit Name	Setting	R/W	Description
7	K7	0	R/W	Key code
6	K6	1	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM. Only When H'5A is written, programming/erasing of the flash memory can be executed.
5	K5	0	R/W	
4	K4	1	R/W	When a value other than H'5A is written, even if the programming/erasing program is executed, programming/erasing cannot be performed.
3	K3	1	R/W	
2	K2	0	R/W	H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.) H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'5A, the software protection state is entered.)
1	K1	1	R/W	
0	K0	0	R/W	H'00: Initial value

- Flash MAT select register (FMATS) Number of bits: 8 Address: H'FFFEAD

Bit	Bit Name	Setting	R/W	Description
7	MS7	0	R/W	MAT Selection
6	MS6	0	R/W	The memory MATs can be switched by writing a value to FMATS.
5	MS5	0	R/W	
4	MS4	0	R/W	When H'AA is written to FMATS, the user boot MAT is selected. When a value other than H'AA is written, the user MAT is selected. In the user boot mode:
3	MS3	0	R/W	
2	MS2	0	R/W	H'AA: The user boot MAT is selected. A value other than H'AA: The user MAT is selected.
1	MS1	0	R/W	
0	MS0	0	R/W	

- Flash pass and fail parameter (FPFR)
(CPU general register R0L)

Return value of the erase results

Bit	Bit Name	Setting	R/W	Description
6	MD	Undefined	R/W	<p>Programming Mode Related Setting Error Detect</p> <p>Detects the error protection state and returns the result. When the error protection state is entered, this bit is set to 1. Whether the error protection state is entered or not can be performed with the FLER bit of the FCCS register.</p> <p>0: Normal operation (FLER = 0)</p> <p>1: Error protection state, and programming cannot be performed (FLER = 1)</p>
5	EE	Undefined	R/W	<p>Programming Execution Error Detect</p> <p>Writes 1 to this bit when the specified data could not be written because the user MAT was not erased. If this is set to 1, there is a high possibility that the user MAT has been written partially. In this case, after removing the error factor, erase the user MAT.</p> <p>0: Erasure has ended normally.</p> <p>1: Erasure has ended abnormally.</p>
4	FK	Undefined	R/W	<p>Flash Key Register Error Detect</p> <p>Checks the FKEY value (H'A5) before programming starts, and returns the results.</p> <p>0: FKEY setting is normal (H'5A).</p> <p>1: FKEY setting is abnormal (a value other than H'5A).</p>
2	WD	Undefined	R/W	<p>Write Data Address Detect</p> <p>When an address not in the flash memory area is specified as the start address of the storage destination for the program data, an error occurs.</p> <p>0: Setting of the start address of the storage destination for the program data is normal.</p> <p>1: Setting of the start address of the storage destination for the program data is abnormal.</p>
1	WA	Undefined	R/W	<p>Write Address Error Detect</p> <p>When the following items are specified as the start address of the programming destination, an error occurs.</p> <ul style="list-style-type: none"> An area other than flash memory The specified address is not aligned with the 128-byte boundary. (lower eight bits of the address are other than H'00 and H'80) <p>0: Setting of the start address of the programming destination is normal.</p> <p>1: Setting of the start address of the programming destination is abnormal.</p>
0	SF	Undefined	R/W	<p>Success/Fail</p> <p>Indicates the program results.</p> <p>0: Programming ended normally (no error).</p> <p>1: Programming ended abnormally (error occurred).</p>

- Flash multipurpose address area parameter (FMPAR)
(CPU general register ER1)

FMPAR sets the start address of the programming destination on the user MAT.

When an address in an area other than the flash memory is set, or the start address of the programming destination is not aligned with the 128-byte boundary, an error occurs. The error occurrence is indicated by the WA bit of the FPCR register.

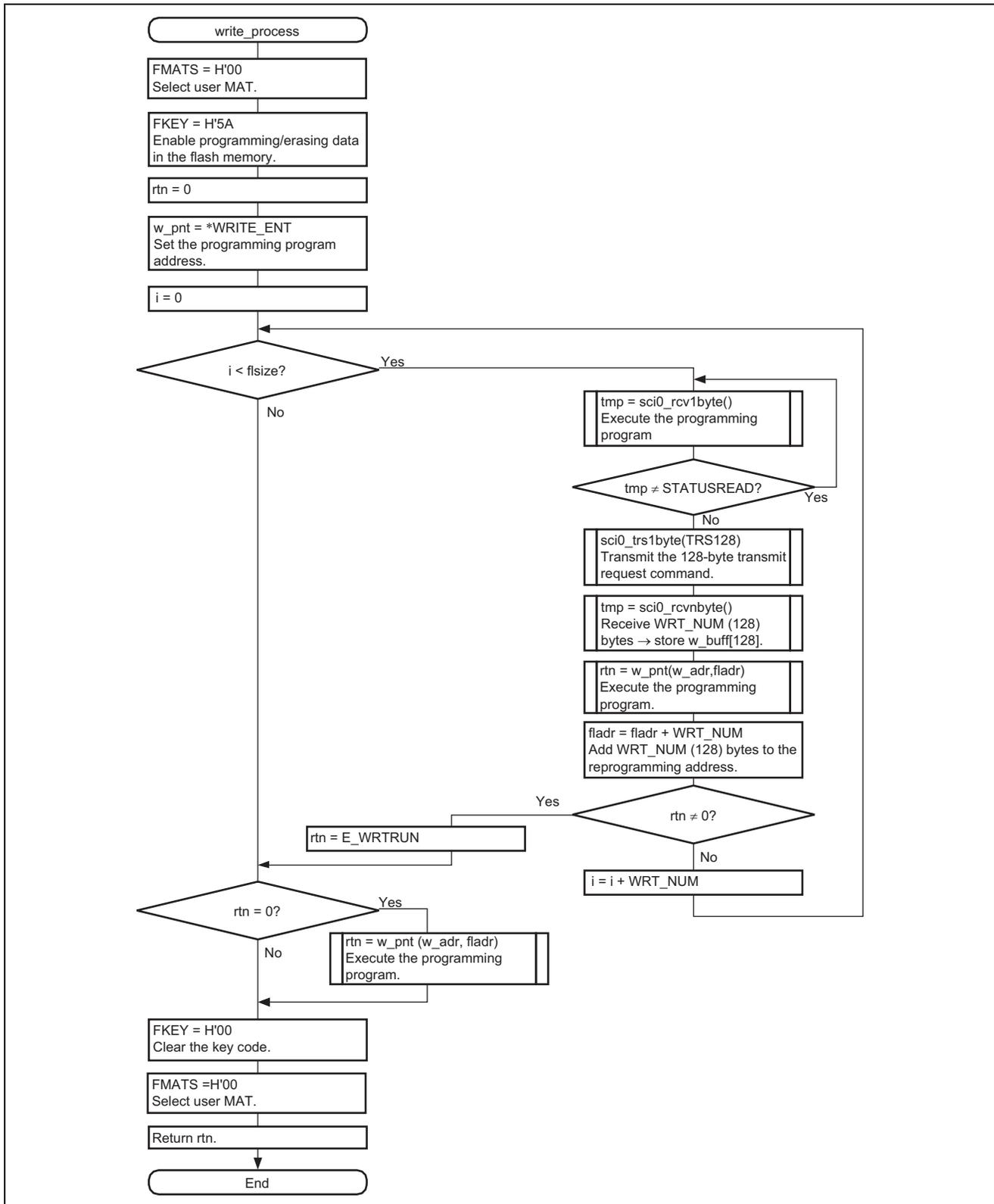
Bit	Bit Name	Setting	R/W	Description
31 to 0	MOA31 to MOA0	fladr (local variable)	R/W	Sets the start address of the programming destination on the user MAT. Consecutive 128-byte programming is executed starting from the specified start address of the user MAT. Therefore, the specified start address of the programming destination becomes a 128-byte boundary, and MOA6 to MOA0 are always cleared to 0.

- Flash multipurpose data destination parameter (FMPDR)
(CPU general register ER0)

FMPDR sets the start address in the area which stores the data to be programmed in the user MAT. When the storage destination for the program data is in flash memory, an error occurs. The error occurrence is indicated by the WD bit in FPCR.

Bit	Bit Name	Setting	R/W	Description
31 to 0	MOD31 to MOD0	fladr (local variable)	R/W	Sets the start address of the area which stores the program data for the user MAT. Consecutive 128-byte data is programmed to the user MAT starting from the specified start address.

5. Flowchart



6.2.4 download Function

1. Functional overview

Downloads the on-chip modules.

2. Arguments

None

3. Return value

Type	Description
unsigned char	Download pass and fail result parameter (DPFR) Return value of the download result.

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Flash key code register (FKEY) Number of bits: 8 Address: H'FFFDEC

Bit	Bit Name	Setting	R/W	Description
7	K7	1	R/W	Key Code
6	K6	0	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is enabled. When a value other than H'A5 is written, the SCO bit cannot be set to 1. Therefore, the on-chip program cannot be downloaded to the on-chip RAM. Only When H'5A is written, programming/erasing of the flash memory can be executed.
5	K5	1	R/W	
4	K4	0	R/W	When a value other than H'5A is written, even if the programming/erasing program is executed, programming/erasing cannot be performed.
3	K3	0	R/W	
2	K2	1	R/W	H'A5: Writing to the SCO bit is enabled. (The SCO bit cannot be set to 1 when FKEY is a value other than H'A5.)
1	K1	0	R/W	
0	K0	1	R/W	H'5A: Programming/erasing of the flash memory is enabled. (When FKEY is a value other than H'5A, the software protection state is entered.)
H'00: Initial value				

- Flash transfer destination address register (FTDAR) Number of bits: 8 Address: H'FFFDEE

Bit	Bit Name	Setting	R/W	Description
7	TDER	0	R/W	<p>Transfer Destination Address Setting Error</p> <p>This bit is set to 1 when an error has occurred in setting the start address specified by bits TDA6 to TDA0. A start address error is determined by whether the value set in bits TDA6 to TDA0 is within the range of H'00 to H'02 when download is executed by setting the SCO bit in FCCS to 1. Make sure that this bit is cleared to 0 before setting the SCO bit to 1 and the value specified by bits TDA6 to TDA0 should be within the range of H'00 to H'02.</p> <p>0: The value specified by bits TDA6 to TDA0 is written the range.</p> <p>1: The value specified by TDER and bits TDA6 to TDA0 is between H'03 and H'FF and download has stopped.</p>
6	TDA6	0	R/W	<p>Transfer Destination Address</p> <p>Specifies the on-chip RAM start address of the download destination. A value between H'00 and H'02, and up to 4 Kbytes can be specified as the start address of the on-chip RAM.</p> <p>H'00: H'FF9000 is specified as the start address. H'01: H'FFA000 is specified as the start address. H'02: H'FFB000 is specified as the start address. H'03 to H'7F: Setting prohibited. (Specifying a value from H'03 to H7F sets the TDER bit to 1 and stops download of the on-chip program.)</p>
5	TDA5	0	R/W	
4	TDA4	0	R/W	
3	TDA3	0	R/W	
2	TDA2	0	R/W	
1	TDA1	1	R/W	
0	TDA0	0	R/W	

- Flash code control status register (FCCS) Number of bits: 8 Address: H'FFFDE8

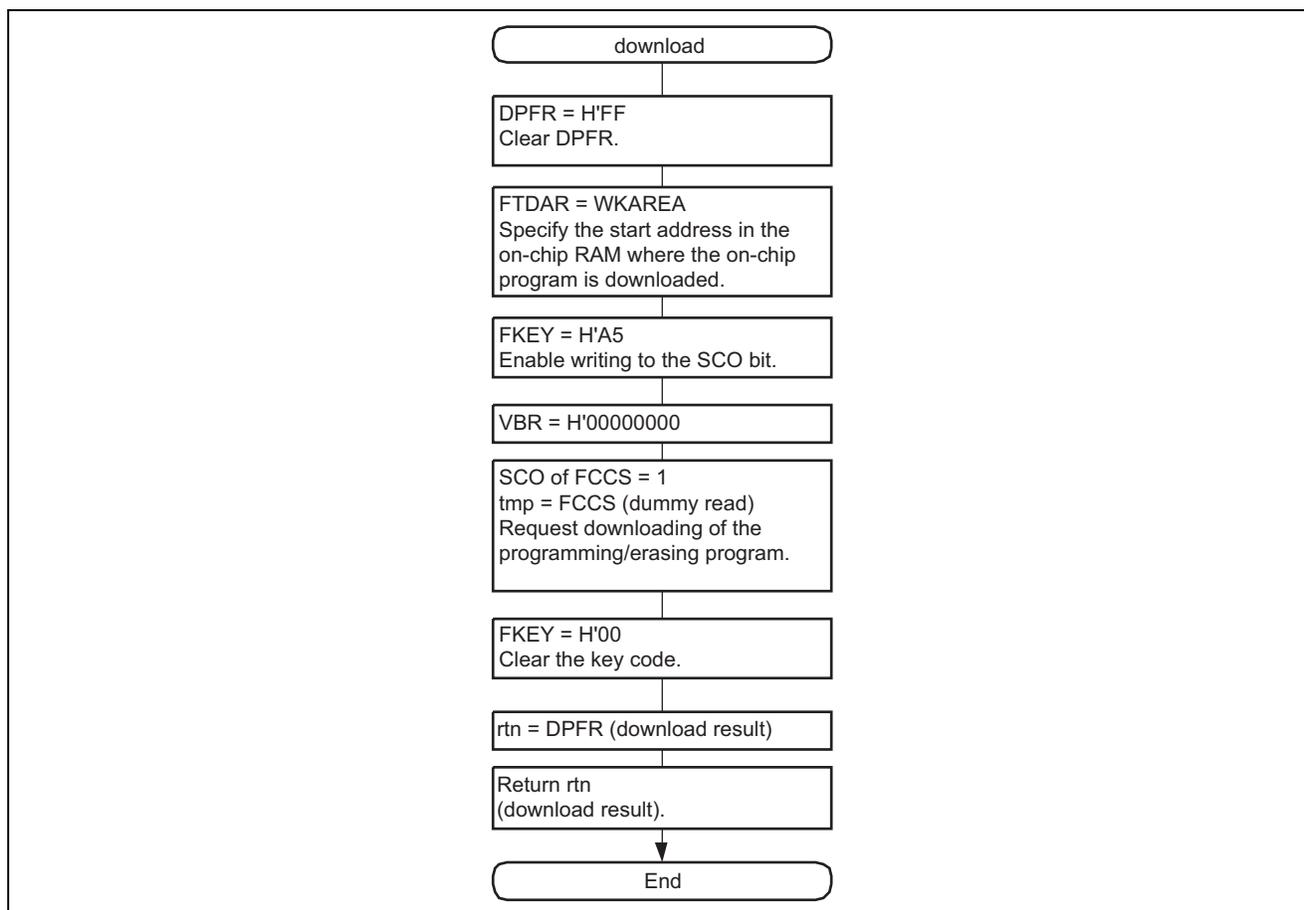
Bit	Bit Name	Setting	R/W	Description
4	FLER	0	R	<p>Flash Memory Error</p> <p>Indicates that an error has occurred during programming/erasing the flash memory. When this bit is set to 1, the flash memory enters the error protection state. When this bit is set to 1, high voltage is applied to the internal flash memory. To reduce the damage to the flash memory, the reset must be released after the reset input period (period of $\overline{RES} = 0$) of at least 100 μs.</p> <p>0: Flash memory operates normally (Error protection is invalid). [Clearing condition]</p> <ul style="list-style-type: none"> At a power-on reset <p>1: An error occurs during programming/erasing flash memory (error protection is valid). [Setting conditions]</p> <ul style="list-style-type: none"> When an interrupt, such as NMI, occurs during programming/erasing. When the flash memory is read during programming/erasing (including a vector read and an instruction fetch). When the SLEEP instruction is executed during programming/erasing (including software standby mode). When a bus master other than the CPU, such as the DTC and DMAC, obtains bus mastership during programming/erasing.
0	SCO	0	(R)/W*	<p>Source Program Copy Operation</p> <p>Requests the on-chip programming/erasing program to be downloaded to the on-chip RAM. When this bit is set to 1, the on-chip program which is selected by FPCS or FECS is automatically downloaded in the on-chip RAM area specified by FTDAR.</p> <p>In order to set this bit to 1, the RAM emulation mode must be canceled, H'A5 must be written to FKEY, and the setting of SCO bit must be executed in the on-chip RAM. Dummy read of FCCS must be executed twice immediately after setting this bit to 1. All interrupts must be disabled during download. This bit is cleared to 0 when download is completed.</p> <p>During program download initiated with this bit, particular processing which accompanies bank switching of the program storage area is executed.</p> <p>Before a download request, initialize the VBR contents to H'00000000. After download is completed, the VBR contents can be changed.</p> <p>0: Download of the programming/erasing program is not requested. [Clearing condition]</p> <ul style="list-style-type: none"> When download is completed. <p>1: Download of the programming/erasing program is not requested. [Setting conditions] (When all of the following conditions are satisfied.)</p> <ul style="list-style-type: none"> Not in RAM emulation mode (The RAMS bit of RAMER is cleared to 0). H'A5 is written to FKEY. Setting of SCO bit in FCCS is executed in the on-chip RAM.

Note: * SCO is a write-only bit. This bit is always read as 0.

- Download pass and fail result parameter (DPFR)
 (Single byte of start address in on-chip RAM specified by FTDAR.)
 DPFR indicates the return value of the download result. The DPFR value is used to determine the download result.

Bit	Bit Name	Setting	R/W	Description
2	SS	1	R/W	Source Select Error Detect Only one type can be specified for the on-chip program which can be downloaded. When the program to be downloaded is not selected, more than two types of programs are selected, or a program which is not mapped is selected, an error occurs. 0: Download program selection is normal. 1: Download program selection is abnormal.
1	FK	1	R/W	Flash Key Register Error Detect Checks the FKEY value (H'A5) and returns the result. 0: FKEY setting is normal (H'A5). 1: FKEY setting is abnormal (value other than H'A5)
0	SF	1	R/W	Success/Fail Returns the download result. Reads back the program downloaded to the on-chip RAM and determines whether it has been transferred to the on-chip RAM. 0: Download of the program has ended normally. 1: Download of the program has ended abnormally (error occurred).

5. Flowchart



6.2.5 fw_init Function

1. Functional overview

Initializes flash memory before programming.

2. Arguments

None

3. Return value

Type	Description
unsigned char	Flash pass and fail parameter (FPFR) Return value of the initialization result.

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Flash program/erase frequency parameter (FPEFEQ)
(CPU general register ER0)

FPEFEQ sets the operating frequency of the CPU. The CPU operating frequency available in this LSI ranges from 8 to 50 MHz.

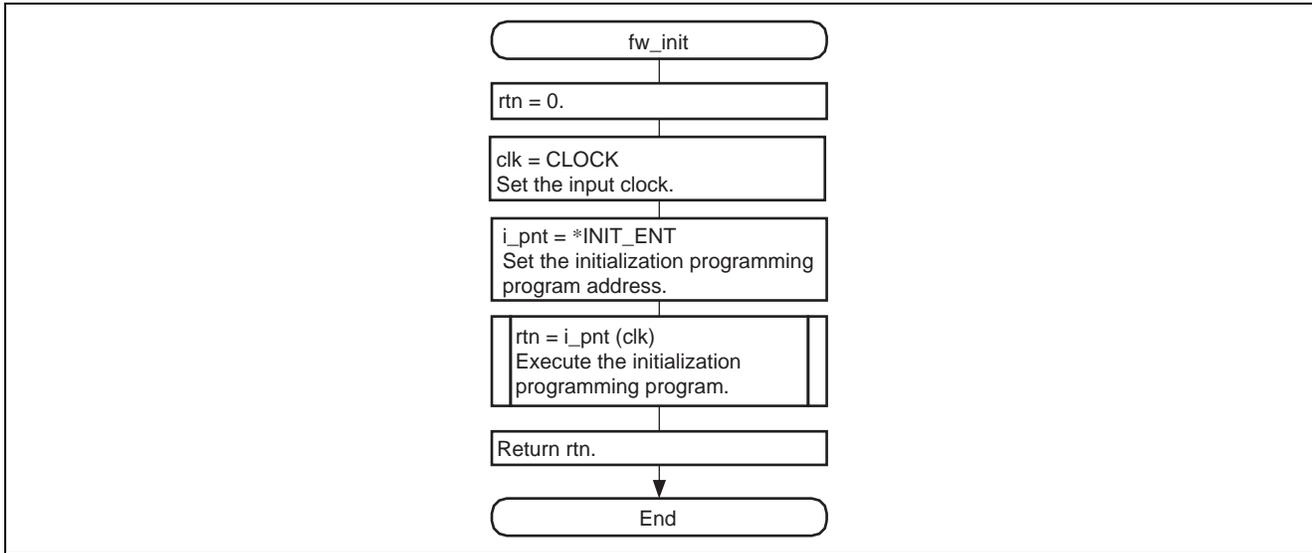
Bit	Bit Name	Setting	R/W	Description
15 to 0	F15 to F0	CLOCK	R/W	Frequency Set Sets the operating frequency of the CPU. When the PLL multiplication function is used, set the multiplied frequency. The setting value must be calculated as follows: <ul style="list-style-type: none"> The operating frequency shown in MHz units must be rounded in a number of three decimal places and be shown in a number of two decimal places. The value multiplied by 100 is converted to the binary digit and is written to FPEFEQ (general register ER0). For example, when the operating frequency of the CPU is 35.000MHz, the value is as follows: <ol style="list-style-type: none"> The number of three decimal places of 35.000 is rounded. The formula of $35.00 \times 100 = 3500$ is converted to the binary digit and B'0000 1101 1010 1100 (H'0CE4) is set to ER0.

- Flash pass and fail parameter (FPFR)
(CPU general register R0L)

Return value of the initialization results

Bit	Bit Name	Setting	R/W	Description
1	FQ	Undefined	R/W	Frequency Error Detect Compares the specified CPU operating frequency with the operating frequencies supported by this LSI, and returns the result. 0: Setting of operating frequency is normal. 1: Setting of operating frequency is abnormal.
0	SF	Undefined	R/W	Success/Fail Indicates the erasure results. 0: Erasure ended normally (no error). 1: Erasure ended abnormally (error occurred).

5. Flowchart



7. Description of Software for the Clock Synchronous Serial Communications Program on the Slave Side

7.1 List of Functions

The clock synchronous serial communications program (sci0.c) performs communications processing to the master side. Table 13 is a list of functions in the clock synchronous serial communications program, and figure 15 shows the hierarchy structure.

Table 13 Functions in the Clock Synchronous Serial Communications Program

Function Name	Description
sci0_init	Initializes clock synchronous serial communications
sci0_rcv1byte	Receives one byte of data
sci0_rcvnbyte	Receives n bytes of data
sci0_trs1byte	Transmits one byte of data
sci0_trsnbyte	Transmits n bytes of data

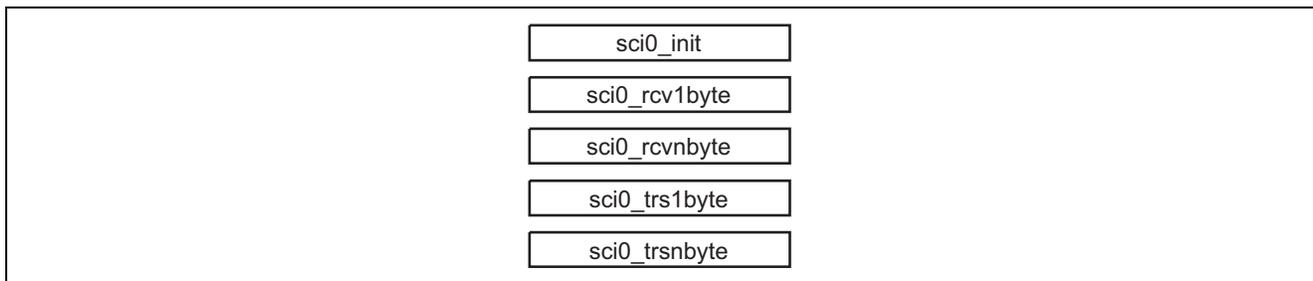


Figure 15 Clock Synchronous Serial Communications Program

7.2 Description of Functions

7.2.1 sci0_init Function

1. Functional overview

Initializes clock synchronous serial communications

2. Arguments

None

3. Return value

None

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Serial mode register_0 (SMR_0) Number of bits: 8 Address: H'FFFF80

Bit	Bit Name	Setting	R/W	Description
7	C/A	1	R/W	Communications Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length 0: Selects 8 bits as the data length 1: Selects 7 bits as the data length
1	CKS1	0	R/W	Clock Selection 1, 0
0	CKS0	0	R/W	B'00: Clock source of the on-chip baud rate generator is set to P ϕ clock.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.
4	RE	0	R/W	Receive Enable 0: Disables reception. 1: Enables reception.
1	CKE1	0	R/W	Clock Enable 1, 0
0	CKE0	0	R/W	In the clock synchronous mode: B'00: Internal clock is used for clock source, and SCK3 pin is set to clock output pin. B'1X: External clock is used for clock source, and SCK3 pin is set to clock input pin.

Legend

X: Don't care.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty 0: Transmit data written to TDR is not transferred to TSR. 1: Transmit data is not written to TDR, or transmit data written to TDR is not transferred to TSR.
6	RDRF	Undefined	R/(W)*	Receive Data Register Full 0: No receive data is stored in RDR. 1: The receive data is stored in RDR.
5	ORER	0	R/(W)*	Overrun Error 0: No overrun error. 1: Overrun error occurred during receive operation.
2	TEND	Undefined	R	Transmit End 0: In transmission 1: Transmission completed

Note: * Only 0 can be written here, to clear the flags.

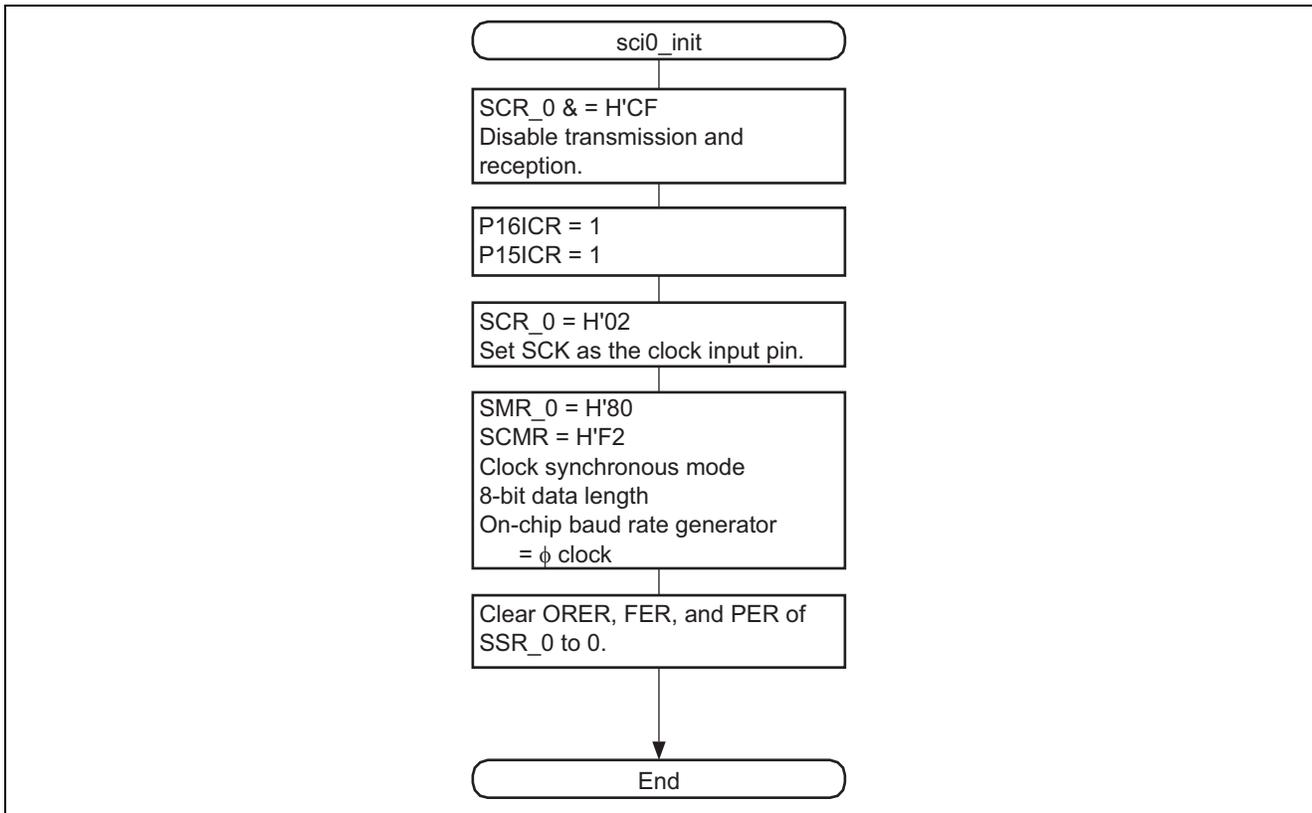
- Port 1 input buffer control register (P1ICR) Number of bits: 8 Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Description
6	P16ICR	1	R/W	0: Input buffer for P16 (SCK3) pin is disabled. 1: Input buffer for P16 (SCK3) pin is enabled.
5	P15ICR	1	R/W	0: Input buffer for P15 (RxD3) pin is disabled. 1: Input buffer for P15 (RxD3) pin is enabled.

- Smart card mode register_0 (SCMR_0) Number of bits: 8 Address: H'FFFE8E

Bit	Bit Name	Setting	R/W	Description
0	SMIF	0	R/W	Smart card interface mode select 0: Operates in normal asynchronous or clock synchronous mode. 1: Operates in smart card interface.

5. Flowchart



7.2.2 sci0_rcv1byte Function

1. Functional overview

Receives one byte of clock synchronous serial data.

2. Arguments

None

3. Return value

Type

Description

Type	Description
unsigned char	Receives one byte of data.

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
-----	----------	---------	-----	-------------

4	RE	0	R/(W)*	Receive Enable 0: Disables reception. 1: Enables reception.
---	----	---	--------	---

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
-----	----------	---------	-----	-------------

6	RDRF	Undefined	R/(W)*	Receive Data Register Full 0: No receive data is stored in RDR. 1: The receive data is stored in RDR.
---	------	-----------	--------	---

5	ORER	Undefined	R/(W)*	Overrun Error 0: No overrun error. 1: Overrun error occurred during receive operation.
---	------	-----------	--------	--

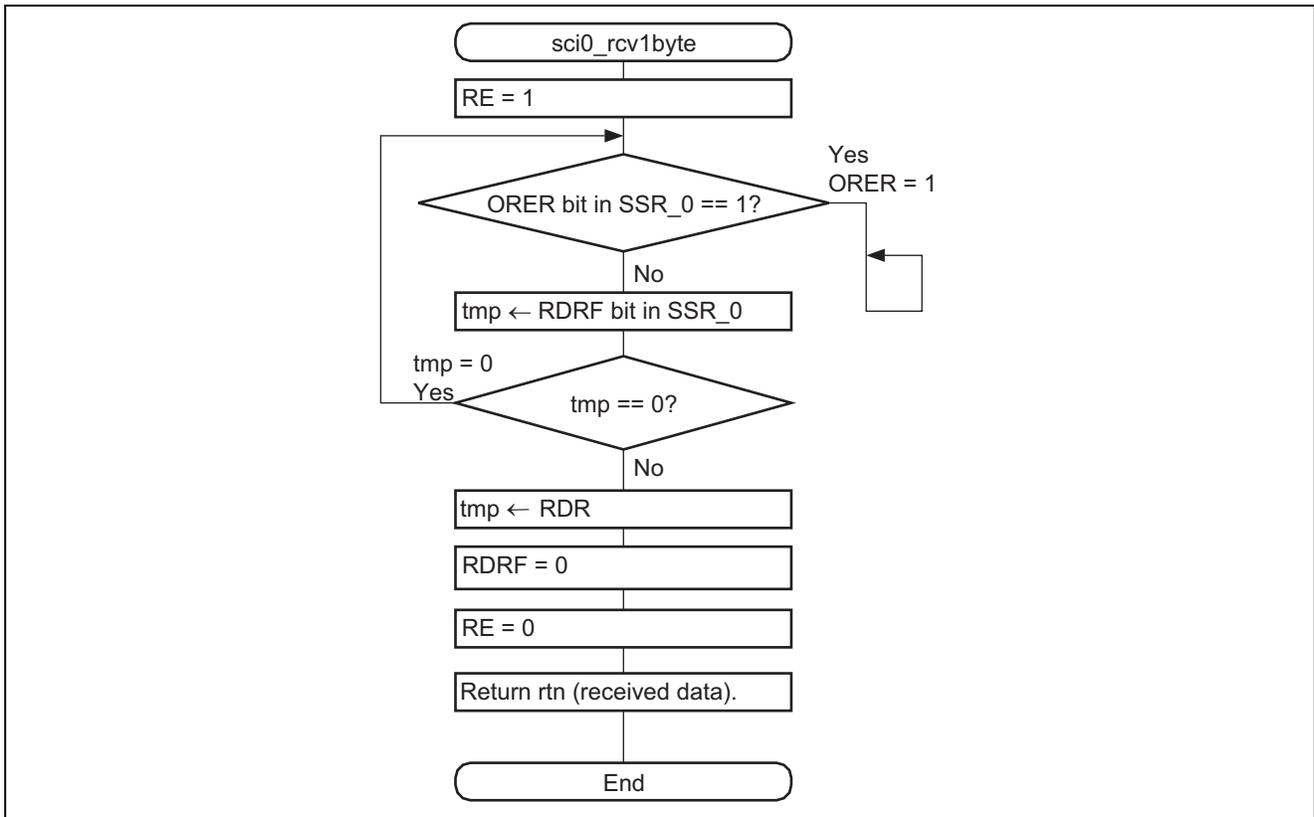
Note: * Only 0 can be written here, to clear the flags.

- Receive data register_0 (RDR_0) Number of bits: 8 Address: H'FFFF85

Function: An 8-bit register for storing receive data.

Setting: Undefined

5. Flowchart



7.2.3 sci0_rcvbyte Function

1. Functional overview

Receives n byte of clock synchronous serial data.

2. Arguments

Type	Variable Name	Description
unsigned char	dtno	No. of receive bytes
unsigned char	*ram	The start address of RAM in which the receive data is stored.

3. Return value

None

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF83

Bit	Bit Name	Setting	R/W	Description
4	RE	0	R/W	Receive Enable 0: Disables reception. 1: Enabled reception.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
6	RDRF	Undefined	R/(W)*	Receive Data Register Full 0: No receive data is stored in RDR. 1: The receive data is stored in RDR.
5	ORER	Undefined	R/(W)*	Overrun Error 0: No overrun error. 1: Overrun error occurred during receive operation.

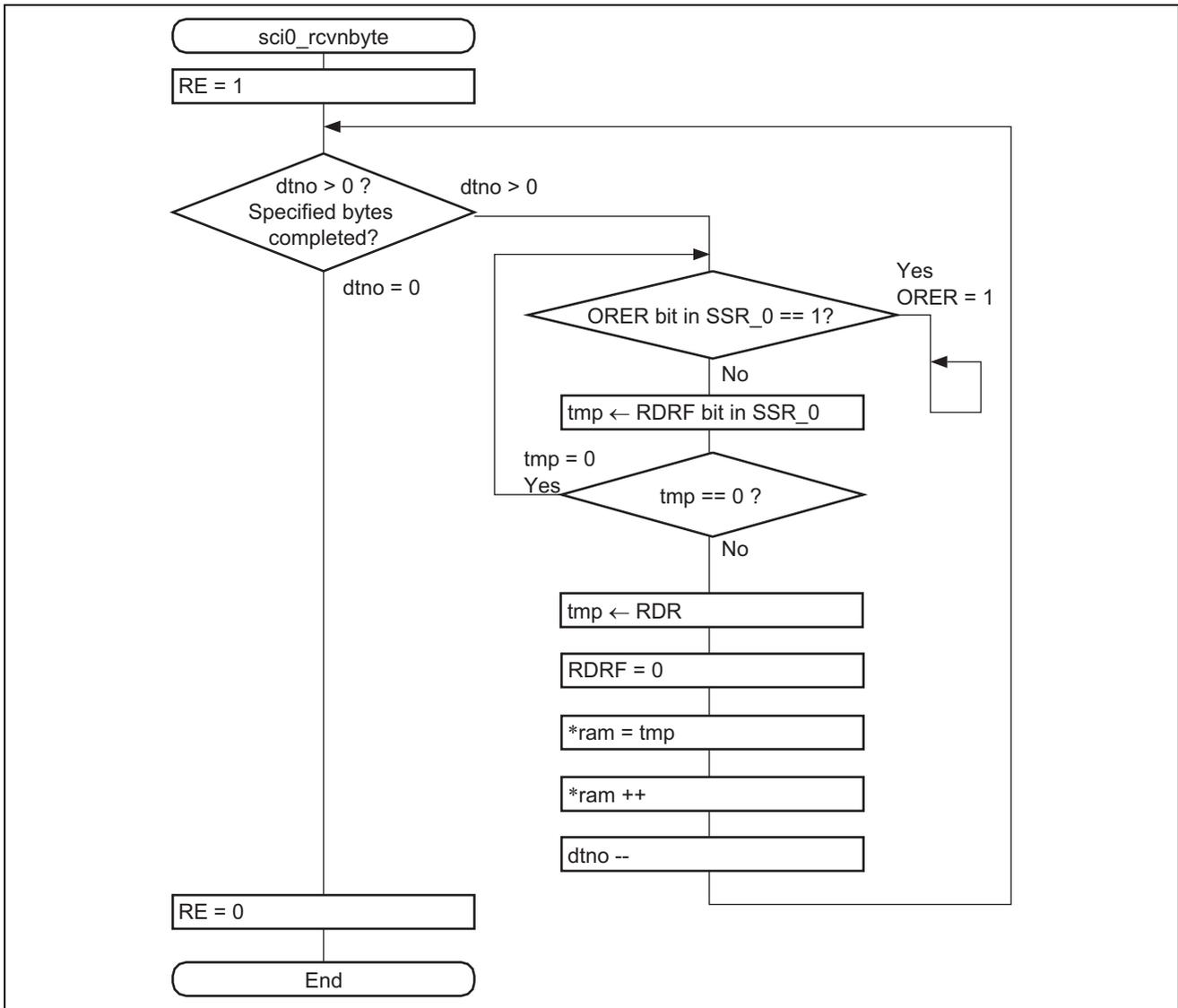
Note: * Only 0 can be written here, to clear the flags.

- Receive data register_0 (RDR_0) Number of bits: 8 Address: H'FFFF85

Function: An 8-bit register for storing receive data.

Setting: Undefined

5. Flowchart



7.2.4 sci0_trs1byte Function

1. Functional overview

Receives one byte of clock synchronous serial data.

2. Arguments

Type	Variable Name	Description
unsigned char	tdt	Transmits one byte of data

3. Return value

None

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.

- Transmit data register_0 (TDR_0) Number of bits: 8 Address: H'FFFF83

Function: An 8-bit register of storing transmit data.

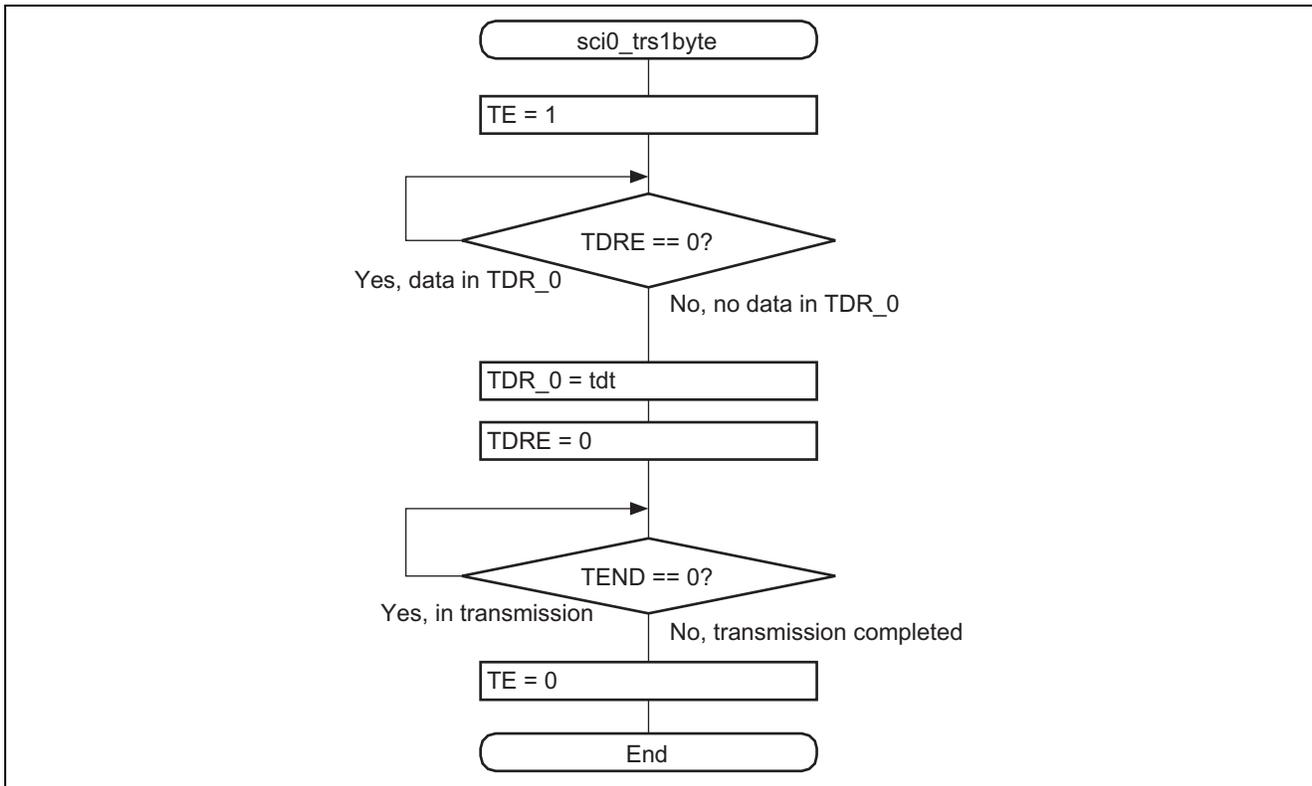
Setting: Undefined.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty 0: Transmit data written to TDR is not transferred to TSR. 1: Transmit data is not written to TDR, or transmit data written to TDR is not transferred to TSR.
2	TEND	Undefined	R	Transmit End 0: In transmission 1: Transmission completed

Note: * Only 0 can be written here, to clear the flag for TDRE.

5. Flowchart



7.2.5 sci0_trsnbyte Function

1. Functional overview

Transmits n bytes of clock synchronous serial data.

2. Arguments

Type	Variable Name	Description
unsigned short	dtno	Transmit size
unsigned char	*tdt	Start address of the transmit data

3. Return value

None

4. Internal registers used

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.

- Transmit data register_0 (TDR_0) Number of bits: 8 Address: H'FFFF83

Function: An 8-bit register of storing transmit data.

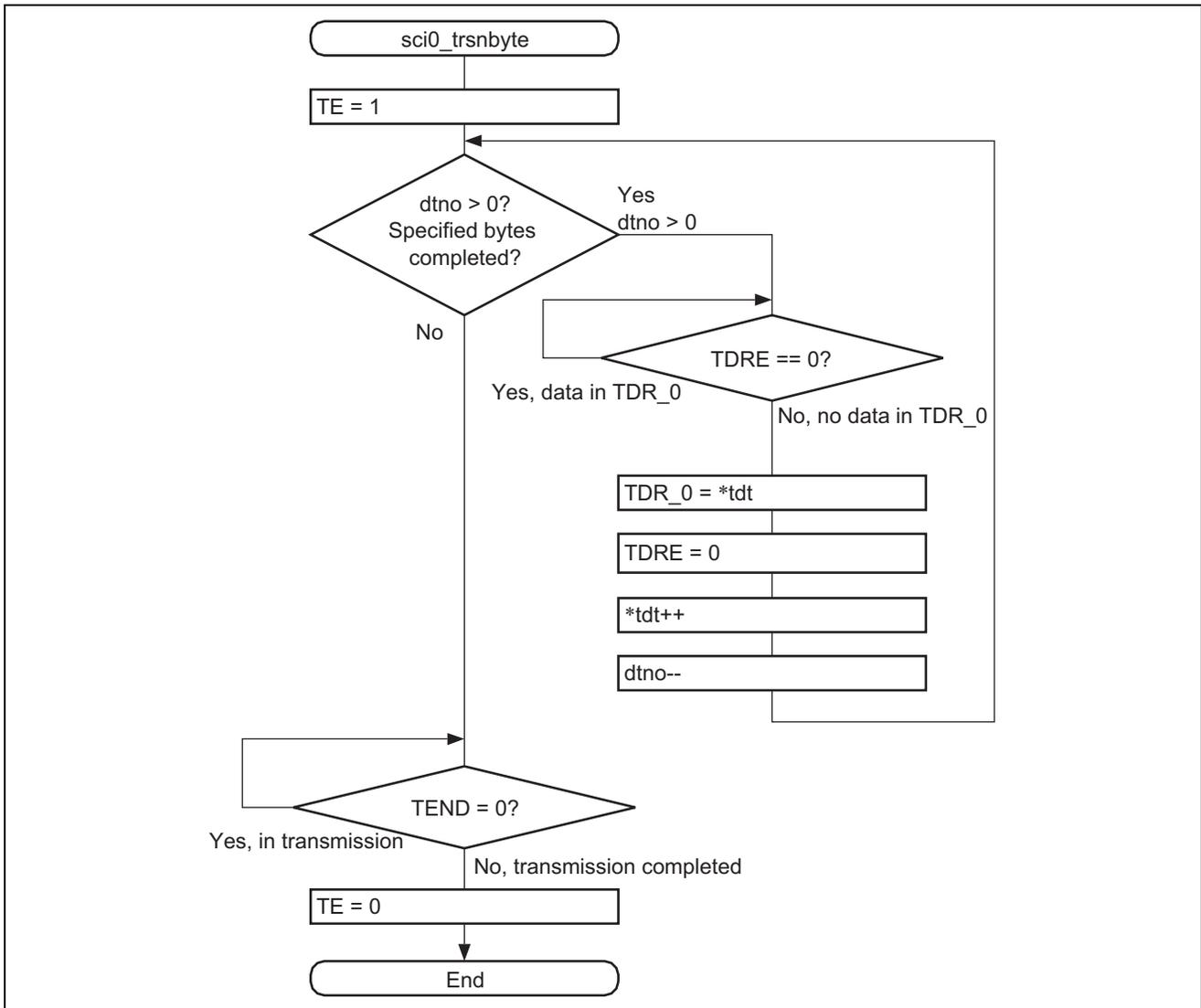
Setting: Undefined.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W) *	Transmit Data Register Empty 0: Transmit data written to TDR is not transferred to TSR. 1: Transmit data is not written to TDR, or transmit data written to TDR is not transferred to TSR.
2	TEND	Undefined	R	Transmit End 0: In transmission 1: Transmission completed

Note: * Only 0 can be written here, to clear the flag for TDRE.

5. Flowchart



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