How to use the External Loopback Clock
SLG47910

Abstract

This application shows how to connect the FPGA Board to run using an external clock source though GPIO. This application note comes complete with design files which can be found in the References section.

Contents

Terms and Definitions

FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA Window	Main FPGA project window for debug and IO programming

References

For related documents and software, please visit:

ForgeFPGA Low-density FPGAs | Renesas

Download our free ForgeFPGA™ Designer software [1] to open the. ffpga design files [2] and view the proposed circuit design.

[1] ForgeFPGA Designer Software, Software Download and User Guide, Renesas Electronics

[2] AN-FG-010 How to use External Loopback Clock.ffpga, ForgeFPGA Design File, Renesas Electronics

[3] SLG47910, Preliminary Datasheet, Renesas Electronics

1. Introduction

The SLG47910 Development board has the capability to work with 3 types of Global Clocks Trees: PLL Clock, Oscillator Clock and External Clock 0/1. This application note focuses on how to setup the ForgeFPGA Workshop software to operate on External Clock.

We will be using the example of a simple Frequency Divider to showcase the connections for External Clock. The input & output ports of the design must be assigned to the IOB Titles in the IO Planner of the ForgeFPGA Software according to Figure 1.

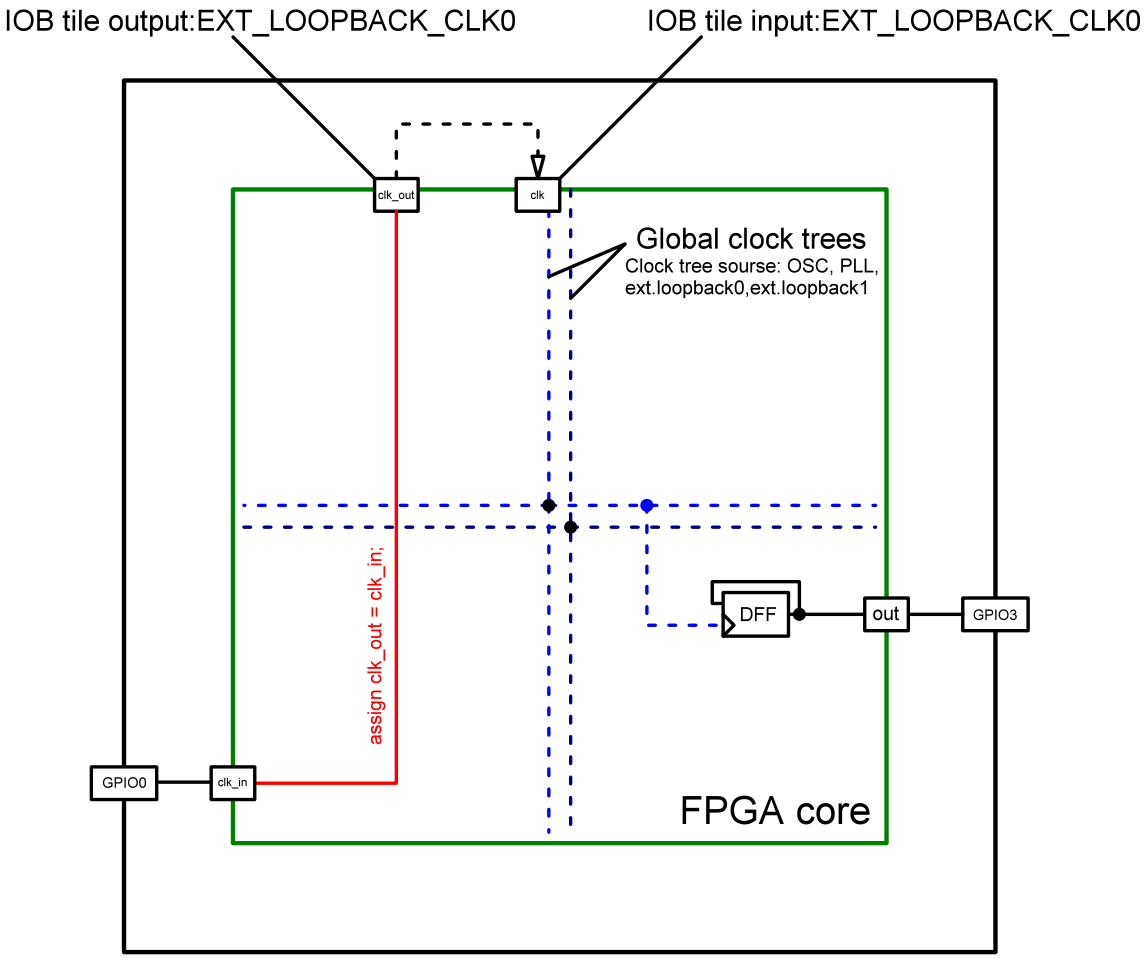

Figure 1: Clock Connections to FPGA Core

The IOB Input Tile with function as EXT_LOOPBACK_CLK0 is assigned to the main *loopback_clock* signal. On the other hand, the IOB Output Tile with function also as EXT_LOOPBACK_CLK0 is assigned to *clk_out* signal. Hence connecting the *loopback_clock* signal and *clk_out* signal internally.

2. Ingredients

- ForgeFPGA Device SLG47910
- Latest Revision of ForgeFPGA Workshop software
- SLG47910 Development Board and Adaptor Board

3. Verilog Code

Shown below is the (*top*) module called clock_loopback. It is available for download [AN-FG-010 How to use External Loopback Clock.ffpga].

```
// Example project

(* top *) module clock_loopback(
  (* iopad_external_pin, clkbuf_inhibit *) input clk,
  (* iopad_external_pin *) input nreset,
  (* iopad_external_pin *) input clk_in,//GPIO0
  (* iopad_external_pin *) output clk_in_oe,
  (* iopad_external_pin *) output clk_out,
  (* iopad_external_pin *) output out//GPIO3
);

  reg dff;
  reg nrst;

  assign clk_in_oe = 1'b1;
  assign clk_out = clk_in;
  assign out = dff;

  //Synchronize nReset
  always @(posedge clk) begin
    nrst <= nreset;
  end

  always @(posedge clk) begin
    if(!nrst)
      dff <= 1'b1;
    else
      dff <= ~dff;
  end

endmodule
```

4. Floorplan: CLB Utilization

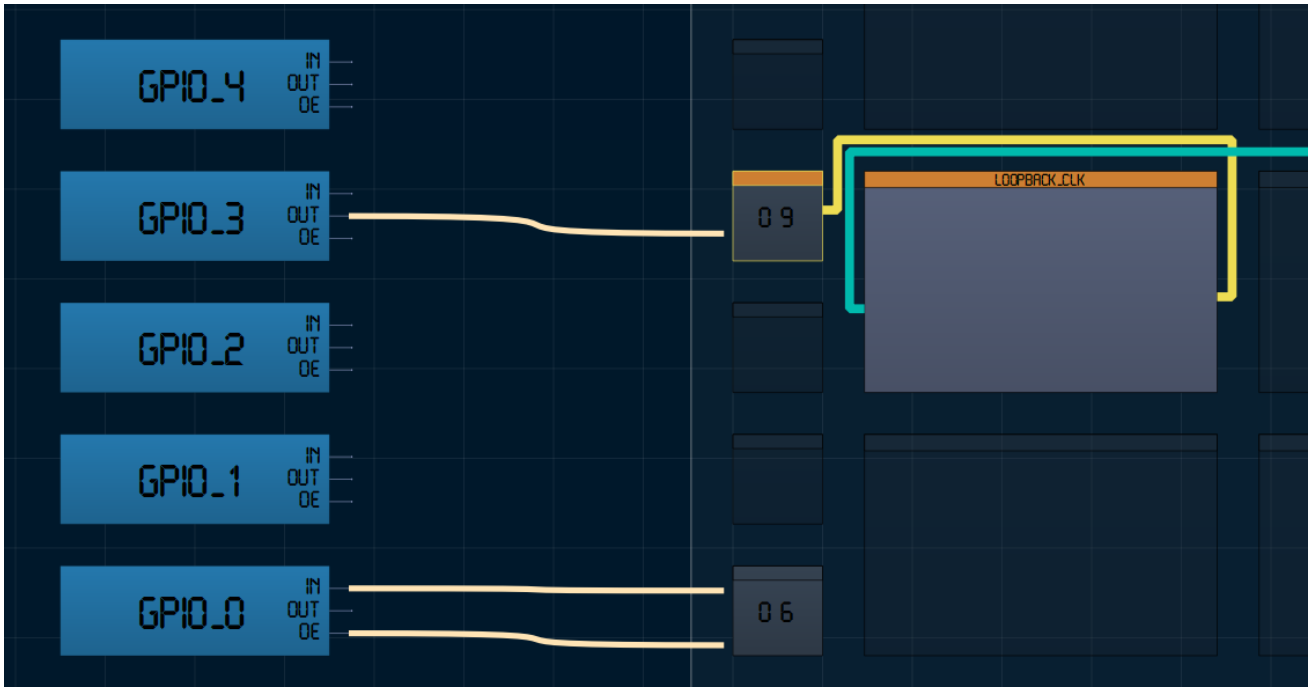

Figure 2: Floorplan & CLB Utilization

5. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47910V device and the ForgeFPGA Workshop software will load.

2. Download the design example AN-FG-010 How to use External Loopback Clock.ffpga. If you are not familiar with the ForgeFPGA Workshop software, review the Four-Bit Counter application notes that covers the basic design steps.

3. Open the AN-FG-010 How to use External Loopback Clock.ffpga file after downloading.

4. Open the FPGA editor and review the Verilog code. There is a main code with the module name clock_loopback, which is the top module defining the whole design. This is a Frequency Divider code using DFF.

5. Open the IO planner tab on the FPGA editor and review the pin assignment. The Pin assignment in the IO Planner is what makes the External Clock connection work as expected. (Figure 3)

IOB tile[0, 0] coord[31, 10] Input1	EN	
CLK tile[0, 0] clk_side=E Input0	EXT_LOOPBACK_CLK0	clk
IOB tile[0, 0] coord[31, 11] Output0	EXT_LOOPBACK_CLK0	clk_out
CLK tile[0, 0] clk_side=E Input1	EXT_LOOPBACK_CLK1	
IOB tile[0, 0] coord[31, 11] Output1	EXT_LOOPBACK_CLK1	
IOB tile[0, 0] coord[31, 10] Output0	INTERNAL_RESET	
CLK tile[0, 0] clk_side=W Input0	OSC_CLK	
CLK tile[0, 0] clk_side=W Input1	PLL_CLK	
IOB tile[0, 0] coord[31, 11] Input0	POR	nreset
IOB tile[0, 0] coord[31, 10] Input0	PWR	
IOB tile[0, 0] coord[0, 6] Input0	[PIN 13] GPIO0_IN	clk_in
IOB tile[0, 0] coord[0, 6] Output1	[PIN 13] GPIO0_OE	clk_in_oe
IOB tile[0, 0] coord[0, 6] Output0	[PIN 13] GPIO0_OUT	
IOB tile[0, 0] coord[0, 7] Input0	[PIN 14] GPIO1_IN	
IOB tile[0, 0] coord[0, 7] Output1	[PIN 14] GPIO1_OE	
IOB tile[0, 0] coord[0, 7] Output0	[PIN 14] GPIO1_OUT	
IOB tile[0, 0] coord[0, 8] Input0	[PIN 15] GPIO2_IN	
IOB tile[0, 0] coord[0, 8] Output1	[PIN 15] GPIO2_OE	
IOB tile[0, 0] coord[0, 8] Output0	[PIN 15] GPIO2_OUT	
IOB tile[0, 0] coord[0, 9] Input0	[PIN 16] GPIO3_IN	
IOB tile[0, 0] coord[0, 9] Output1	[PIN 16] GPIO3_OE	
IOB tile[0, 0] coord[0, 9] Output0	[PIN 16] GPIO3_OUT	out
IOB tile[0, 0] coord[0, 10] Input0	[PIN 17] GPIO4_IN	

Figure 3: IO Planner

6. Next select the Synthesize button on the lower left side of the FPGA editor.

7. Select the Generate Bitstream button on the lower left side of the FPGA editor. Check the Logger and Issues tabs to make sure that the bit steam was generated correctly.

8. Now click on the Floorplan tab and see the CLB utilization (Figure 2). Press the Ctrl and the mouse wheel to zoom-in. Confirm that the IOs selected in the IO Planner are shown in the floorplan.

9. Connect the Development Board and attach it to Adaptor Board with the SLG47910 part in the socket on it. Click on the Debug button on the ForgeFPGA Workshop studio and select Emulation (Figure 4).

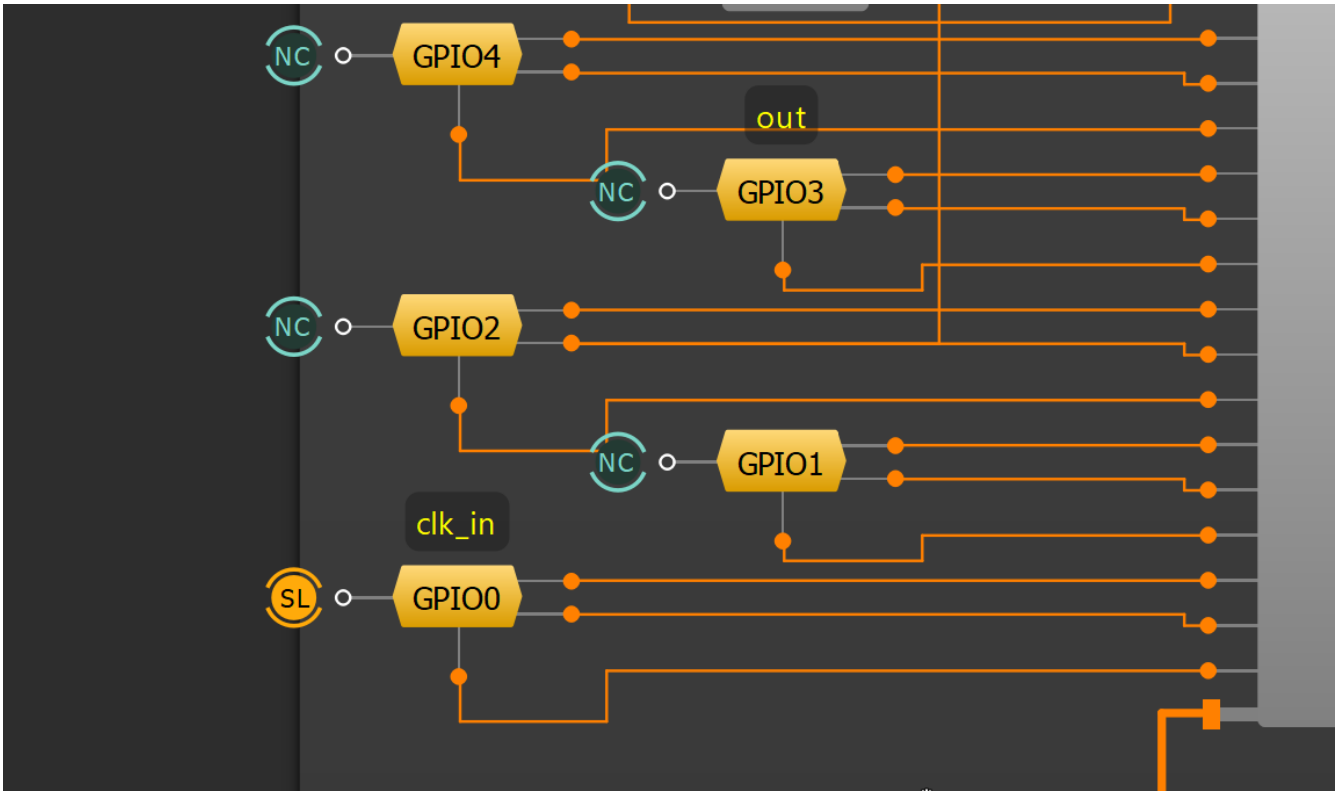

Figure 4: GPIO Connection

10. Connect the GPIO0(clk_in) to the Synchronous Logic Generator and produce 1 MHz clock frequency on it and observe the output from GPIO3 on oscilloscope (Figure 5). The input frequency will be divided by two due to flip-flop connected to the output.

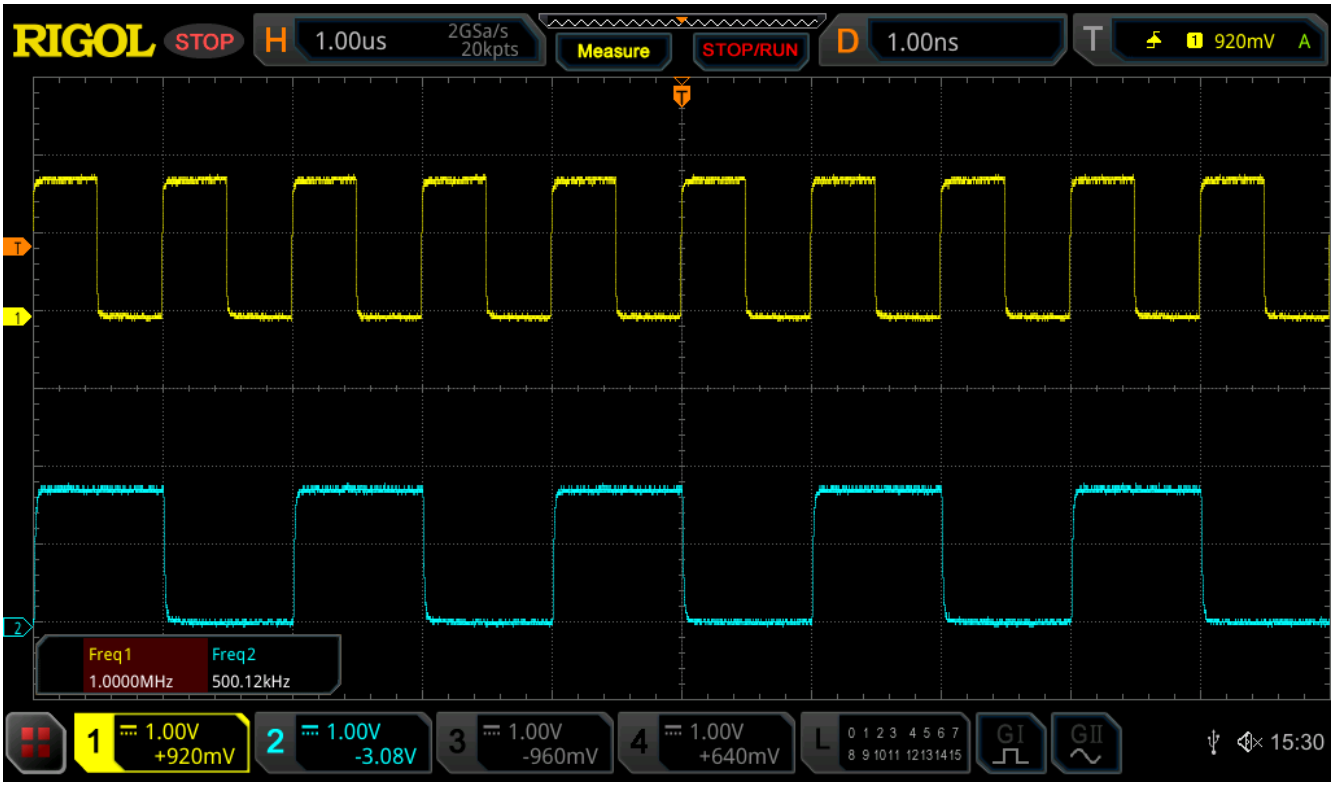

Figure 5: Waveform using External Clock

6. Conclusion

This application note shows how the Frequency Divider is designed using an External Clock and how the input-output ports are assigned in IO Planner. This procedure can be utilized for any design. This testcase is available for download (AN-FG-010 How to use External Loopback Clock.ffpga). If interested, please contact the ForgeFPGA Business Support Team.

7. Revision History

Revision	Date	Description
1.00	Jul 22, 2022	Initial release.

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