Power Sequence Example
SLG47910

This abstract shows how to use the Delay IP Block in the ForgeFPGA Software. The Delay IP Blocks are used to create a Power Sequencing Function which has three instances of Delay Blocks.

This application note comes complete with a design file which can be found in the Reference Section.

Contents

Terms and Definitions

FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure	Software Hub Main window for device selection
ForgeFPGA Window	Main FPGA project window for debug and IO programming

References

For related documents and software, please visit:

ForgeFPGA Low-density FPGAs | Renesas

Download our free ForgeFPGA™ Designer software [1] to open the .ffpga design files [2] and view the proposed circuit design.

[1] ForgeFPGA Designer Software, Software Download and User Guide

[2] AN-FG-009 Power Sequence Example.ffpga, ForgeFPGA Design File

[3] SLG47910, Preliminary Datasheet

1. Introduction

The Delay Block is a module that postpones rising and/or falling edges for the duration of the register values. The Delay IP Block has 5 inputs as seen in Figure 1.

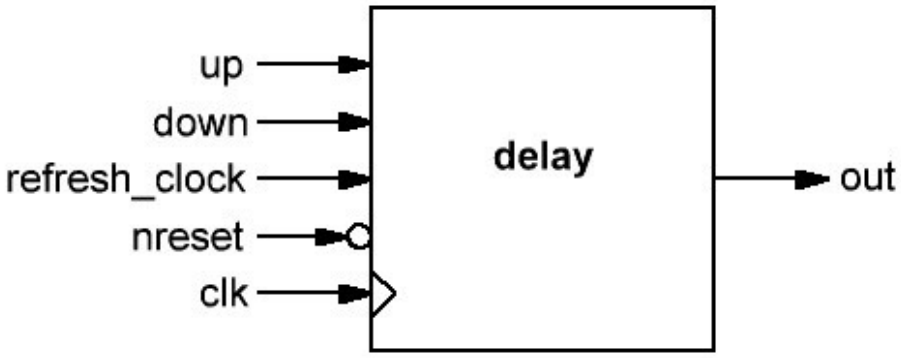

Figure 1: Delay IP Block Pin Diagram

The following signal names are the PINs that are used in the design:

- clk - input clock signal
- nreset - input negative reset signal
- refresh_clock - divide clock from the external counter
- up - input up signal
- down - input down signal (Highest Priority)
- out - output delay signal

The register value is defined by two parameters: RISING_COUNTER_DATA & FALLING_COUNTER_DATA. These two parameters define the length of the rising and falling delay period. By default, it is set to 255 in the IP Block Design. If the input signal is shorter than the delay time, it can work as filter. In Figure 2, assume that the RISING_COUNTER_DATA = FALLING_COUNTER_DATA = 2, hence we can observe that the Rising DLY1 Edge goes High after 2 clock cycles from when the UP signal goes High. Similarly, the Falling DLY1 edge goes Low after two clock cycles of the rising edge of the DOWN signal. As the DOWN signal has the highest priority, the Falling edge of the DOWN signal triggers a Rising DLY1 edge again on the OUT signal.

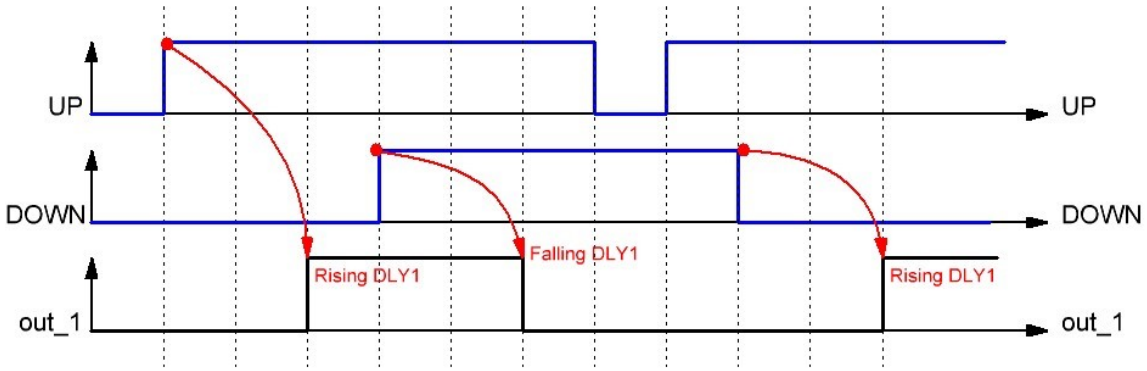

Figure 2: Delay IP Block Functionality Waveform

This application note is focused on designing a Power Sequencing Function which has 3 Delay IP Block instances (see Figure 3). We can see that the output of each Delay Block becomes a control signal for the other Delay Blocks. Figure 4 shows the output waveform functionality of the Power Sequencing where each Rising and Falling Edge of the Output Signal depends on the RISING_COUNTER_DATA & FALLING_COUNTER_DATA parameter value specified in each Delay Block Instance.

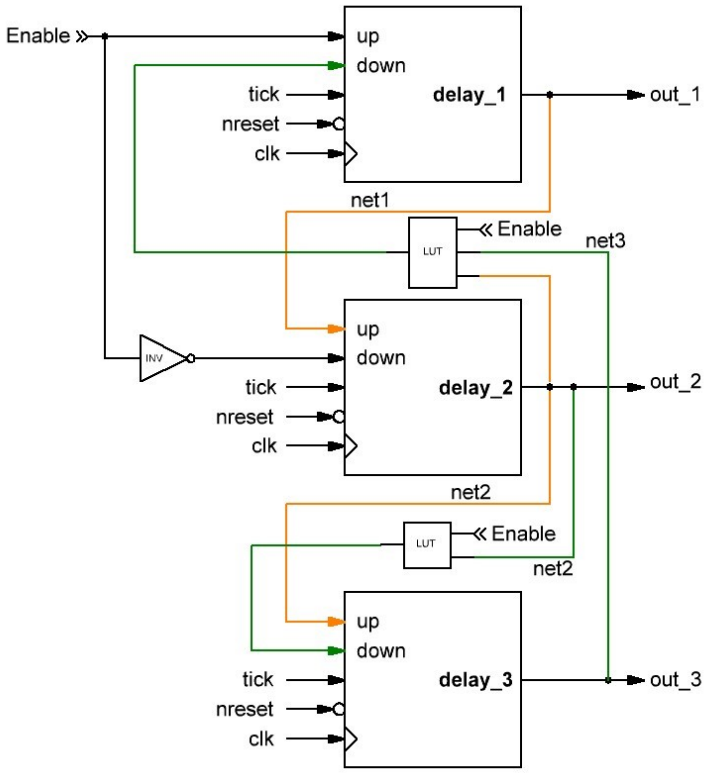

Figure 3: Power Sequencing Block Diagram

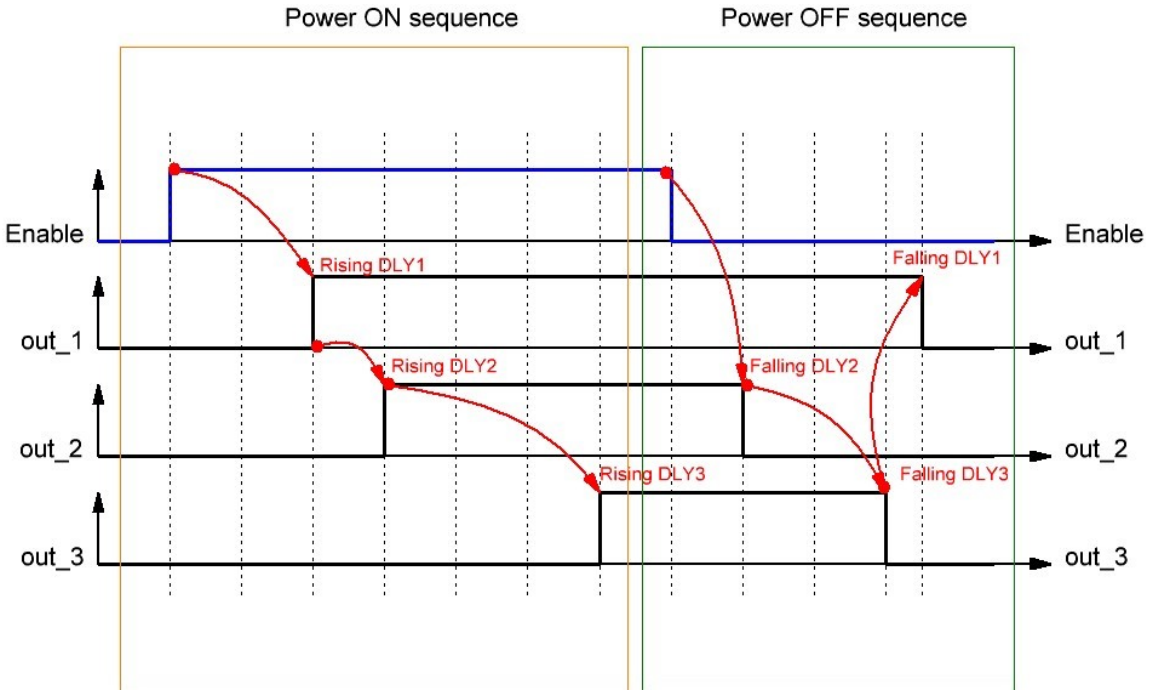

Figure 4: Power Sequencing Output Waveform

Using the ForgeFPGA Designer Software, the Verilog code was synthesized and the Bitstream was loaded on the SLG47910 device.

2. Ingredients

- ForgeFPGA Device SLG47910V
- Latest Revision of ForgeFPGA Workshop software
- GTKWave software (inbuilt in ForgeFPGA Designer Software)

3. Delay Verilog Code

Shown below is the (*top*) module called Delay_top. It is available for download (AN-FG-009 Power Sequence Example.ffpga).

```
(* top *) module delay_top #(
parameter WIDTH = 8
)(
// Main inputs
(* iopad_external_pin, clkbuf_inhibit *) input clk,
(* iopad_external_pin *) input nreset,
(* iopad_external_pin *) input enable,
(* iopad_external_pin *) output enable_oe,
(* iopad_external_pin *) output out_1,
(* iopad_external_pin *) output out_2,
(* iopad_external_pin *) output out_3,
(* iopad_external_pin *) output OSC_CTRL_MODE,
(* iopad_external_pin *) output OSC_CTRL_EN
);

assign OSC_CTRL_MODE = 1'b0;
assign OSC_CTRL_EN = 1'b1;
assign enable_oe = 1'b1;
reg [7:0] counter;
wire tick;
wire net1;
wire net2;
wire net3;
// refresh clock
always @(posedge clk) begin
```

```
if (!nreset)
counter <= 'b0;
else if ( counter == 10)
counter <= 'b0;
else
counter <= counter + 1;
end
assign tick = (counter == 10)? 1'b1 : 1'b0;
delay_1 #(
.RISING_COUNTER_DATA (4),
.FALLING_COUNTER_DATA (3),
.WIDTH (WIDTH)
) delay_1_wrapper(
.clk (clk),
.up (enable),
.down (~net3 & ~net2 & ~enable),
.nreset (nreset),
.refresh_clock (tick),
.out (net1)
);
delay_1 #(
.RISING_COUNTER_DATA (5),
.FALLING_COUNTER_DATA (5),
.WIDTH (WIDTH)
) delay_2_wrapper(
.clk (clk),
.up (net1),
.down (~enable),
.nreset (nreset),
.refresh_clock (tick),
.out (net2)
);
delay_1 #(
.RISING_COUNTER_DATA (21),
.FALLING_COUNTER_DATA (15),
.WIDTH (WIDTH)
) delay_3_wrapper(
```

```
.clk (clk),
.up (net2 & enable),
.down (~net2 & ~enable),
.nreset (nreset),
.refresh_clock (tick),
.out (net3)
);
assign out_1 = net1;
assign out_2 = net2;
assign out_3 = net3;
endmodule
```

4. Floorplan: CLB Utilization

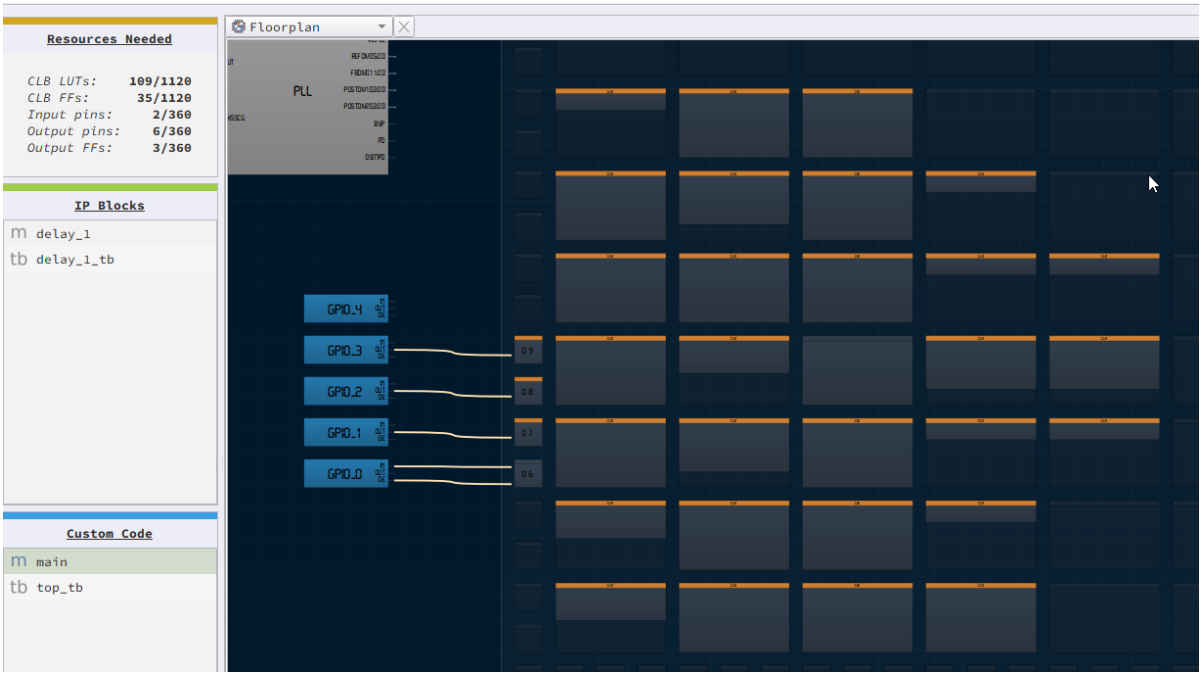

Figure 5: CLB Utilization

The Floorplanner tab in the FPGA Editor shows the placement of CLBs and FFs (Figure 3). The resource utilization is shown in the top left corner

5. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47910V device and the ForgeFPGA Workshop software will load.
2. Download the design example Power Sequence Example.ffpga. If you are not familiar with the ForgeFPGA Workshop software, review the Four-Bit Counter application notes that covers the basic design steps.

3. Open the Power Sequence Example.ffpga file after downloading.
4. Open the FPGA editor and review the Verilog code and the testbench code. There is a main code with the module name Delay_top which is the top module defining the whole design. This code has 3 instances for Delay Block mapped.
5. Open the IO planner tab on the FPGA editor and review the pin assignment.
6. Next select the Synthesize button on the lower left side of the FPGA editor.
7. Select the Generate Bitstream button on the lower left side of the FPGA editor. Check the Logger and Issues tabs to make sure that the bit steam was generated correctly.
8. Now click on the Floorplan tab and see the CLB utilization (Figure 5). Press the Ctrl and the mouse wheel to zoom-in. Confirm that the IOs selected in the IO Planner are shown in the floorplan.
9. Now click on the Simulate Testbench button on the top and select top_tb to simulate the testbench for the complete design. The GTKWave will automatically open if there are no Syntax errors in the testbench. Check logger for errors.
10. In the GTKWave software, select the signals you want to view and Click Insert on the left corner to insert the signals in the wave window. Once the desired signals are selected, click on Reload (Figure 4).
11. You can observe the countdown in the waveform displayed in the GTKWave software.

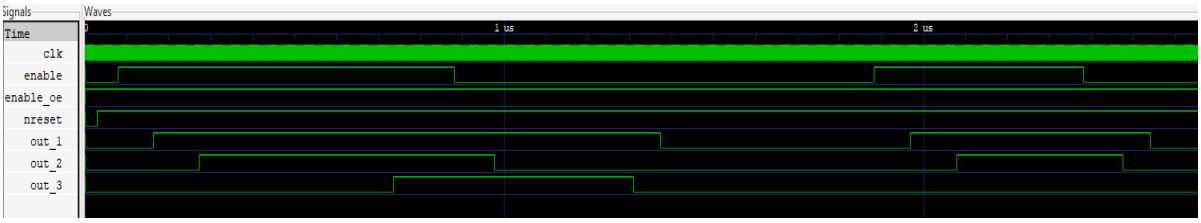

Figure 6: GTWave Simulation Results

12. This Delay IP Block is also inbuilt in the ForgeFPGA Software and can be launched by clicking the "Add Block" Button on the top left corner of the FPGA Editor. That will open a list of inbuilt IP Blocks we have in the software. User can then select the Delay Block under the "Data Pipelining" option by typing it in the search bar (see Figure 7).

13. After selecting the desired Block, the window then displays the basic information of the Block such as the Schematic, the Resource Estimation and the Parameters which can be edited, and the desired value can be added. After the desired value has been entered, Click Select and this will open the Verilog Code for Delay Block as well as its TestBench.

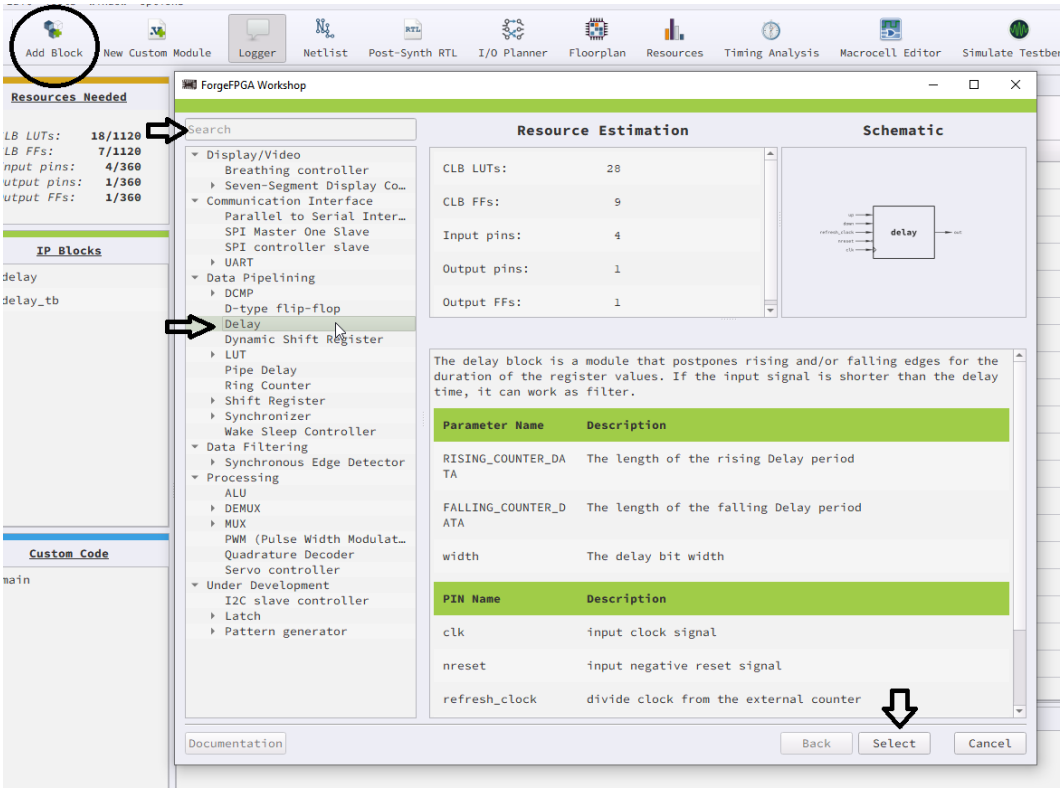

Figure 7: How to add Delay IP Block

6. Conclusions

The application note shows how the Delay IP Block is design and how it can be used to delay the Rising and Falling edge of the input with the help of different Register Values. This testcase is available for download (AN-FG-009 Power Sequence Example.ffpga). If interested, please contact the ForgeFPGA Business Support Team.

7. Revision History

Revision	Date	Description
1.0	26-Apr-2022	Initial Version

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