Macro Cell Mode
SLG47910V

Abstract

This application shows how to create the Verilog Code automatically using the Macro Cell Editor in the software. The Macro cell feature will let you assemble and configure your design graphically using a library of numerous Blocks ranging from different Logic Gates, Sequential Logic Blocks, in-built IP Blocks.

This application note comes complete with design files which can be found in the References section

Contents

1. Terms and Definitions

CLB	Configuration Logic Block
HDL	Editor Workspace where Verilog code is entered
FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA	Window Main FPGA project window for debug and IO programming

2. References

For related documents and software, please visit: https://www.dialog-semiconductor.com/products/greenpak/low-power-low-cost-forgefpga . Download our free ForgeFPGA™ Designer software [1] to open the .ffpga design files [2] and view the proposed circuit design.

[1] ForgeFPGA Designer Software, Software Download and User Guide

[2] AN-FG-003 Macro Cell Mode, ForgeFPGA Design File, Renesas Electronics

[3] SLG47910, Preliminary Datasheet, Renesas Electronics

3. Introduction

The Marco Cell Mode works on the same lines as the GreenPAK software. This feature will let you assemble and configure your design graphically using a library of numerous Blocks ranging from different Logic Gates, Sequential Logic Blocks, in-built IP Blocks. You'll be able to generate the Verilog Code using the schematics that you create with the Macro Cell tool and use it in our toolchain.

This tool allows you to take advantage of the flexibility of FPGAs even without knowledge of Verilog Code.

4. Ingredients

- Latest Revision of ForgeFPGA Workshop software

5. Verilog Code

Shown below is the (*top*) module called **macrocellmode_autogen**. The Verilog code displays how to connect different modules under one top module using synchronous style of Verilog coding.

```
module mcm_AND_2(output Y, input A, B);
  and(Y, A, B);
endmodule

module mcm_XOR_2(output Y, input A, B);
  xor (Y, A, B);
endmodule

module mcm_NAND_2(output Y, input A, B);
  wire Yd;
  and(Yd, A, B);
  not(Y, Yd);
endmodule

module mcm_NOT(output Y, input A);
  not (Y, A);
endmodule

(* top *) module macrocellmode_autogen (
  (* iopad_external_pin, clkbuf_inhibit *) input clock,

  (* iopad_external_pin *) input A_in,

  (* iopad_external_pin *) output Y_out
);

  wire wire59;
  wire wire66;
  wire wire82;
  wire wire38;
  wire wire74;
  wire wire46;
  wire wire42;


  assign wire46 = 1'b1;
  assign wire38 = clock;
  assign wire42 = A_in;
  assign Y_out = wire82;


  mcm_NOT not57(wire59, wire46);
```

```
mcm_AND_2 and63(wire66, wire38, wire42);
mcm_NAND_2 nand71(wire74, wire66, wire59);
mcm_XOR_2 xor79(wire82, wire66, wire74);

endmodule
```

6. Design Steps

1. Open the ForgeFPGA Workshop software in GreenPAK and select the SLG47910 device From the ForgeFPGA tool bar, select the FPGA Editor Tab (see Figure 1).

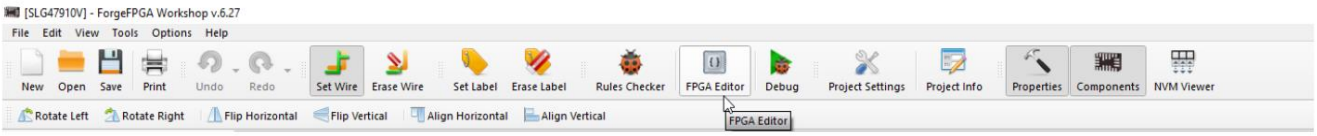

Figure 1: ForgeFPGA Tool Bar

2. Launch the Macro Cell Editor Window from the toolbar on the top.

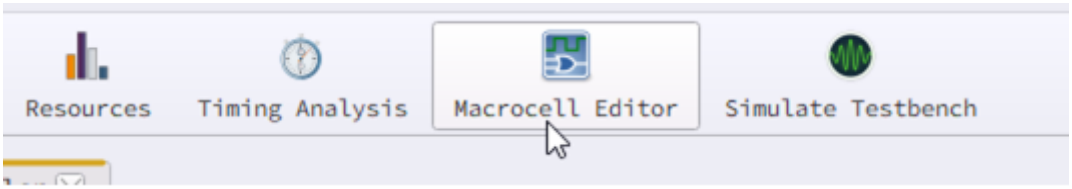

Figure 2 : Macrocell Editor Icon

3. In the Macrocell Editor Window, create the design of your choice by dragging and drooping the blocks from the library on the right side of the window and connecting the ports through the wires.

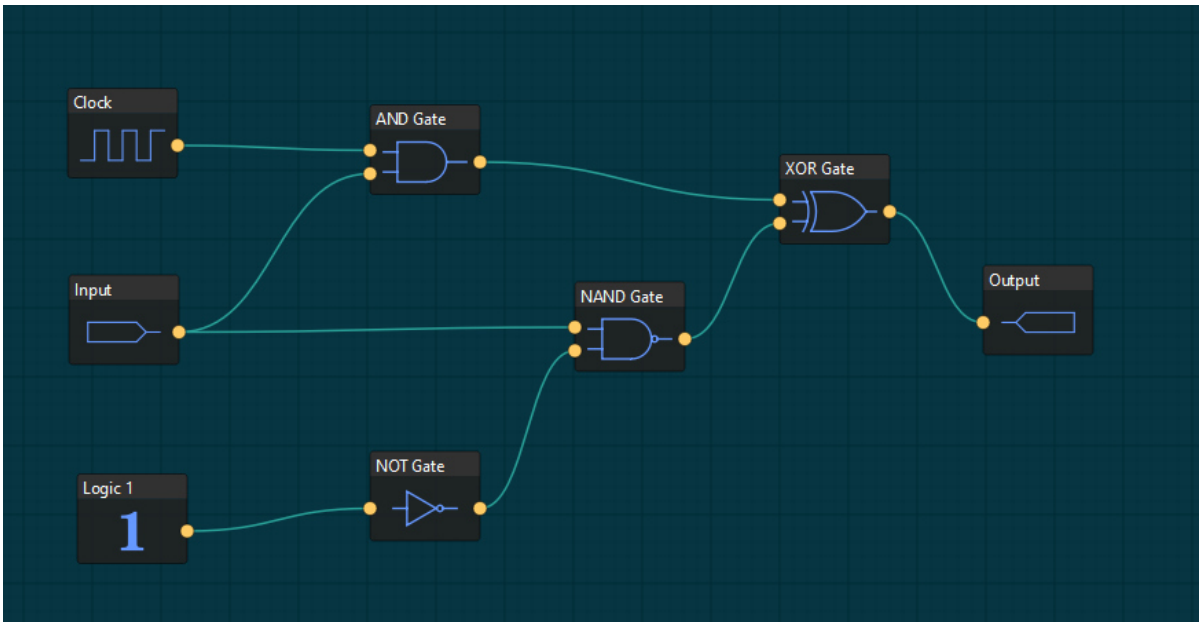

Figure 3: Steps to Launch Custom Module

4. User can also rename the blocks by double-clicking the blocks and typing in the names of their choice.

5. After the user has created the desired design, click on the Generate Verilog button on the right to automatically generate the Verilog code for the design created in Macro Cell Editor(See Figure 3)

6. User can save the Verilog code automatically created or edit it as per the need. The user can then Synthesize the design and create a testbench to check the functionality of the design.

7. Conclusion

This Application Note outlines how to create a design in the macrocell mode and how to create its Verilog code automatically. The library contents in the Macro Cell editor will be expanding in the future to help the user to create more designs. If interested, please contact ForgeFPGA Business Support Team.

8. Revision History

Revision	Date	Description
1.00	Dec 10, 2021	Initial release.
2.0	Feb 20, 2024	Revised according to BB revision

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