Macro Cell Mode
SLG47910

This application shows how to create the Verilog Code automatically using the Macro Cell Editor in the software. The Macro cell feature will let you assemble and configure your design graphically using a library of numerous Blocks ranging from different Logic Gates, Sequential Logic Blocks, in-built IP Blocks.

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Terms and Definitions

CLB	Configuration Logic Block
HDL Editor	Workspace where Verilog code is entered
FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA Window	Main FPGA project window for debug and IO programming

References

For related documents and software, please visit:

ForgeFPGA Low-density FPGAs | Renesas

Download our free ForgeFPGA™ Designer software [1] to open the .ffpga design files [1] and view the proposed circuit design.

[1] ForgeFPGA Designer Software, Software Download and User Guide, Renesas Electronics

[2] AN-FG-004 Macro Cell Mode.ffpga, ForgeFPGA Design File, Renesas Electronics

[3] SLG47910, Preliminary Datasheet, Renesas Electronics

1. Introduction

The Marco Cell Mode works on the same lines as the GreenPAK software. This feature will let you assemble and configure your design graphically using a library of numerous Blocks ranging from different Logic Gates, Sequential Logic Blocks, in-built IP Blocks. You'll be able to generate the Verilog Code using the schematics that you create with the Macro Cell tool and use it in our toolchain.

This tool allows you to take advantage of the flexibility of FPGAs even without knowledge of Verilog Code.

2. Ingredients

Latest ForgeFPGA Workshop Software

3. Macro Cell Editor

We can create the needed schematic in the Macro Cell Editor window as per our design requirement.

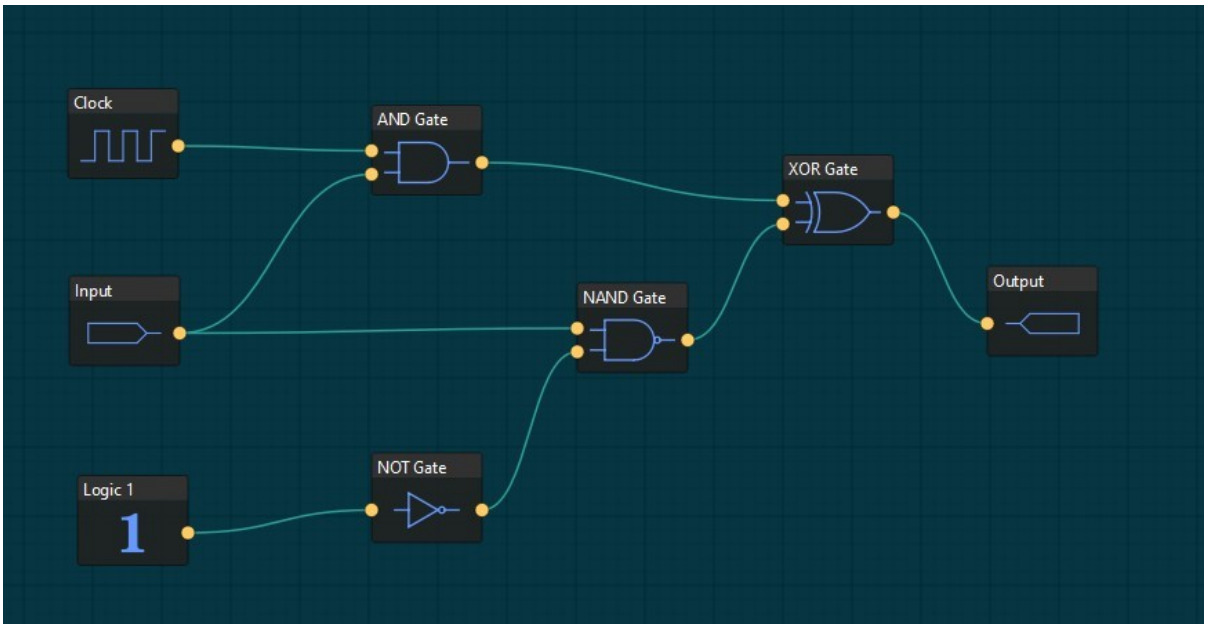

Figure 1: System Diagram

4. Verilog Code

This Verilog code was generated automatically after the creation of the design in the Macrocell Editor

```
// module for XOR Gate
module mcm_XOR_2(output Y, input A, B);
  xor (Y, A, B);
endmodule
// Module for NAND Gate
module mcm_NAND_2(output Y, input A, B);
  wire Yd;
  and(Yd, A, B);
  not(Y, Yd);
endmodule
// Module for NOT Gate
module mcm_NOT(output Y, input A);
  not (Y, A);
endmodule
// Module for AND Gate
module mcm_AND_2(output Y, input A, B);
  and(Y, A, B);
endmodule
// Top module - connections between all modules
(* top *) module macrocellmode_autogen (
  (* iopad_external_pin, clkbuf_inhibit *) input clock35,
  (* iopad_external_pin *) input input18,
  (* iopad_external_pin *) output output29
);
// wires connecting the modules
  wire wire40; wire wire57;
  wire wire24; wire wire28;
  wire wire48; wire wire36;
  wire wire19;
// assigning values for input & Output
  assign wire57 = 1'b1;
  assign wire36 = clock35;
  assign wire19 = input18;
  assign wire48 = output29;
// port mapping different modules
  mcm_NOT not22(wire24, wire57);
  mcm_NAND_2 nand25(wire28, wire19, wire24);
  mcm_AND_2 and37(wire40, wire36, wire19);
  mcm_XOR_2 xor45(wire48, wire40, wire28);
endmodule
```

Figure 2: Verilog Code

5. Design Steps

1. Open the ForgeFPGA Workshop software in GreenPAK and select the SLG47910 device.
2. From the ForgeFPGA tool bar, select the FPGA Editor Tab (see Figure 3).

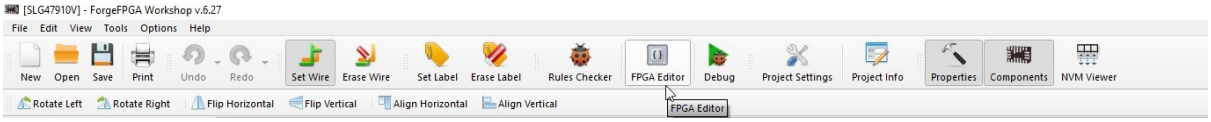

Figure 3: ForgeFPGA Tool Bar

3. Launch the Marco Cell Editor Window from the toolbar on the top of ForgeFPGA Workshop software (see Figure 4).

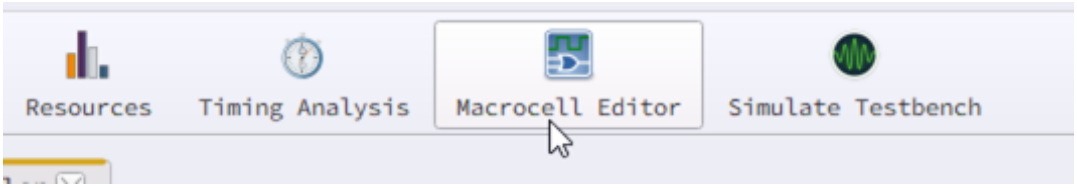

Figure 4: Macrocell Editor Icon

4. In the Macrocell Editor window, Create the design of your choice by dragging and dropping the blocks from the library on the right and connecting the ports of the blocks through wires.

5. After you are satisfied with your design, click on the Generate Verilog button on the right to generate the Verilog Code for the design you just created (see Figure 5).

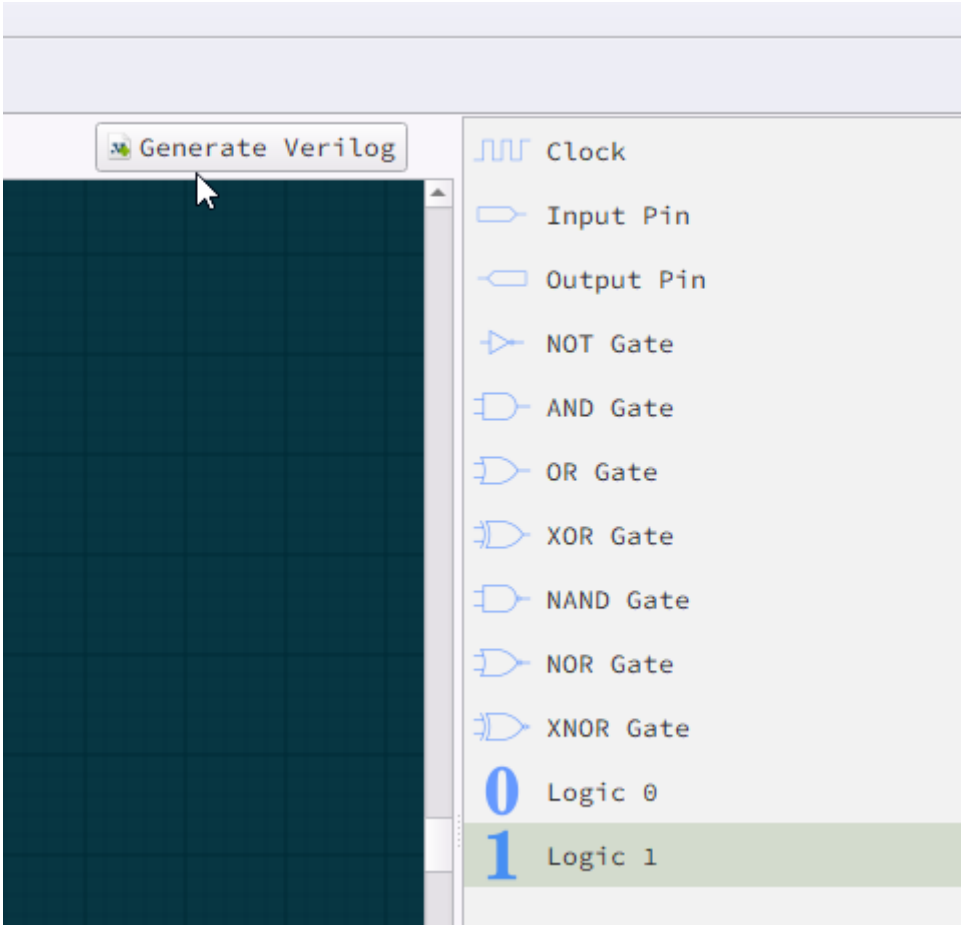

Figure 5: Generate Verilog Code from MacroCell Design

6. This will create another tab in the software called mcm_generated. This Verilog code corresponds to the design you created in Step 5. Verify that the topmost module is the just created.

7. Once satisfied with the code generated, save the code using the save button in the top left corner of the FPGA Editor.

8. The design is now ready to be Synthesized, BitStream Generation.

9. Create a Testbench Code to verify the working of the design and simulate it using the in-built GTKWave software.

6. Conclusion

The procedure outlines in this application example can be applied to any design you can create in the marcocell mode and then generate its equivalent Verilog Code. This testcase is available for download. If interested, please contact the ForgeFPGA Business Support Team.

7. Revision History

Revision	Date	Description
1.00	Mar 3, 2022	Initial release.

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