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Application Note

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F-ZTAT™ Microcomputer On-Board Programming

Application Note

Renesas F-ZTAT™ Microcomputer

Renesas Electronics
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Rev.2.00 2004.12

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General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Address

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these address. Do not access these registers; the system's operation is not guaranteed if they are accessed.

Preface

This Application Note describes on-board programming of F-ZTAT™* microcomputers (H8/538F, H8/3434F, H8/3334YF, H8/3048F) which have on-chip flash memory that can be programmed after mounting on the board, and also on-board programming tools. It has been prepared as a reference guide to on-board programming for users engaged in system design.

The circuits in this Application Note are included to illustrate examples of on-board programming, and their contents are not guaranteed. Be sure to check the operation of any circuits before actual use.

Note: * F-ZTAT is a trademark of Renesas Technology Corp.

Organization of F-ZTAT Microcomputer On-Board Programming Application Note

Section 1 F-ZTAT Microcomputer Overview

- Introduces the complete range of F-ZTAT microcomputer products and outlines their features.
- Describes the two on-board programming modes (boot mode and user program mode).

Section 2 On-Board Programming Tools

- Describes the control aspects of Renesas' tools for facilitating on-board programming: the adapter board (providing hardware support during on-board programming), and PC interface software (providing software support during on-board programming).

Section 3 Examples of Use with User Machine

- Describes the type of circuitry required in the user machine to conduct on-board programming/erasure for an F-ZTAT microcomputer using Renesas' on-board programming tools (adapter board and PC interface software).

Section 4 On-Board Programming Methods

- Describes the requirements for F-ZTAT microcomputer programming/erasure using Renesas' on-board programming tools, and the operating procedure in each on-board programming mode.

Main Revisions for this Edition

Item	Page	Revisions (See Manual for Details)
All	—	All references to Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names changed to Renesas Technology Corp. Designation for categories changed from “series” to “group”

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Section 1 F-ZTAT Microcomputer Overview

Section 2 On-Board Programming Tools

Section 3 Examples of Use with User Machine

Section 4 On-Board Programming Methods

Tables

Section 1 F-ZTAT Microcomputer Overview

1.1 F-ZTAT Microcomputer Product Introduction

The F-ZTAT is a single-chip microcomputer with a built-in flash memory, on-board programming, and erasure capability.

Since the F-ZTAT microcomputer allows on-board programming, you can set the optimum parameters for every piece of equipment in which it is installed. The device also lets you take advantage of software upgrades after the product is shipped, making maintenance easier.

There are two on-board programming modes (boot mode and user program mode) that can be set according to conditions (see section 1.2, On-Board Programming Modes). Programming and erasure are possible even with a general purpose PROM writer.

F-ZTAT microcomputers are available in the H8/500 Series (H8/538F), H8/300 Series (H8/3434F, H8/3334YF), and H8/300H Series (H8/3048F). Features of the F-ZTAT microcomputers are shown in table 1.1.

Note: F-ZTAT is a trademark of Renesas Technology Corp.

Table 1.1 F-ZTAT Microcomputer Features

Item	Product		
	H8/538F	**H8/3334YF, H8/3434F**	**H8/3048F**
CPU	H8/500 CPU	H8/300 CPU	H8/300H CPU
Max. operating frequency	• 16 MHz (5 V) • 10 MHz (3 V)	• 16 MHz (5 V) • 10 MHz (3 V)	• 16 MHz (5 V) • 10 MHz (3 V)
Flash memory capacity (kbyte)	60	32	128
Flash memory erase block partitions (blocks)	15	12	16
Programming cycles	100 cycles guaranteed		
Program/erase voltage	Vpp = 12 V ± 0.6 V		
Programming time	50 µs/byte (typ.)		
Erase time	1 s (typ.)		
Program/erase method	• CPU control method (software control method) • PROM writer programming		

1.2 On-Board Programming Modes

There are two on-board programming modes: boot mode for batch programming/erasure, and a user program mode that allows presetting of block areas for programming and erasure.

User program mode parameters that require frequent rewriting during program development can be rewritten in real-time while tuning (flash memory emulation by RAM).

For more information about on-board programming modes, see the hardware manual for each F-ZTAT microcomputer device (on-board programming modes).

1.2.1 Boot Mode

Boot mode activates the boot program built into the F-ZTAT microcomputer to program and erase application programs in the on-chip flash memory.

The user sets up the application and programming control program (for controlling flash memory reprogramming) in the transfer source. The F-ZTAT microcomputer uses an on-chip serial communication interface (SCI) (channel 1, start-stop sync mode) to send the program from the transfer source.

The three steps below correspond to figure 1.1 to give an overview of the boot mode.

1. First, reset the F-ZTAT microcomputer.

2. Apply 12 V to the Vpp pin and mode pin, and start the boot program by canceling reset. The boot program transfers the write control program received from the transfer source to the F-ZTAT microcomputer's on-chip RAM. All areas of the on-chip flash memory are then erased. The H8/3434F and H8/3334YF boot program transfers the write control program to RAM after erasure of all areas of flash memory.

3. After erasure, there is a branch from the boot program to the write control program that was transferred to the F-ZTAT microcomputer's on-chip RAM, and the application program received from the transfer source is written to flash memory.

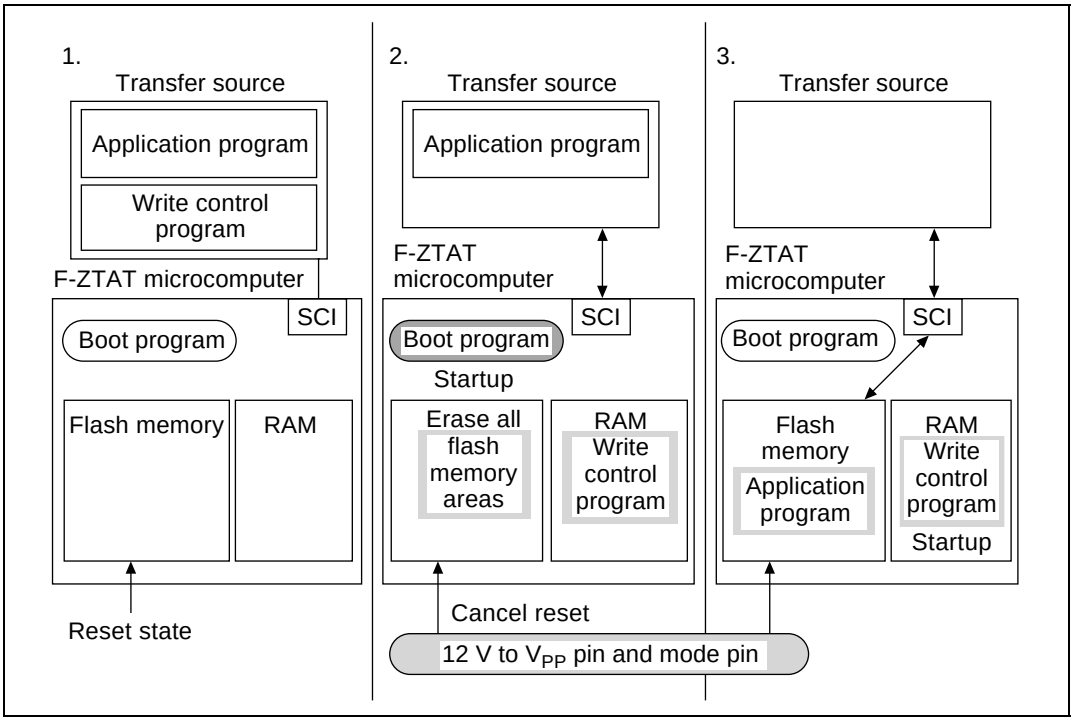


Figure 1.1 Boot Mode Overview

1.2.2 User Program Mode

In user program mode, the program/erase control program transferred in advance to the F-ZTAT microcomputer's flash memory, and the program that transfers this program to RAM (RAM transfer program) are written in boot mode or PROM mode. Figure 1.2 shows an overview of user program mode.

Transfer of an application from the transfer source using a Renesas on-board programming tool is via the F-ZTAT microcomputer's built-in SCI (channel 1, start-stop sync mode).

The three steps below correspond to figure 1.2 to give an overview of the user program mode.

1. First, reset the F-ZTAT microcomputer.

2. Apply 12 V to the Vpp pin and start the RAM transfer program by canceling reset. The program/erase program is transferred to RAM (on-chip or external) and started up.

3. The program/erase control program erases block areas specified by the user, and writes the application program received from the transfer source to that area.

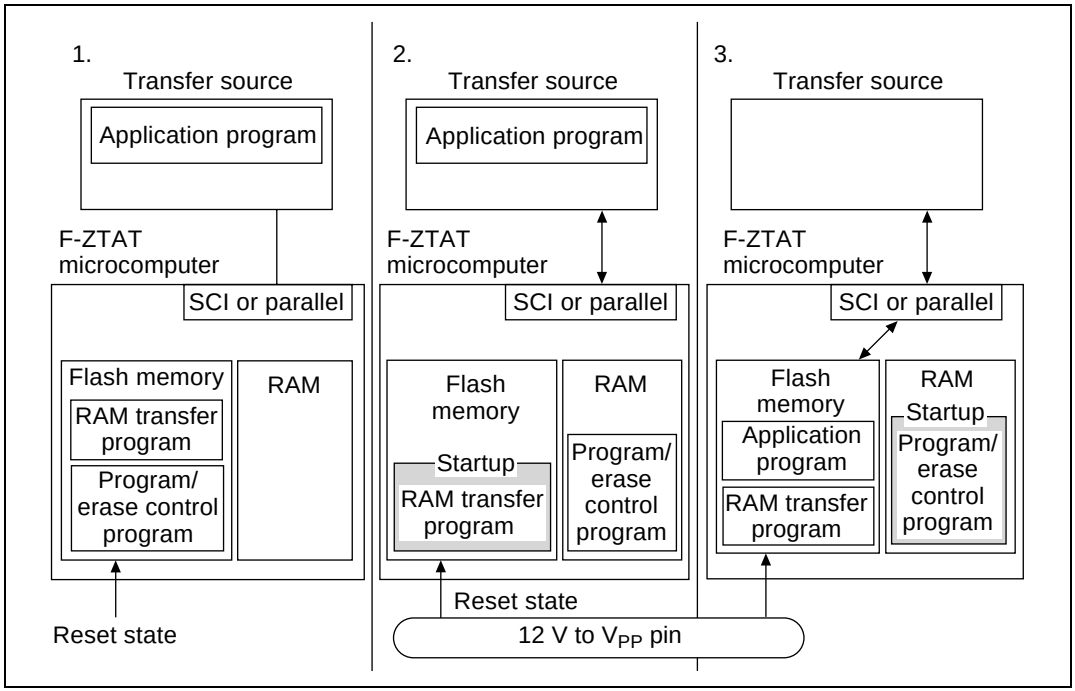


Figure 1.2 User Program Mode Overview

Figures 1.3 to 1.5 show the on-chip flash memory block partitions for each product in the F-ZTAT microcomputer line.

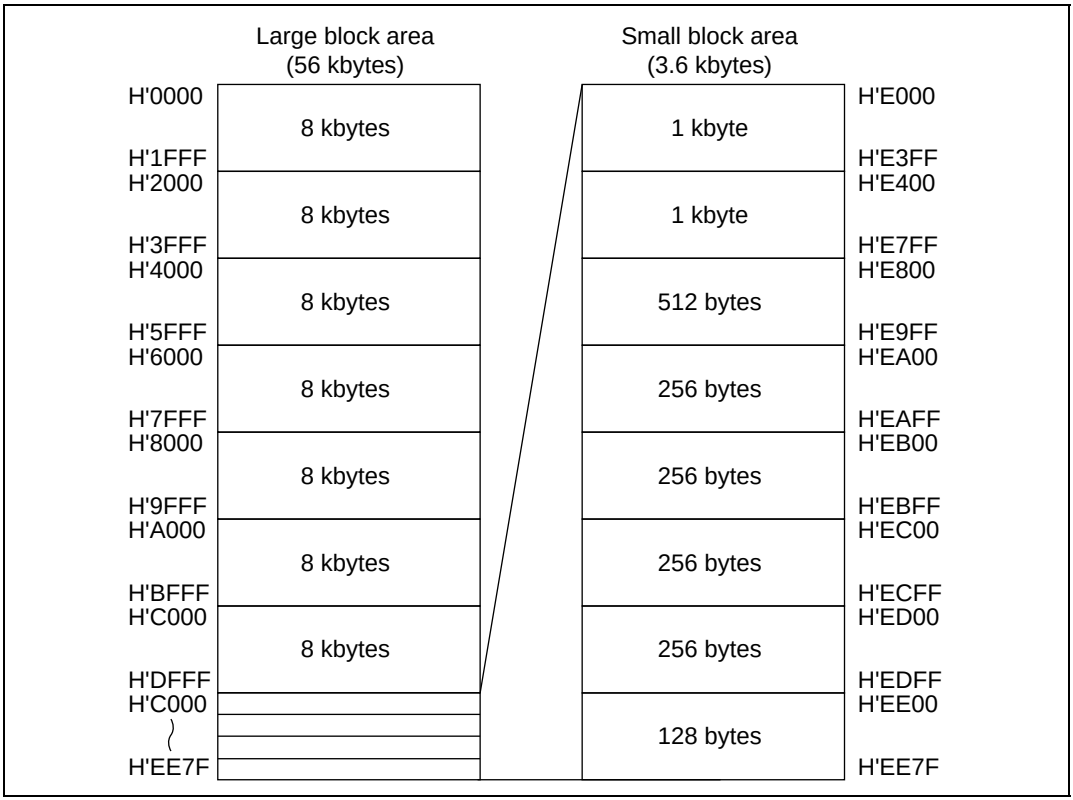


Figure 1.3 Block Partitioning of H8/538F On-Chip Flash Memory

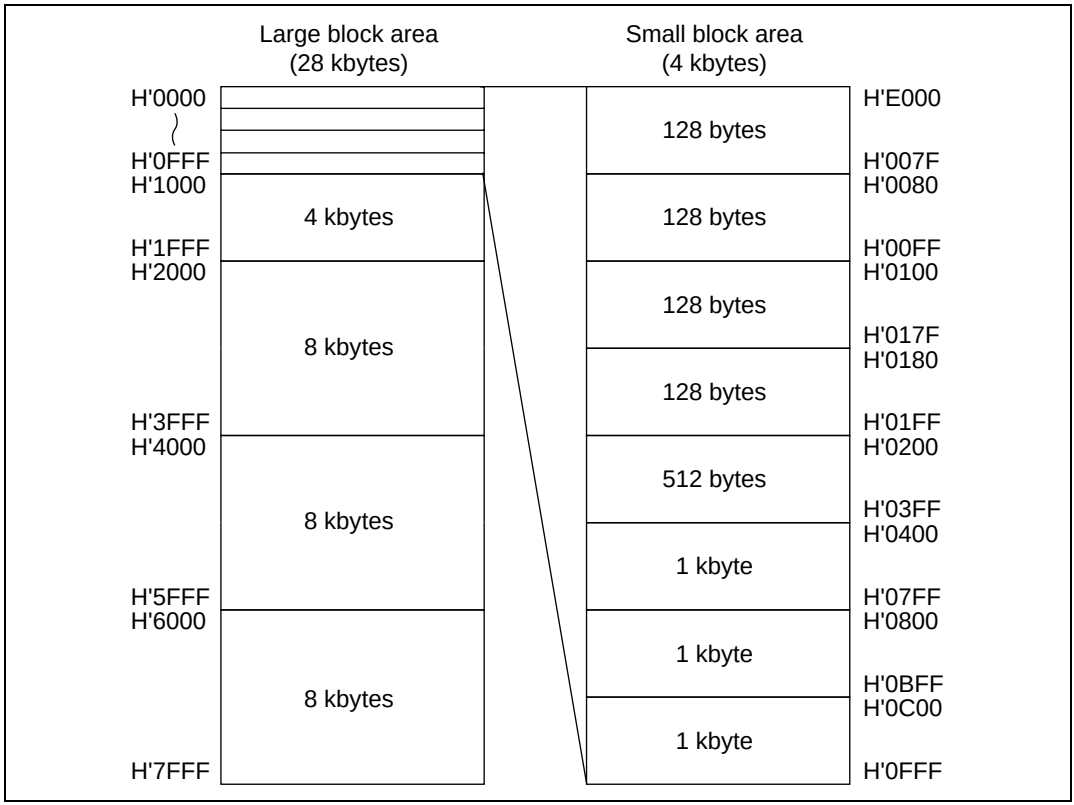


Figure 1.4 Block Partitioning of H8/3434F and H8/3334YF On-Chip Flash Memory

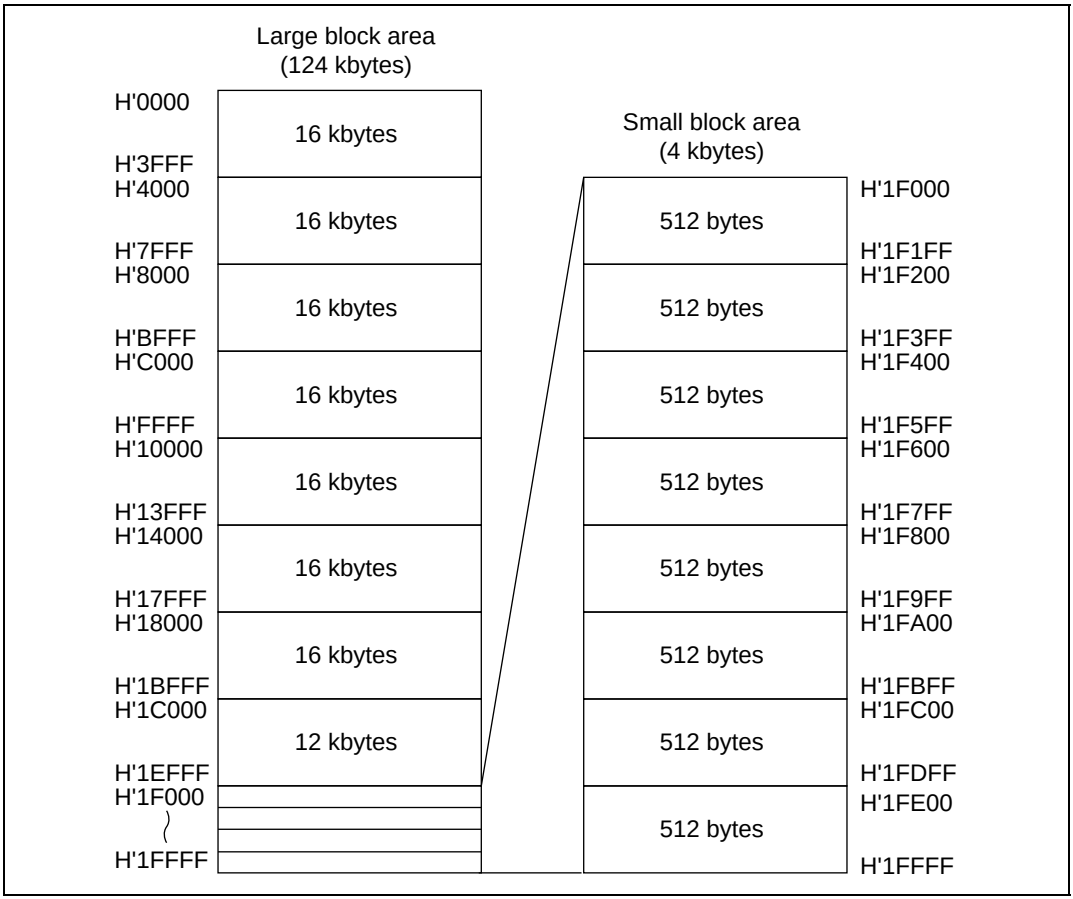


Figure 1.5 Block Partitioning of H8/3048F On-Chip Flash Memory

1.2.3 Flash Memory Emulation by RAM

Flash memory emulation by RAM emulates small block areas of flash memory in the on-chip RAM, allowing real-time rewriting of frequently rewritten parameters and other data during program development. This function reduces the number of data rewrite cycles to flash memory. For RAM area emulation, set the control registers for each device with 12 V applied to the Vpp pin. (H8/538F, H8/3048F: RAM control register (RAMCR) lower 4 bits; H8/3434F, H8/3334YF: wait state control register (WSCR) upper 2 bits.)

Figures 1.6 to 1.10 give an overview of flash memory emulation by RAM in the user program mode.

Preparation for Flash Memory Emulation by RAM: First write the program/erase control program (control program for flash memory program/erase and RAM area change) and the program that transfers this program to RAM, to the F-ZTAT microcomputer's built-in flash memory either in boot mode or PROM mode.

Reset the F-ZTAT microcomputer (figure 1.6).

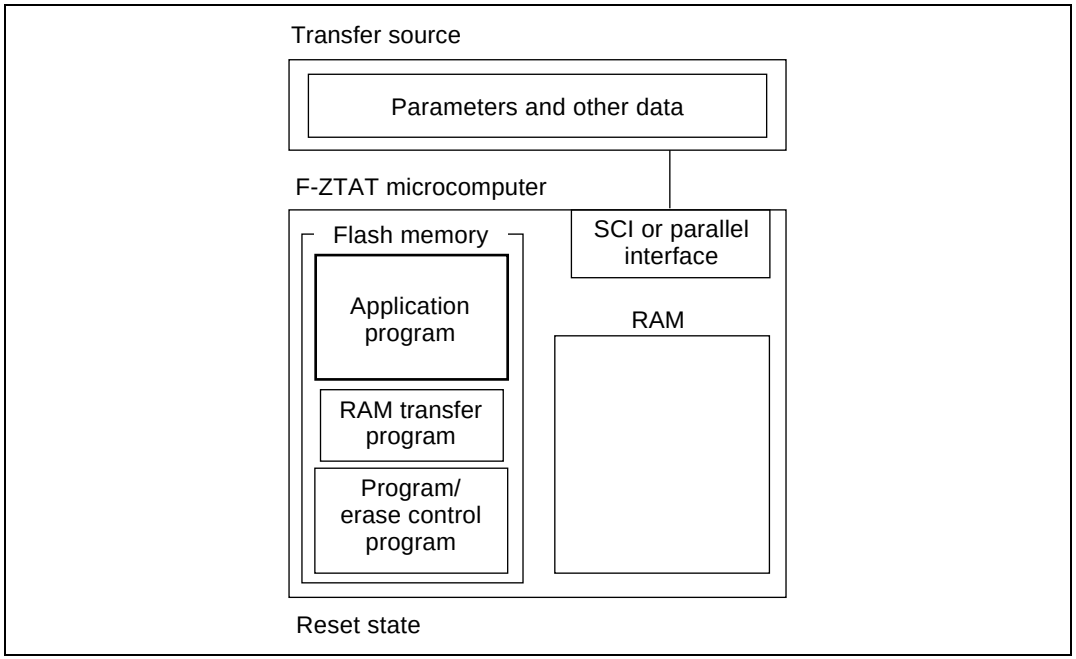


Figure 1.6 Preparation for Flash Memory Emulation by RAM

User Program Mode Startup: Apply 12 V to the Vpp pin to cancel reset and start up the RAM transfer program and transfer the program/erase control program to on-chip or external RAM for startup (figure 1.7).

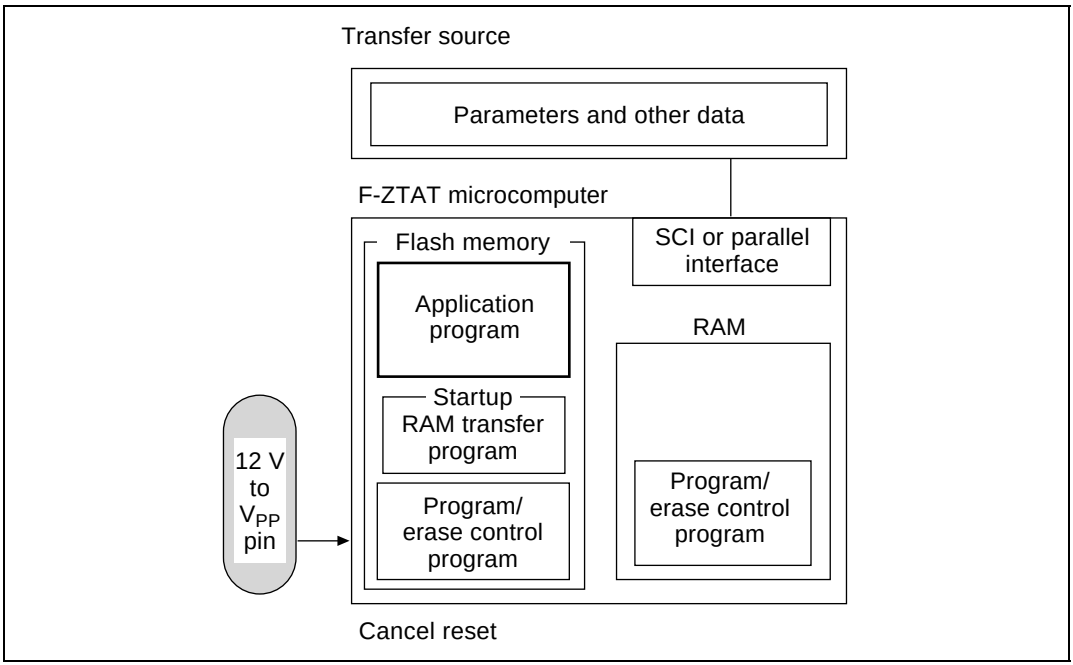


Figure 1.7 User Program Mode Startup

Program/Erase Control Program Startup: Setting the RAM area change register (H8/538F, H8/3048F: RAMCR; H8/3434F, H8/3334YF: WSCR) makes the program/erase control program emulate a flash memory area in part of the RAM area. Next, the F-ZTAT receives program data and writes it to the emulating RAM area (figure 1.8).

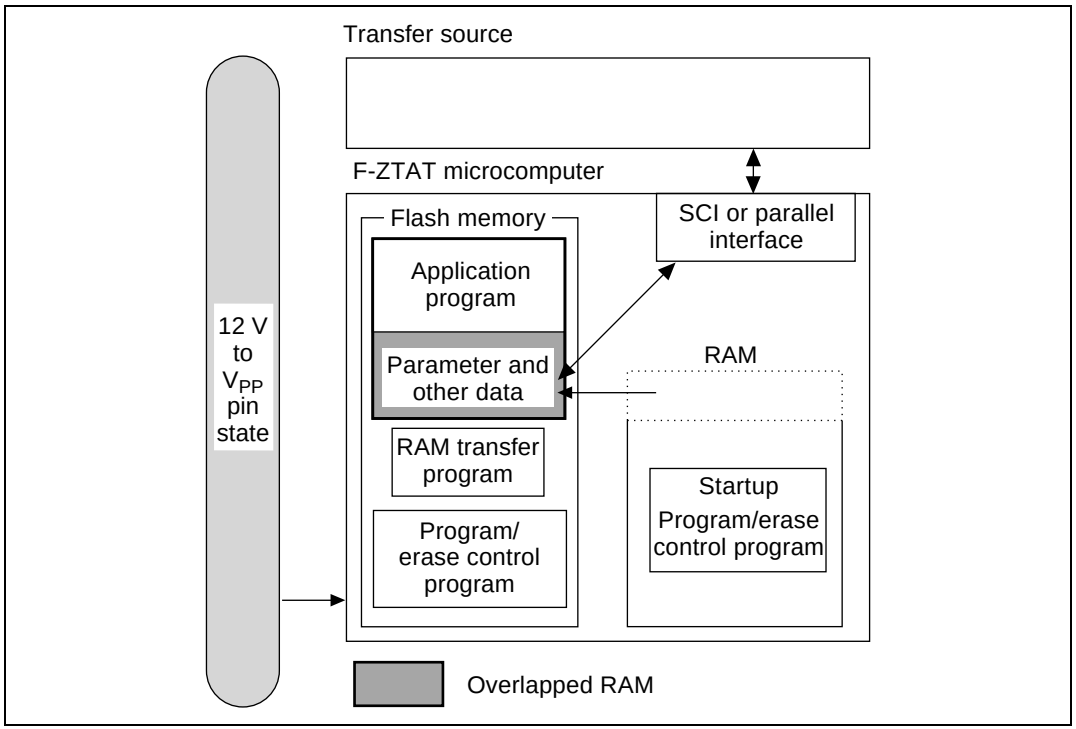


Figure 1.8 Program/erase Control Program Startup

Application Program Startup: After programming, the program/erase control program branches to the application program. After the branch, the user checks whether the application is running normally. To change data again, restart user program mode, and rewrite the required parameters and other data (figure 1.9).

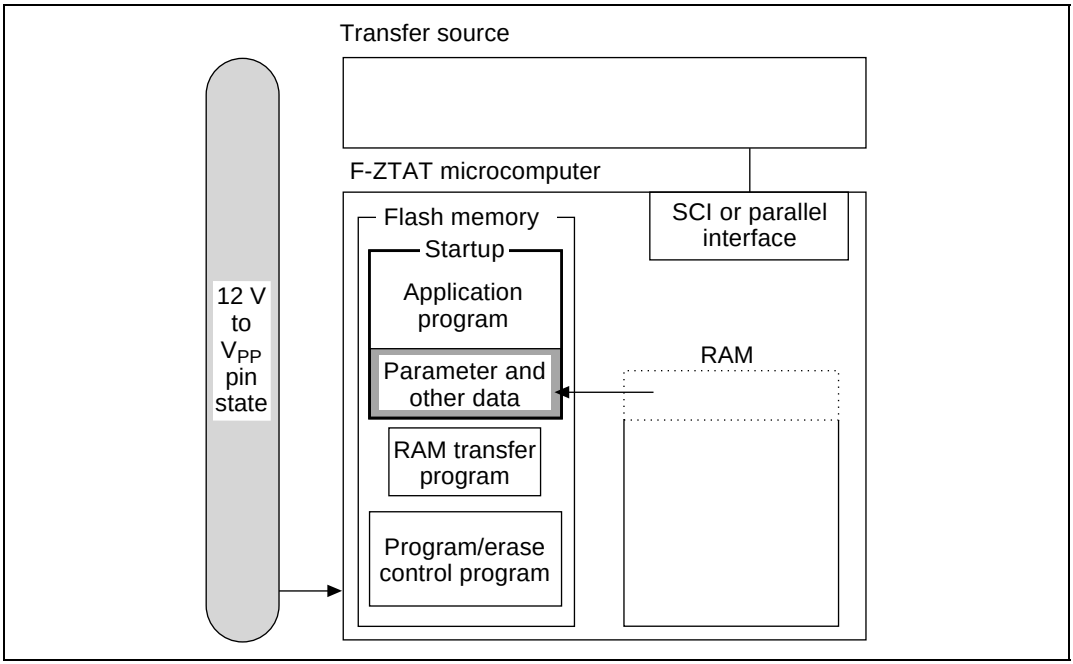


Figure 1.9 Application Program Startup

Writing to Flash Memory: After data confirmation, cancel RAM emulation. (H8/538F, H8/3048F: RAMCR's RAMS bit; H8/3434F, H8/3334YF: WSCR's RAMS and RAM0 bits are cleared.)

Data written to RAM is held externally, and can be written again to flash memory in user program mode (figure 1.10).

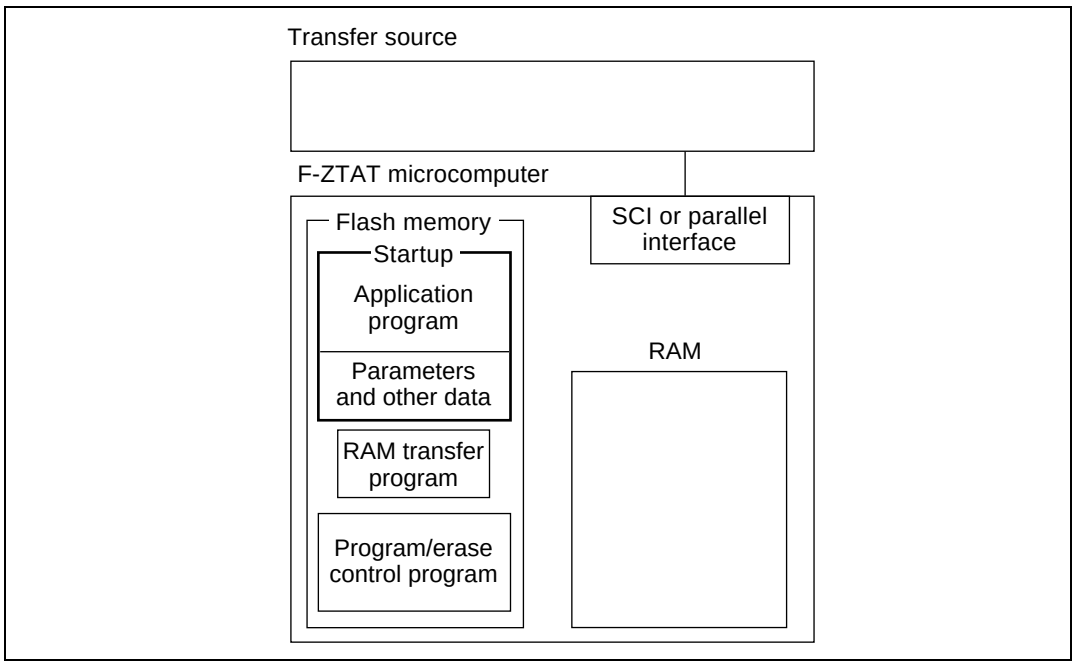


Figure 1.10 Writing to Flash Memory

RAM Area Change Register: To emulate flash memory area in RAM, set the control register for each device with 12 V applied to the Vpp pin. (H8/538F, H8/3048F: RAM control register (RAMCR) lower 4 bits, H8/3434F, H8/3334YF: wait state control register (WSCR) upper 2 bits.)

Setting methods for the RAMCR of H8/3048F and for the WSCR of H8/3434F and H8/3334YF are shown in the respective F-ZTAT microcomputer hardware manuals (flash memory Emulation by RAM).

Table 1.2 shows how to set the overlap area for the H8/538F RAM.

Table 1.2 Overlap Area Setting Method for the H8/538F RAM

Bit 3	Bit 2	Bit 1	Bit 0		
RAMS	**RAM2**	**RAM1**	**RAM0**	**Used RAM Area**	**RAM Overlap Area**
0	0/1	0/1	0/1	H'F680 to H'F6FF	H'F680 to H'F6FF
1	0	0	0		H'EC00 to H'EC7F
1	0	0	1		H'EC80 to H'ECFF
1	0	1	0		H'ED00 to H'ED7F
1	0	1	1		H'ED80 to H'EDFF
1	1	0	0		H'EE00 to H'EE7F

- Bits 3 to 0 set a small block area of flash memory to overlap a RAM area.
- Bits 3 to 0 can be set when 12 V is applied to the Vpp pin.
- The overlap RAM area is 128 bytes located at addresses H'F680 to H'F6FF (figure 1.11).
- The flash memory area that can be superimposed in RAM (H'EC00 to H'EE7F) is 128 bytes × 5 blocks.

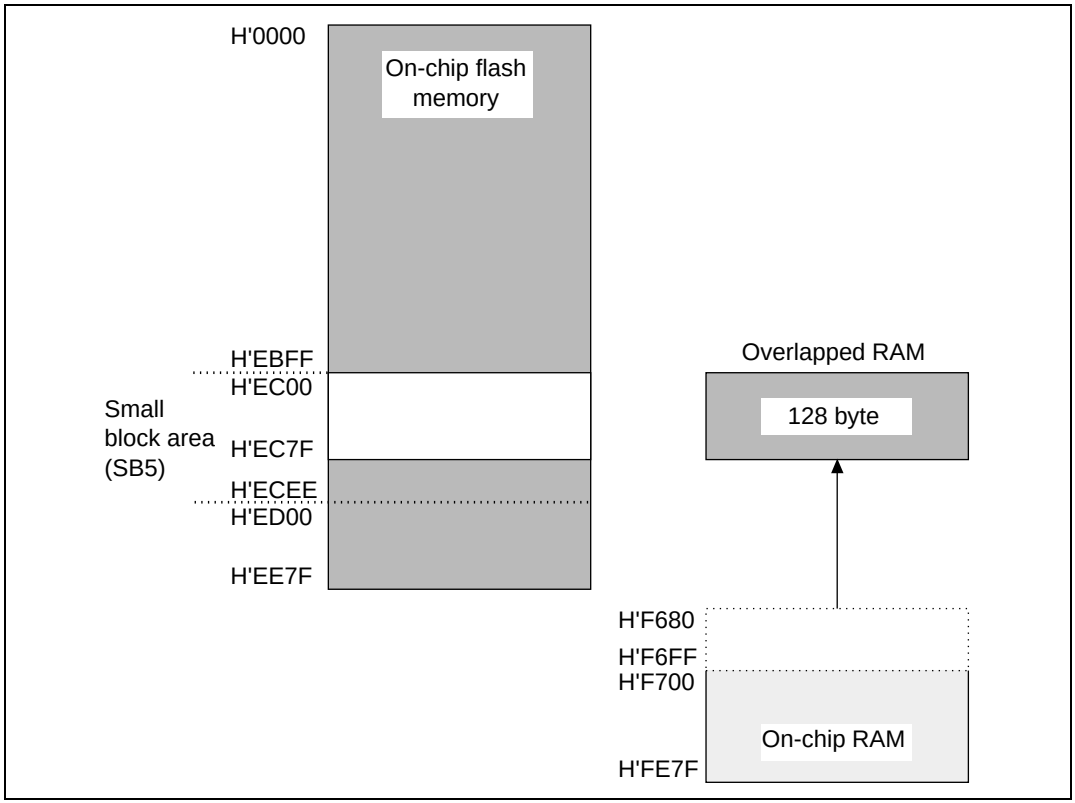


Figure 1.11 RAM Overlap Operation Example (Addresses H'EC00 to H'ECFF)

1. Apply 12 V to the Vpp pin, and set RAMCR bits 3 to 0 to 1, 0, 0, 0.

2. Setting RAMCR causes RAM area addresses H'F680 to H'F6FF overlap with flash memory area addresses H'C00 to H'ECFF) in RAM.

3. When canceling the overlap, reset RAMCR bits 3 to 0, and cut the 12 V to the Vpp pin.

Notes: 1. When overlapping flash memory area in RAM, it is not possible to access the overlapped flash memory area. Access is resumed when you cancel overlap.

2. RAM area addresses H'F680 to H'F6FF overlapping flash memory area allow access in two areas: the flash memory overlap area and original area (addresses H'F680 to H'F6FF).

3. When the RAMS bit of RAMCR is set to 1, all areas of flash memory are protected against programming and erasure, rendering program/erase invalid. Therefore, set the RAMS bit to 0 for program/erase.

4. For details of flash memory program/erase protection see the hardware manual of the particular F-ZTAT microcomputer device you are using (program/erase protect mode).

1.2.4 Program Voltage (Vpp = 12 V) On/Off, and Reset Signal Timing

For program/erase of an application program in the F-ZTAT microcomputer's built-in flash memory, use the timing shown in figure 1.12 for Vpp (12 V) on/off and reset signal control.

Precautions:

1. If the Vcc voltage does not satisfy the rated voltage (Vcc = 2.7 to 5.5 V), do not turn Vpp (12 V) on/off since this could result in an erroneous program/erase operation to flash memory.

2. When applying Vpp with Vcc power on, apply Vpp during oscillation settling time (toscl = 20 ms) after reset has been held low.

3. Turn Vpp on/off when the F-ZTAT microcomputer is reset, or when the CPU is not accessing flash memory (during execution of a program in on-chip RAM or external memory space). Flash memory cannot be read normally the instant Vpp on/off is activated.

4. When doing a program/erase for flash memory when an F-ZTAT microcomputer application is running, turn Vpp on/off after the reset pin has been driven low. (H8/538F: during 6 system clock cycles minimum; H8/3048F, H8/3434F, H8/3334YF: during 10 system clock cycles minimum.)

5. When programming in boot mode, apply 12 V to the mode pin with the same timing as Vpp on/off.

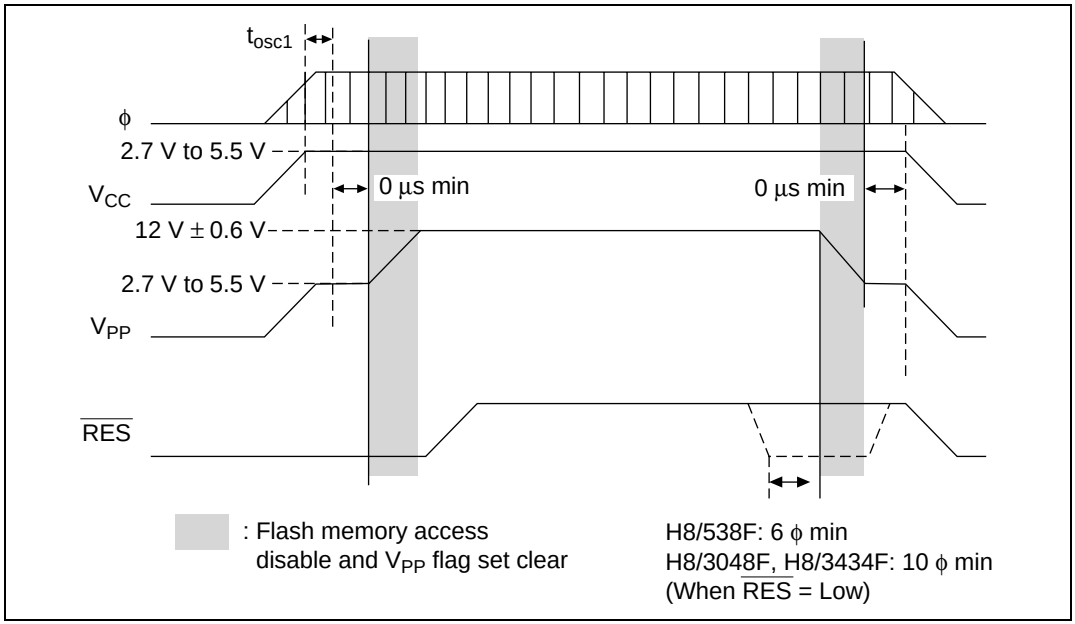


Figure 1.12 Program Voltage (Vpp = 12 V) On/Off Timing

Section 2 On-Board Programming Tools

2.1 Adapter Board

The adapter board is the hardware supplying the required voltage for program/erase during on-board programming of an F-ZTAT microcomputer in a user system.

Figure 2.1 shows the adapter board. Table 2.1 gives a description of the adapter board's switches, connectors, and LEDs. Table 2.2 shows the board's connector pin layout.

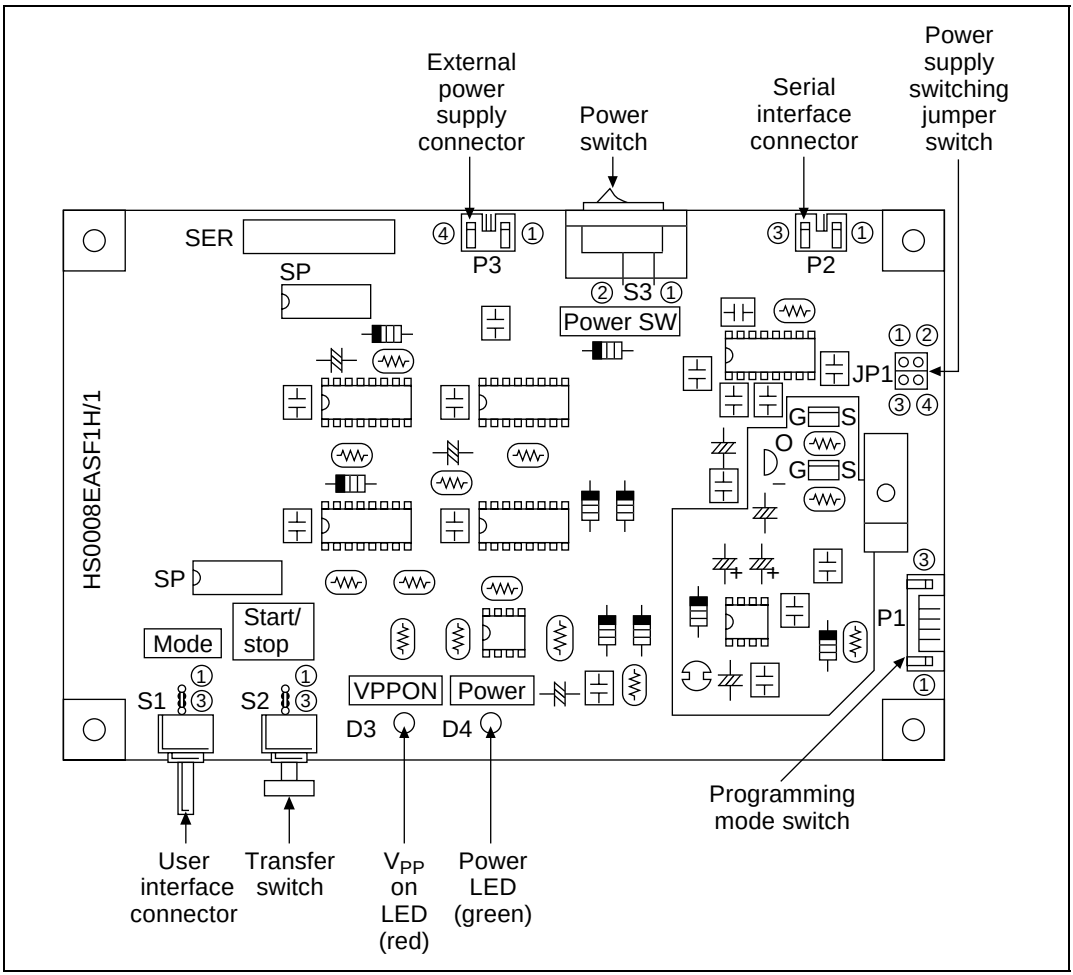


Figure 2.1 Adapter Board

Table 2.1 Adapter Board Switches, Connectors, and LEDs

Name	Function
External power connector	Connects external power (Vcc = 5 V)
Power switch	Controls external power supply on/off
Serial interface connector	Connects RS-232C cable from host machine
Power supply switching jumper switch	Switches power supplies between external source and user machine source
User interface connector	Connects user machine
POWER LED (green)	Lights when adapter board power is on
Vpp ON LED (red)	Lights when Vpp voltage is applied
Transfer switch	Controls on/off of 12 V voltage required for writing data to F-ZTAT microcomputer
Programming mode switch	Switches between F-ZTAT microcomputer on-board programming modes (boot mode, user program mode)

Table 2.2 Adapter Board Connector Pin Arrangement (User interface connector P1)*1

Pin No.	Pin Name	Comments
1	GND	Ground connection
2	RXD	Receives serial data from user machine
3	TXD	Sends serial data to user machine
4	RES	Outputs reset signal to F-ZTAT microcomputer on user machine
5	VIN	Inputs Vcc (3 V to 5 V) from user machine
6	Vpp	Applies 12 V needed for on-board programming to Vpp pin
7	Mode pin*2	Applies 12 V needed for on-board programming to mode pin
8	GND	Ground connection

Notes: 1. Manufacturer: Koku Denshi Model: IL-S-8P-S2L2-EF
2. Mode pin: 12 V applied to mode 2 pin of H8/538F and H8/3048F (MD2) and to mode 1 pin (MD1) of H8/3434F and H8/3334YF.

Table 2.3 Serial Interface Connector P2*

Pin No.	Pin Name	Comments
1	RXD	Receives serial data from host machine
2	TXD	Sends serial data to host machine
3	GND	Ground connection

Note: * Manufacturer: Koku Denshi; Model: IL-S-3P-S2L2-EF

Table 2.4 External Power Connector P3*

Pin No.	Pin Name	Comments
1	NC	Not connected
2	VIN	Inputs Vcc (5 V) from external power supply
3	NC	Not connected
4	GND	Ground connection

Note: * Manufacturer: Koku Denshi; Model: IL-S-2P-S2L2-EF

2.2 Hardware Configuration

The adapter board (figure 2.2) is composed of:

- An RS-232C interface (a)
- Switch unit (program mode switching/Vcc, Vpp supply on/off) (b)
- On-board programming power supply timing unit (c)
- Power supply (d)

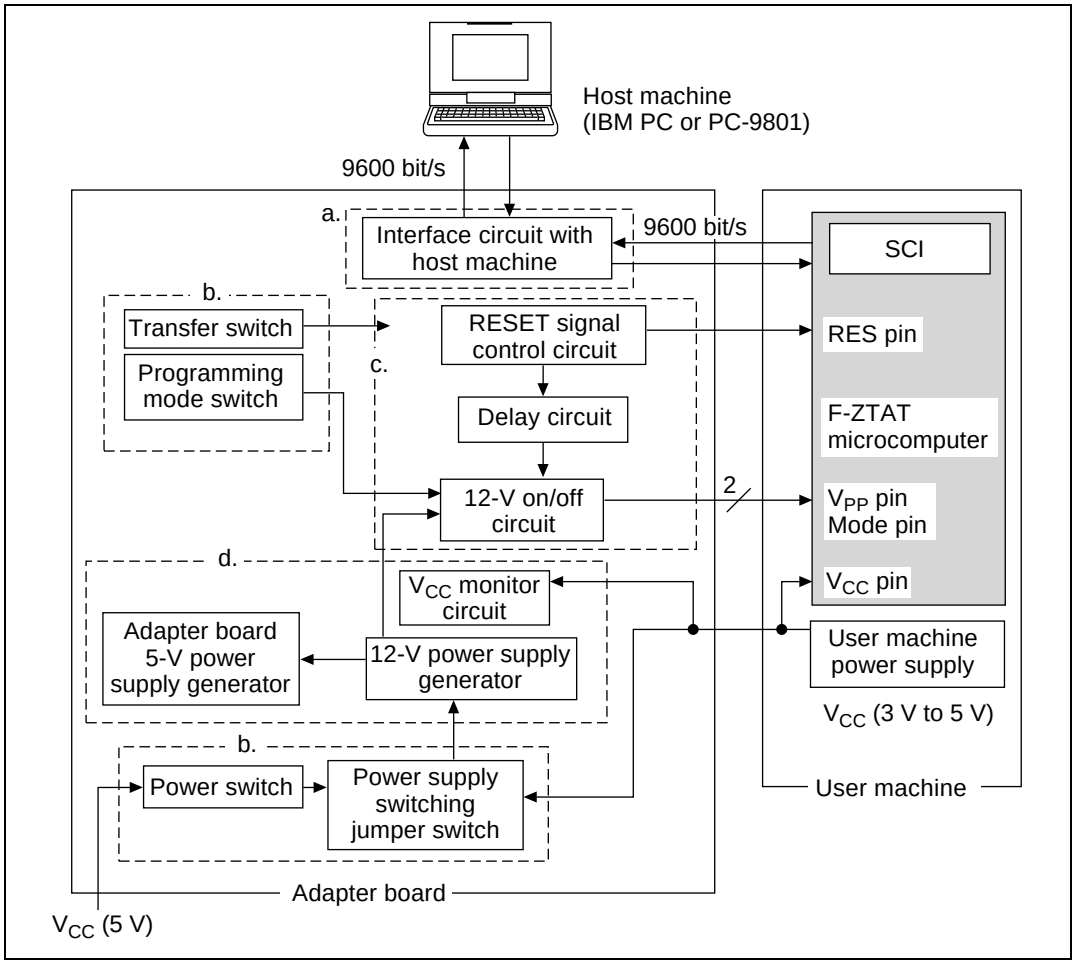


Figure 2.2 Adapter Board Configuration

Sections a, b, c, and d in figure 2.2 correspond to sections 2.2.1 to 2.2.4.

2.2.1 RS-232C Interface

Hardware Specification: Converts signal line voltage level (RS-232C ↔ CMOS/TTL level) during serial communications with host machine or user system.

Figure 2.3 shows a circuit configuration example of the RS-232C interface section.

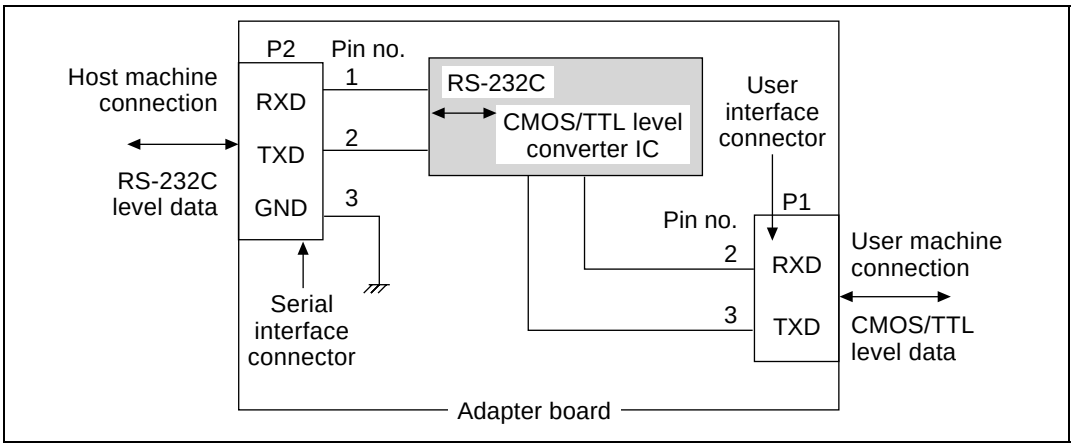


Figure 2.3 RS-232C Interface Circuit Configuration Example

Hardware Operation: Converts the signal line voltage between 12 V level ↔ CMOS/TTL level during serial communication using an RS-232C ↔ CMOS/TTL level converter IC.

Connection of Adapter Board to an IBM PC: Use an RS-232C cable for connection to an IBM PC (figure 2.4).

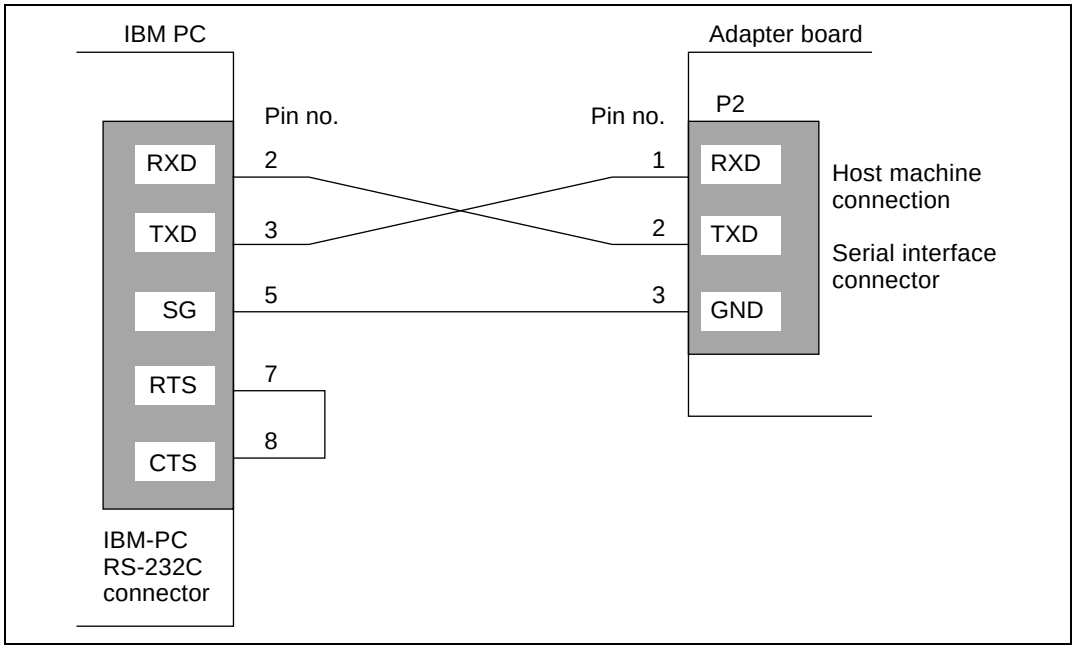


Figure 2.4 Connecting the Adapter Board to an IBM PC

Connection of Adapter Board to a PC-9801: Use an RS-232C cable for connection to a PC-9801 (figure 2.5).

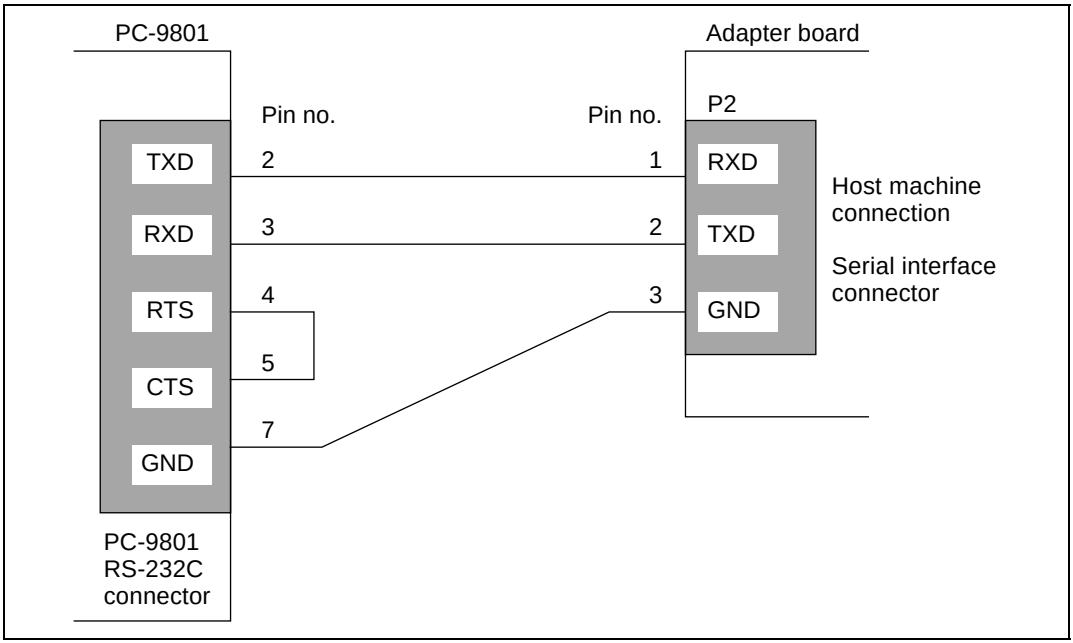


Figure 2.5 Example of RS-232C Interface Circuit Configuration

2.2.2 Switch Unit (Program Mode Switching and Vcc/Vpp On/Off)

Program Mode Switching (S1): Switches between the F-ZTAT microcomputer's on-board programming modes: boot mode (apply 12 V to Vpp pin and mode pin) and user program mode (apply 12 V to Vpp pin). Figure 2.6 illustrates programming mode switching.

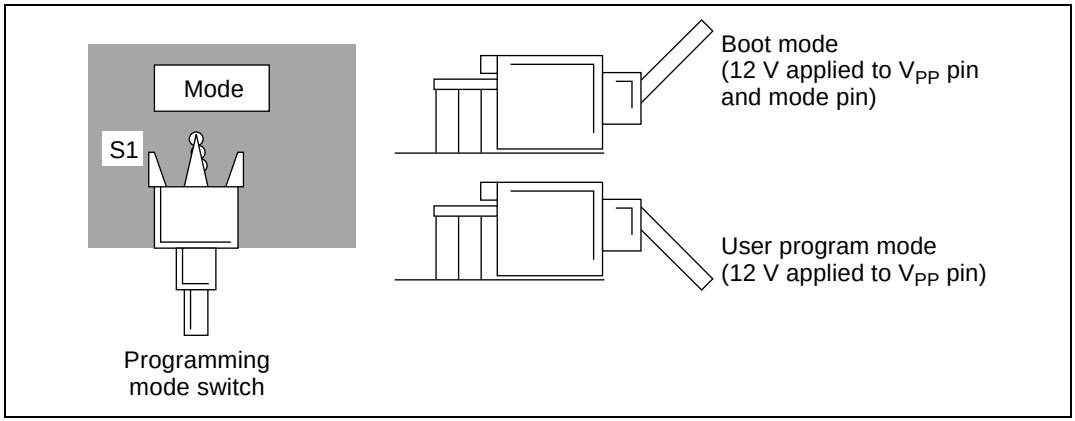


Figure 2.6 Programming Mode Switching

Transfer Switch (S2): When you press the transfer switch to start programming of the F-ZTAT microcomputer, an LED (D3) lights, and 12 V is applied. At the end of programming, press the switch again and the LED (D3) goes off, and the 12-V supply is stopped. Figure 2.7 shows the transfer switch.

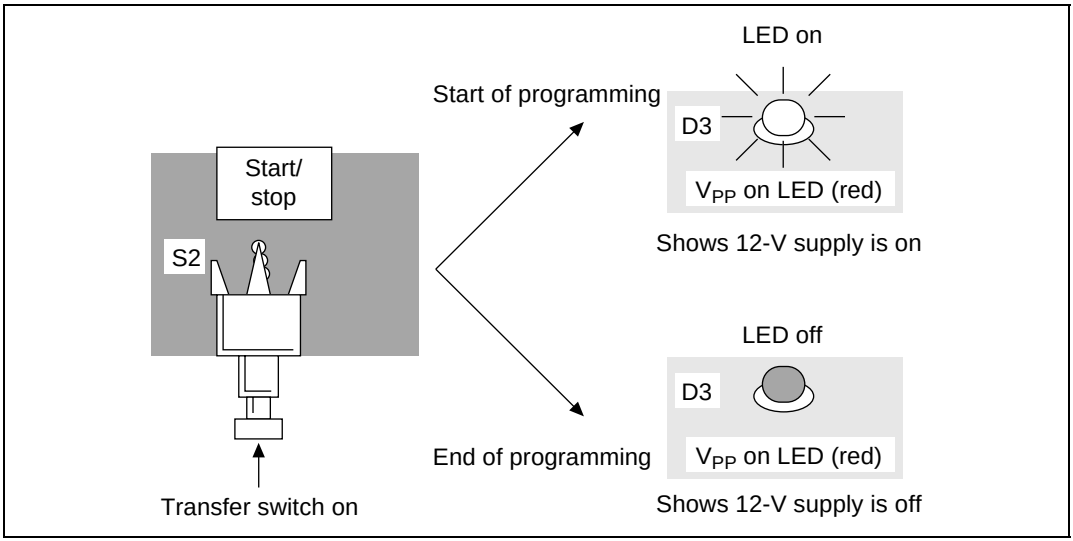


Figure 2.7 Transfer Switch

Power Switch (S3): Controls on/off for Vcc = 5 V from external power supply (figure 2.8).

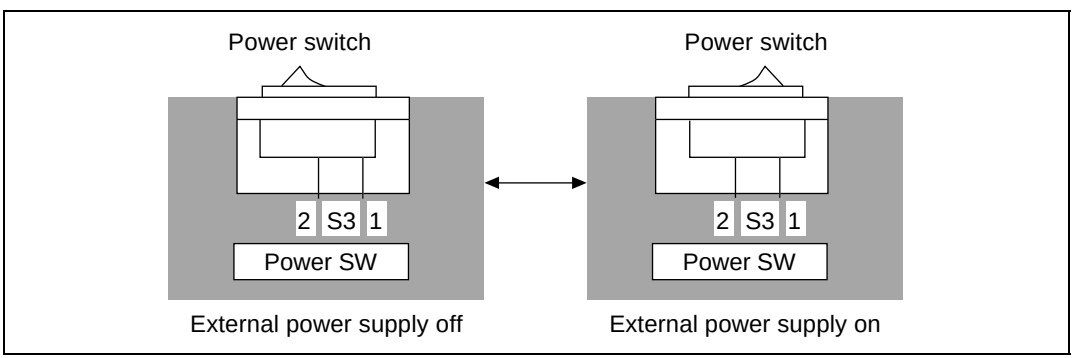


Figure 2.8 Power Switch

Power Supply Switching Jumper Switch (JP1): Switches between external power supply and user machine power supply (figure 2.9).

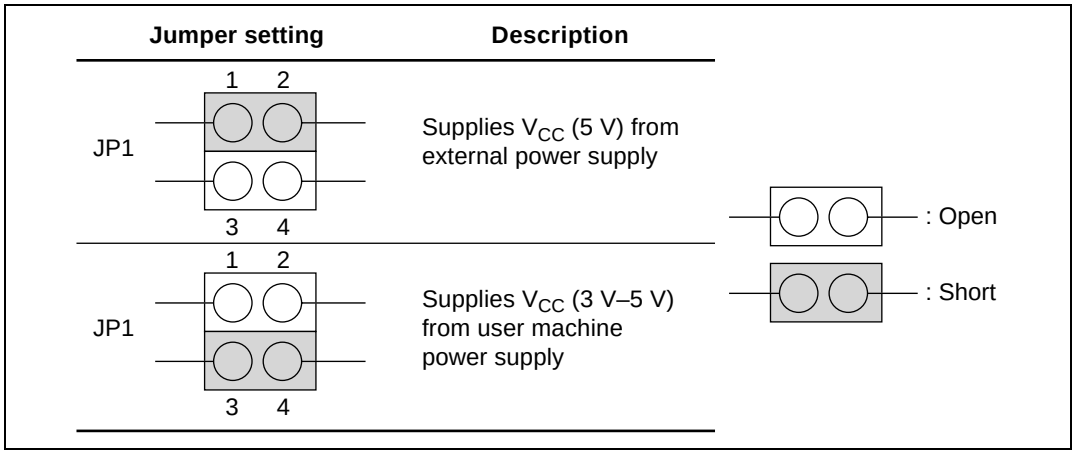


Figure 2.9 Power Supply Switching Jumper Switch

2.2.3 On-Board Programming Power-On Timing Unit

Hardware Specification: Controls the program voltage (Vpp = 12 V) on/off and reset signal output when programming/erasing application programs for the F-ZTAT microcomputer.

Figure 2.10 shows the timing control circuit configuration.

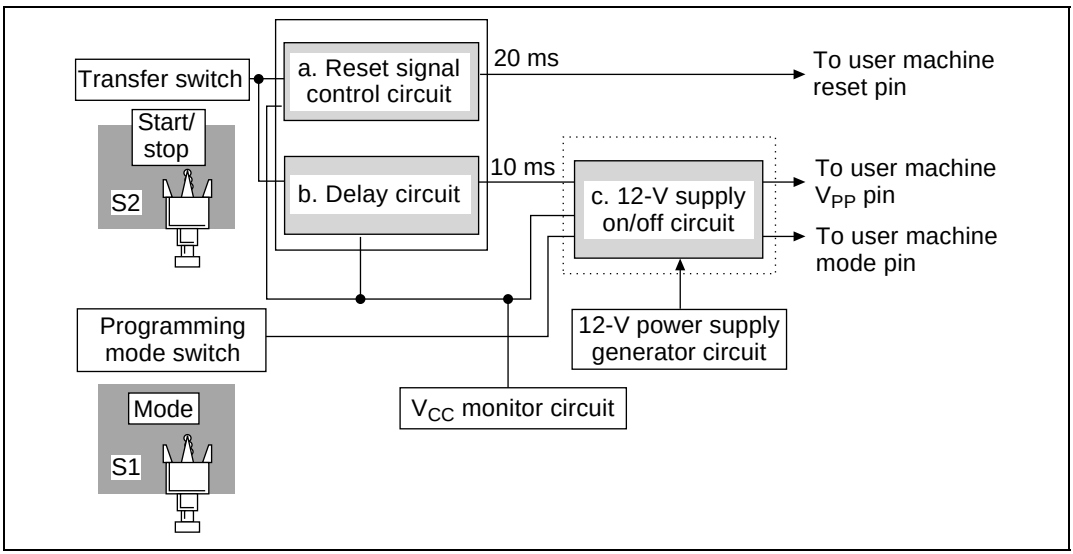


Figure 2.10 Timing Control Circuit Configuration

Hardware Operation: This section details a to c in figure 2.10. Figure 2.11 shows an adapter board timing example.

a. The reset signal control circuit holds the $\overline{RES}$ pin low for 20 ms when you press the transfer switch.
b. The delay circuit allows 12-V on/off for the 12-V on/off circuit 10 ms after the $\overline{RES}$ pin falling edge.
c. When 12-V on/off is enabled from the delay circuit, the 12-V on/off circuit conducts 12-V on/off to the F-ZTAT microcomputer.

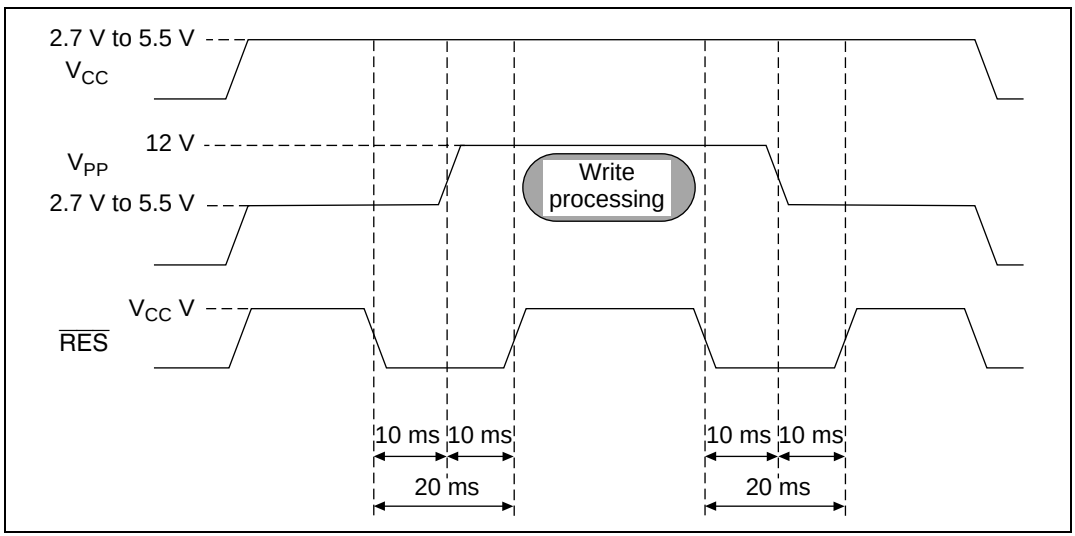


Figure 2.11 Adapter Board 12-V On/Off and Reset Signal Control Timing

2.2.4 Power Unit

Hardware Specification: Generates the 12 V required for F-ZTAT microcomputer programming.

Circuit Configuration: Figure 2.12 shows a circuit configuration example.

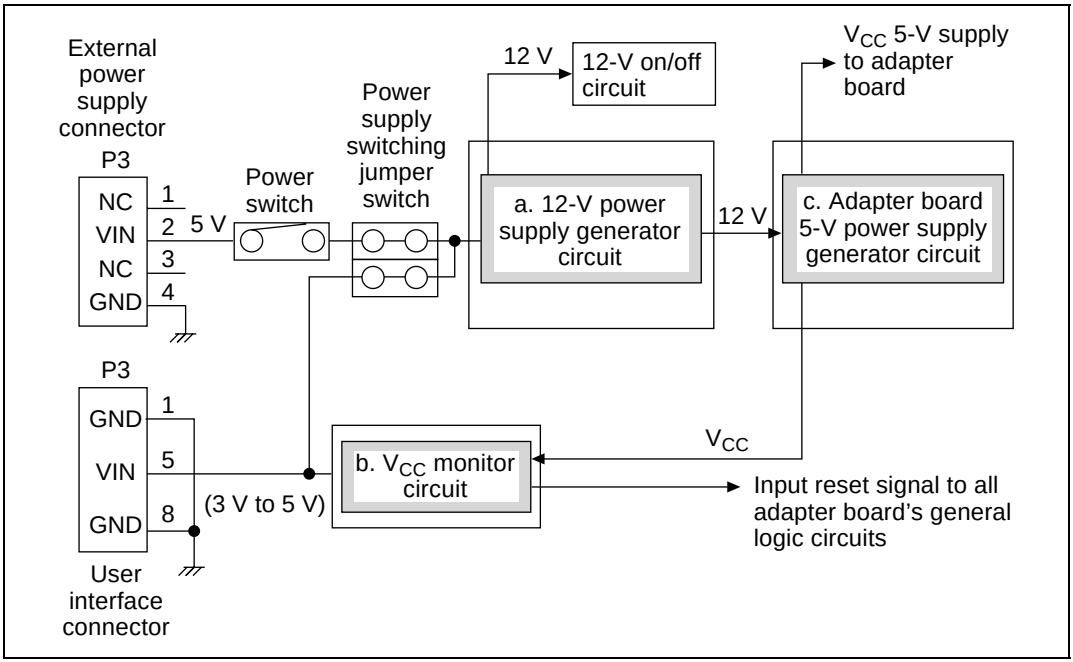


Figure 2.12 Power Unit Circuit Configuration

Hardware Operation:

a. The 12-V power supply circuit inputs either Vcc (3 V to 5 V) from the user machine or Vcc (5 V) from the external power supply depending on the power supply switching jumper switch setting, and generates the required 12 V for F-ZTAT microcomputer programming.

b. Applying 12 V when the F-ZTAT microcomputer's Vcc is not within 2.7 V to 5.5 V could result in a faulty program/erase operation. The user machine Vcc is monitored by the Vcc monitor circuit, and when the voltage drops below 2.6 V (typ.) the 12-V program/erase voltage is not applied to the F-ZTAT microcomputer. If voltage drops below 2.6 V during a 12-V programming voltage supply, the supply is switched off.

c. The adapter board's 5-V power supply circuit converts the 12 V supplied by the 12-V generator to 5 V, and supplies this voltage to the general logic Vcc pin of adapter boards.

2.3 PC Interface Software

PC interface software enables writing of application programs on IBM-PC*1 or PC9801*2 to the F-ZTAT microcomputer's flash memory on-board the user machine.

Notes: 1. IBM-PC is a trademark of International Business Machines (U.S.A.).
2. PC-9801 is a trademark of NEC (Japan).

2.3.1 Functions

Boot Mode:

- Sets the transfer rate (automatic bit rate matching) between the host machine and F-ZTAT microcomputer.
- Transfers the programming control program to the F-ZTAT microcomputer's on-chip RAM.
- Writes the host machine application program (S-type format) to flash memory.
- The programming control program transferred to the on-chip RAM controls writing to flash memory and receiving of the application program.

User Program Mode:

- Writes the host machine application program (S-type format) to flash memory.
- Selects areas of flash memory for block erase from the host machine.
- Enables use of flash memory emulation by RAM function from host machine. (Note that this function is available in PC I/F software version 2.0 or later.)
- Writes the program/erase control program from PC I/F software in advance to flash memory. The control program manages receiving of program/erase and application programs in flash memory by making RAM transfers during user program mode startup.

Connections: Connections between the user machine and host machine are shown in figure 2.13.

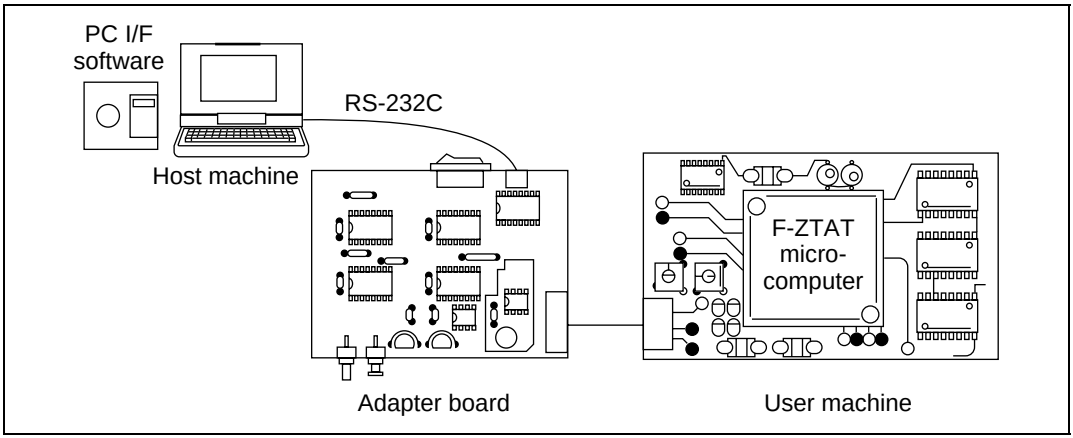


Figure 2.13 User Machine to Host Machine Connection

Operating Environment and Available Formats: Table 2.5 shows the PC I/F software operating environment. (Transfer rate in boot mode is determined by the operating frequency.)

Table 2.5 Operating Environment

Transfer Speed	9600, 4800, 2400 bps
Sync system	Start-stop sync
Data bit	8
Stop bit	1
Parity	None

Available PC I/F software types and MS-DOS versions they run under are given in table 2.6. Table 2.7 shows the file organization.

Table 2.6 PC I/F Software

Host Machine	Product Name	Development Environment
PC-98	HS6400FWPD2SF	MS-DOS (V2.11, V3.1)
IBM-PC	HS6400FWIP2SF	PC-DOS (V3.1)

Table 2.7 PC I/F Software Configuration

File	F-ZTAT Microcomputer		
	H8/538F	H8/3434F	H8/3048F
F-ZTAT microcomputer on-board programming tool	FLASH.EXE (common)		
Flash memory block information file	H8/538F.INF	H8/3434F.INF	H8/3048F.INF
User program/erase control program	H8/538F.SUB	H8/3434F.SUB	H8/3048F.SUB
User program/erase control program source file	H8/538F.SRC	H8/3434F.SRC	H8/3048F.SRC

Note: To start up PC I/F software, it is necessary to change the file names of the flash memory block information file and the user's program/erase control program file. See the F-ZTAT microcomputer on-board programming tools section in the user manual for details. For example, when employing the H8/3048F, change the:

- H8/3048.INF filename to FLASH.INF
- H8/3048F.SUB filename to FLASH.SUB
- H8/3048F.SRC filename to FLASH.SRC

2.3.2 PC I/F Software Display on Host Machine

Display of PC I/F software (version 2.0) on the host machine is described in 1 to 4 below.

1. Display on the host machine when PC I/F software is loaded is as follows:

```
A>FLASH ------------------------------------------- (a)
F-ZTAT MICRO COMPUTER ON-BOARD PURGE/WRITE TOOL Ver2.0
Copyright(c) Renesas Technology Corp.
Licensed Material of Renesas Technology Corp.
Boot Program Mode (Y/N)?------------------------------ (b)
```

Description:

a. Start PC I/F software.

b. Select Yes (Y) for boot mode or No (N) for user program mode.

2. Display on host machine during boot mode startup is as follows:

```
Boot Program Mode (Y/N)? Y---------------------------- (a)

<User Board Setting in Boot Program Mode>-------------- (b)
Charge 12 V at Vpp and MODE pin!
(BOOT PROGRAM MODE)
And then release RESET signal.
Input any key!-----------------------(key input)
Send the Boot program to MCU--------------------------- (c)
******---------------------------------------------- (d)
Finish sending the User program!----------------------- (e)
:W FILENAME.MOT (RET)---------------------------------- (f)
Transfer data address OOOOXXXX------------------------ (g)
:Q---------------------------------------------------- (h)
```

Description:

a. Enter Y to start up boot mode.

b. The hardware setting sequence for starting the F-ZTAT microcomputer's boot program is displayed.

c. Display shows automatic bit rate matching is being conducted, and that the write control program is being transferred.

d. Asterisks (*) are displayed while the boot program erases all areas of flash memory.

e. Display shows that the write control program has been sent.

f. Input the filename of the application program with the W command.

g. Display shows that application program is being sent.

h. End PC I/F software with the Q command.

3. Display on host machine during user program mode startup is as follows:

```
Boot Program Mode (Y/N)? N----------------------------- (a)

<User Board Setting in User Program Mode>-------------- (b)
Charge 12 V at Vpp pin!
(User Program Mode)
BAUDRATE  (1:9600 2:4800 3:2400)----------------------- (c)
Input any key!-------------------(key input)
:W FILENAME.MOT---------------------------------------- (d)
Erase Block address 00000000–0000XXXX(Y/N)?------------ (e)
                    :
Transfer data address 0000XXXX------------------------- (f)
: Q ---------------------------------------------------- (g)
```

Description:

a. Enter N to start up user program mode.

b. The hardware setting sequence for starting the F-ZTAT microcomputer's user program mode is displayed.

c. Set the host machine transfer rate.

d. Input the filename of the application program with the W command.

e. The application program is written. Select flash memory block area erase.

f. Display shows that application program is being sent.

g. End PC I/F software with the Q command.

4. Display on host machine during flash memory emulation by RAM is as follows:

```
:R------------------------------------------ (a)
RAM Emulation OOOOXXXX OOOOXXXX (Y/N)?--------- (b)
                    :
: W FILENAME.MOT XXXX XXXX--------------------- (c)
Transfer data address OOOOXXXX----------------- (d)
:Q ---------------------------------------------- (e)
```

Description:

a. Input the R command for flash memory emulation by RAM.

b. Select part of on-chip RAM for overlapping with flash memory area. (Since the on-chip RAM area for transferring the program/erase control program with the H8/3434F and the H8/3334YF is insufficient, the R command cannot be used.)

c. Input the filename of the application program with the W command to capture in RAM only data in the overlapped flash memory area.

d. “Sending application program” message displayed.

e. End PC I/F software with the Q command.

2.3.3 PC I/F Software Transfer Processing

PC I/F software (version 2.0) has the transfer processing listed in table 2.6.

During flash memory emulation by RAM in boot mode and user program mode, PC I/F software conducts F-ZTAT microcomputer program/erase and flash memory emulation by RAM with the transfer processing items in table 2.8. A transfer processing flowchart for each mode is shown in figure 2.14.

Table 2.8 PC I/F Software Transfer Processing

Transfer Processing	Control Details
Automatic bit rate matching	Sets the transfer rate between host machine and F-ZTAT microcomputer during boot mode (H'00 continuous transfer).
Write control program transfer processing	Transfers write control program (binary data) to the F-ZTAT microcomputer's on-chip RAM.
Start address transfer processing for targeted block(s)	Transfers start address (S-type format) of each erase block for flash memory block erasure.
Application program transfer processing	Transfers application program for writing to flash memory (S-type format).
Ram control register (RAMCR) setting transfer processing	Transfers RAMCR settings for flash memory emulation by RAM.

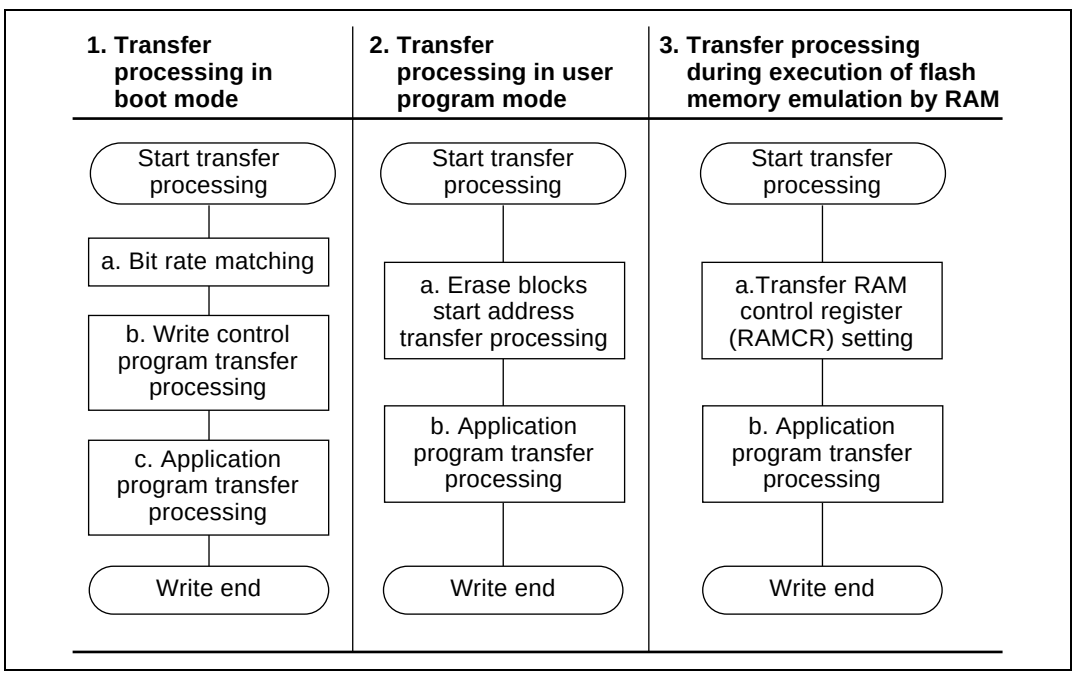


Figure 2.14 Transfer Processing in Each PC I/F Software Mode

Transfer Processing in Boot Mode (Figure 2.14, Process 1): PC I/F software transfer processing details for boot mode are described in 1 to 3 below.

1. Automatic bit rate matching (figure 2.14, step 1a)

   Automatic bit rate matching on the host machine is conducted only when boot mode is selected. Figure 2.15 shows processing for automatic bit rate matching.

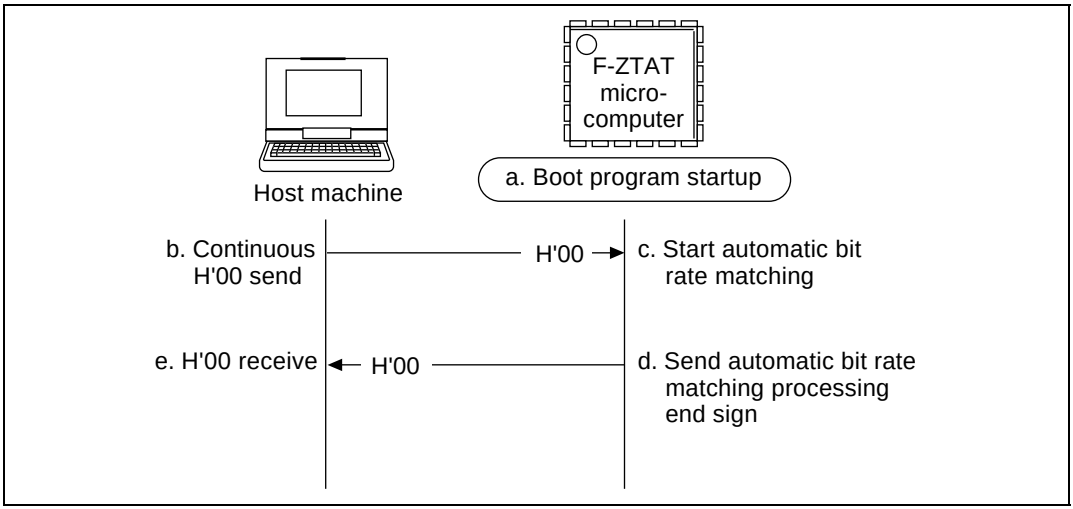


Figure 2.15 Automatic Bit Rate Matching

a. Apply 12 V to the F-ZTAT microcomputer's Vpp pin and mode pin to start the boot program.
b. Host machine sends a continuous H'00.
c. The boot program measures receive data H'00 low period, and begins automatic bit rate matching (setting transfer rate).*
d. At the end of automatic bit rate matching the boot program sends an end sign H'00.
e. Host machine receives end sign H'00 for automatic bit rate matching.

Note: * Automatic bit rate matching (transfer rate setting) is determined by the F-ZTAT microcomputer's operating frequency. The host machine sends H'00 continuously to the F-ZTAT microcomputer at a transfer rate of 9600 bps, and ends automatic matching receiving an end sign H'00. If unable to receive an end sign H'00, the host machine decrements the bit rate in steps (4800 bps to 2400 bps) and continues sending until an end sign H'00 is received. If unable to receive an end sign H'00 at 2400 bps, the error message "FLASH ERROR-FLASH TIME-OUT ERROR" is displayed on the host machine. For more information, see bit rate matching in the F-ZTAT microcomputer hardware manual.

2. Program/erase control program transfer processing (figure 2.14, step 1b)

Write control program transfer processing is conducted after the end of automatic bit rate matching. Figure 2.16 shows program/erase control program transfer processing.

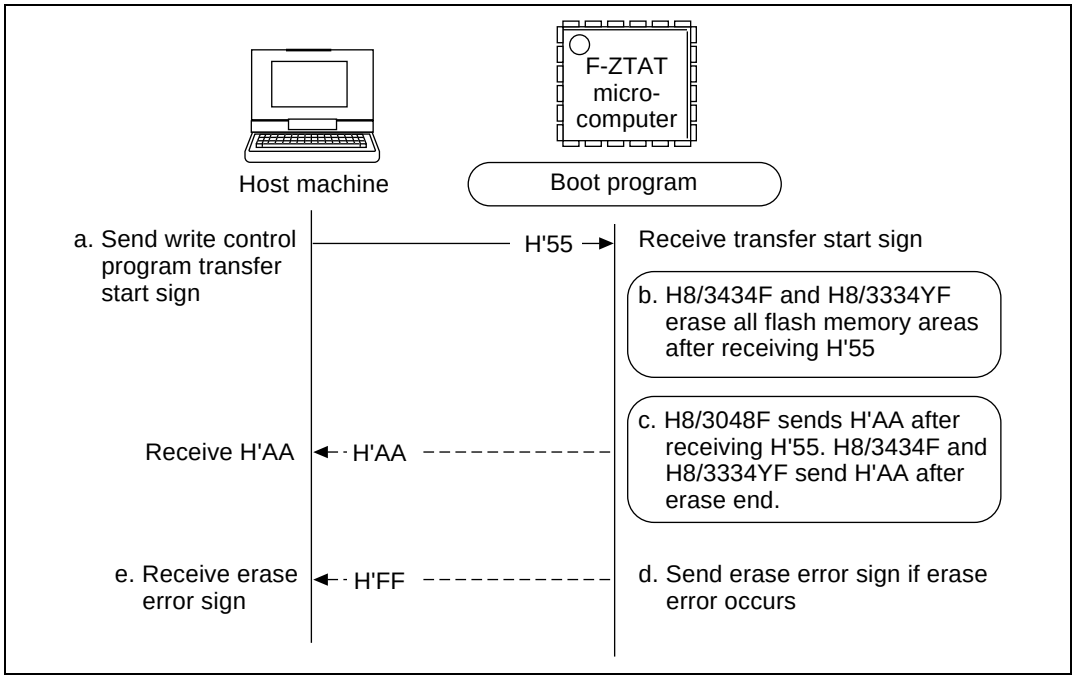


Figure 2.16 Write Control Program Transfer Processing (1)

a. The host machine sends out a start sending H'55 for the program/erase control program.
b. The H8/3434F and the H8/3334YF boot program erases all areas of flash memory after receiving H'55.
c. The H8/3048F boot program sends an H'AA after receiving an H'55. (The H8/538F does not send an H'AA.)

   The H8/538F and H8/3048F shift to program/erase control program transfer processing (2).

   The H8/3434F and the H8/3334YF boot program sends an H'AA after erasing all areas of flash memory.
d. If the H8/3434F and the H8/3334YF boot program failed to erase flash memory correctly, the program sends an H'FF as an erase error sign.
e. The host machine receives an erase error sign H'FF for H8/3434F and the H8/3334YF, and displays the error message “FLASH ERROR-FLASH DEVICE ERROR”.

Figure 2.17 shows program/erase control program transfer processing (2).

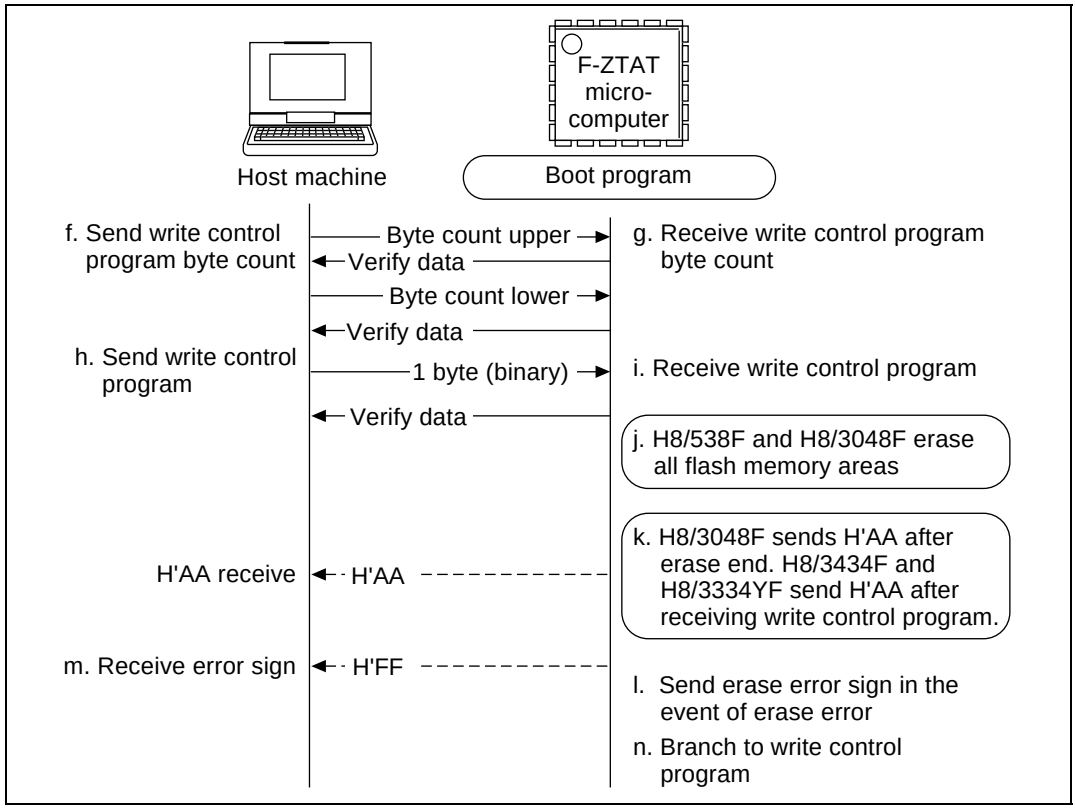


Figure 2.17 Write Control Program Transfer Processing (2)

f. The host machine sends the number of bytes of the program/erase control program in order from upper to lower bytes.

g. The boot program sends verify data for the received number of bytes in byte units for each byte in sequence (echo back).

h. The host machine sends the program/erase control program binary data in byte units. (Note: PC I/F software converts FLASH.SUB files (S-type format) to binary data for transfer.)

i. The boot program transfers the received program/erase control program to the on-chip RAM, and sends verify data in sequence in byte units (echo back).

j. After receiving the program/erase control program, the H8/538F and H8/3048F boot programs erase the entire flash memory area.

k. After erasing the entire flash memory area, the H8/3048F boot program sends an H'AA. (The H8/538F does not send H'AA.) After receiving the program/erase control program, the H8/3434F and H8/3334YF send H'AA and shift to application program transfer processing.

l. If the H8/538F or H8/3048F boot program failed to erase flash memory correctly, the program sends an H'FF as an erase error sign.

m. The host machine receives an erase error sign H'FF for H8/538F and H8/3048F, and displays the error message “FLASH ERROR-FLASH DEVICE ERROR”.

n. The boot program branches to the program/erase control program transferred to the on-chip RAM.

3. Application program transfer (figure 2.14, step 1c)

Application program transfer processing is done after the boot program erases flash memory. Figure 2.18 shows application program transfer processing in boot mode.

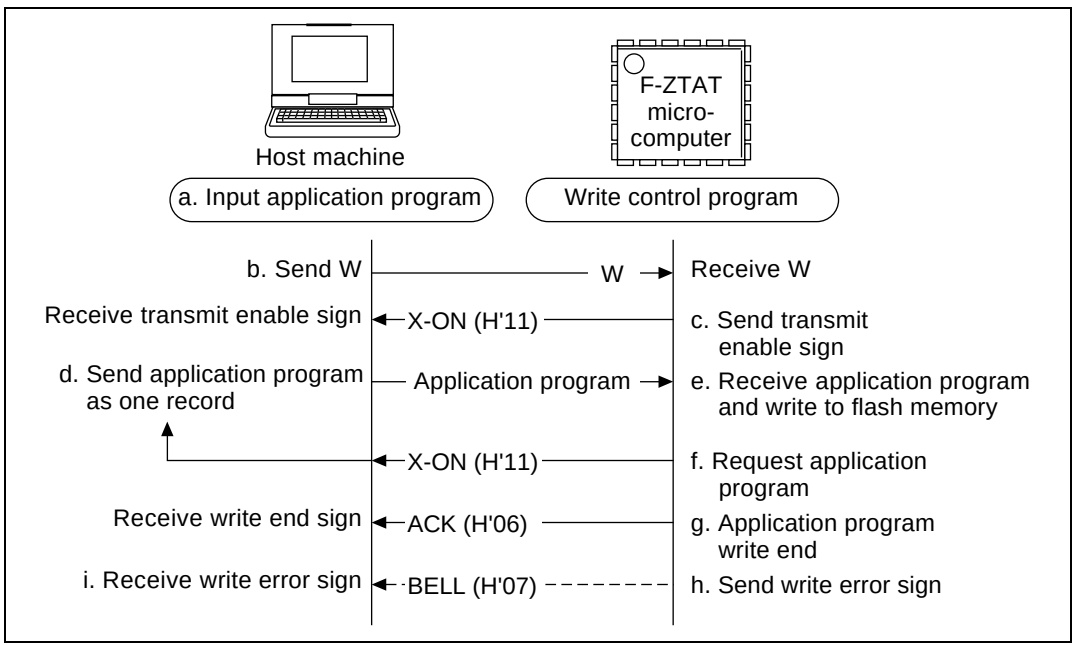


Figure 2.18 Application Program Transfer Processing in Boot Mode

a. Enter the filename of the application program you are writing to flash memory in the host machine.

b. The host machine sends a W command.

c. The program/erase control program sends a send enable sign X-ON (H'11) and an application program transfer request to the host machine.

d. The application program (S-type format) is sent as one record to the host machine.

e. The program/erase control program receives the application program and writes it to flash memory.

f. If the application program is not the final record (S9, S8 record), the program/erase control program sends an X-ON and requests an application program transfer to the host machine.

g. After programming, the program/erase control program sends a programming end sign ACK (H'06).

h. If a programming error occurs, the program/erase control program sends a programming error sign BELL (H'07).

i. The host machine receives the programming error sign BELL and displays the error message “FLASH ERROR-FLASH WRITE ERROR”.

Transfer Processing in User Program Mode (Figure 2.14, Process 2): PC I/F software transfer processing in user program mode is described in 1 and 2 below.

1. Transfer of start address of target erase blocks (figure 2.14, step 2a)

   Transfer processing for the start address of the blocks to be erased is conducted after inputting the application program to be written to flash memory is input in the host machine and after selecting the blocks of flash memory for erasure. Figure 2.19 shows transfer for start address for the objective erase blocks.

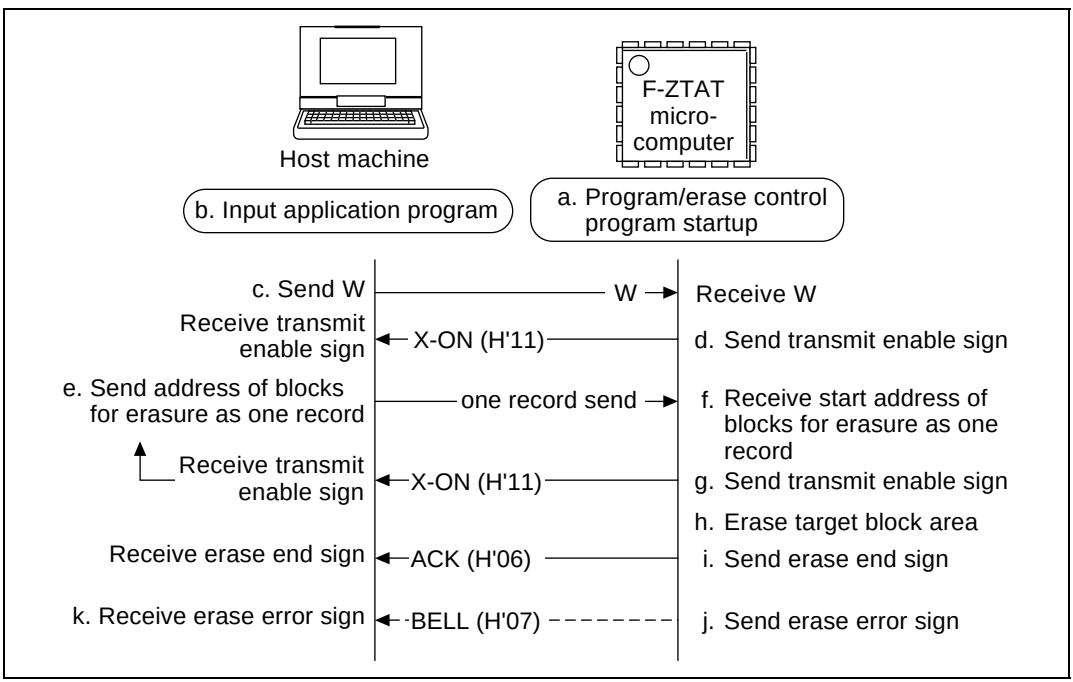


Figure 2.19 Transfer Processing for Target Erase Blocks

a. In user program mode the program/erase control program previously written to flash memory is transferred to on-chip RAM for startup.
b. Enter the filename of the application program for writing to flash memory in the host machine, and select the target blocks of flash memory for erasure.
c. The host machine sends a W command.
d. The program/erase control program sends a transfer data enable sign X-ON (H'11).
e. The host machine sends the start address (S-type format) of the blocks for erasure in one record.
f. The program/erase control program sets the blocks for erasure from the received erase blocks start address.
g. If the received erase blocks start address is not the end record (S9, S8 record), the program/erase control program sends an X-ON and requests transfer of the erase blocks start address to the host machine.
h. After receiving the erase blocks start address, the program/erase control program erases the areas in the objective erase blocks.
i. The program/erase control program sends an ACK (H'06) as an erase end sign.
j. If an erase error occurs, the program/erase control program sends an erase error sign BELL (H'07).
k. The host machine receives the a programming error sign BELL and displays the error message “FLASH ERROR-FLASH ERASE ERROR”.

2. Application program transfer (figure 2.14, step 2b)

Application program transfer processing is done after flash memory erase. Figure 2.20 shows application program transfer processing in user program mode.

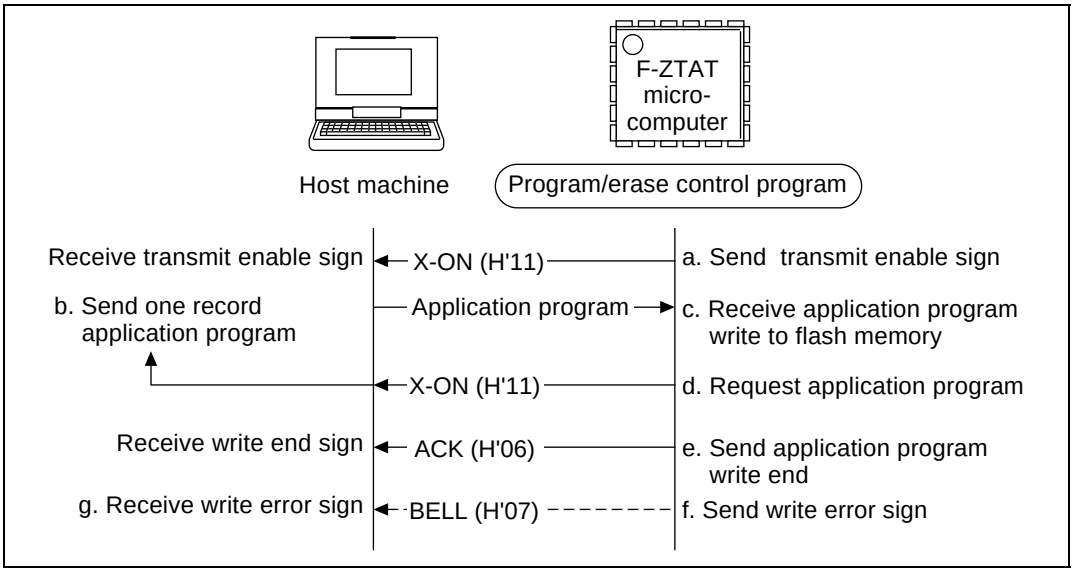


Figure 2.20 Application Program Transfer Processing in User Program Mode

a. After sending the erase end sign, the program/erase control program sends the transmit enable sign X-ON (H'11) and an application program transfer request to the host machine.

b. Send one application program record (S-type format).

c. The program/erase program receives the application program and writes it to flash memory.

d. If the application program is not the last record (S9, S8 record), the program/erase control program sends an X-ON and an application program transfer request to the host machine.

e. After writing, the program/erase control program sends a write end sign ACK (H'06).

f. If a write error occurs, the program/erase control program sends a write error sign BELL (H'07).

g. The host machine receives the write error sign BELL, and displays an error message “FLASH ERROR-FLASH WRITE ERROR”.

Transfer Processing during Flash Memory Emulation by RAM (Figure 2.14, Process 3): Transfer processing during flash memory emulation by RAM is described in 1 and 2 below.

1. Transfer processing for RAM control register (RAMCR) setting (figure 2.14, step 3a)

   RAMCR setting transfer processing is conducted after selecting flash memory emulation by RAM. Figure 2.21 shows RAMCR setting transfer processing.

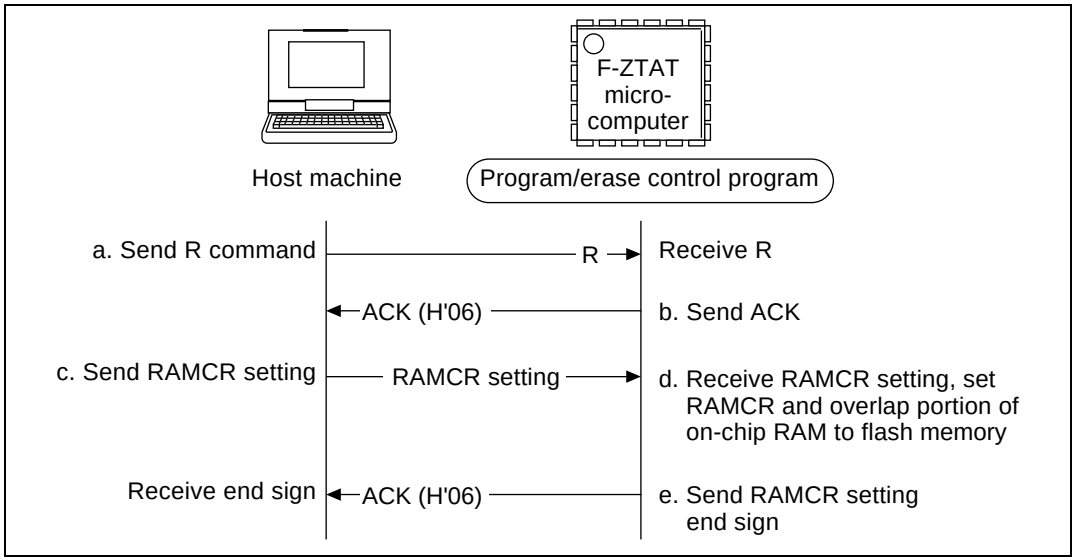


Figure 2.21 RAMCR Setting Transfer Processing

a. Host machine sends the R command.
b. After receiving the R command, the program/erase control program sends an ACK.
c. After receiving the ACK, the host machine sends the RAMCR setting for the selected overlap portion of flash memory in RAM.
d. The program/erase control program receives the RAMCR setting and sets the RAMCR.
e. The program/erase control program sends an ACK after setting RAMCR.

2. Application program transfer (figure 2.14, step 3b)

Application program transfer processing (during flash memory emulation by RAM) is done after the end of RAMCR setting transfer processing. Figure 2.22 shows application program transfer processing during emulation.

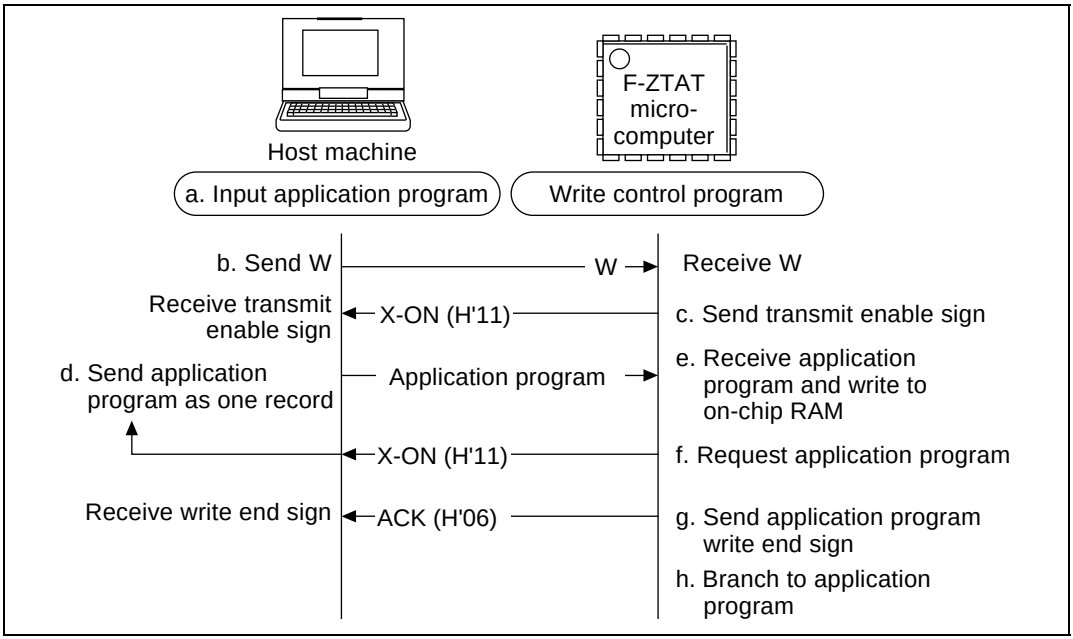


Figure 2.22 Application Program Transfer Processing during Emulation

a. Enter the filename of the application program you are writing to RAM in the host machine.
b. The host machine sends a W command.
c. The program/erase control program sends a send enable sign X-ON (H'11) and an application program transfer request to the host machine.
d. Host machine sends application program (S-type format) 1 record.
e. The program/erase control program receives the application program and writes it to the RAM area overlapping the flash memory area.
f. If the application program is not the final record (S9, S8 record), the program/erase control program sends an X-ON and requests application program transfer to the host machine.
g. After writing, the program/erase control program sends a write end sign ACK (H'06).
h. The program/erase control program branches to the application program.

2.3.4 PC I/F Software Program/Erase Control Program

In boot mode, the PC I/F software program/erase control program controls transfers to the F-ZTAT microcomputer's on-chip RAM and write operations to flash memory. In user program mode, the program/erase control program prewritten to flash memory is transferred to the on-chip RAM and is started to control flash memory program and erase. During flash memory emulation by RAM, the program overlaps a portion of RAM to flash memory area and writes the application program to the overlapped RAM.

Figure 2.23 shows the configuration of the program/erase control program, and details of 1 through 10 in the figure are shown in the flowcharts on the following pages. The H8/3048F is cited as an example for the method of flash memory program and erase.

For more information on flash memory program/erase see flash memory programming and erasure in the relevant F-ZTAT microcomputer hardware manual.

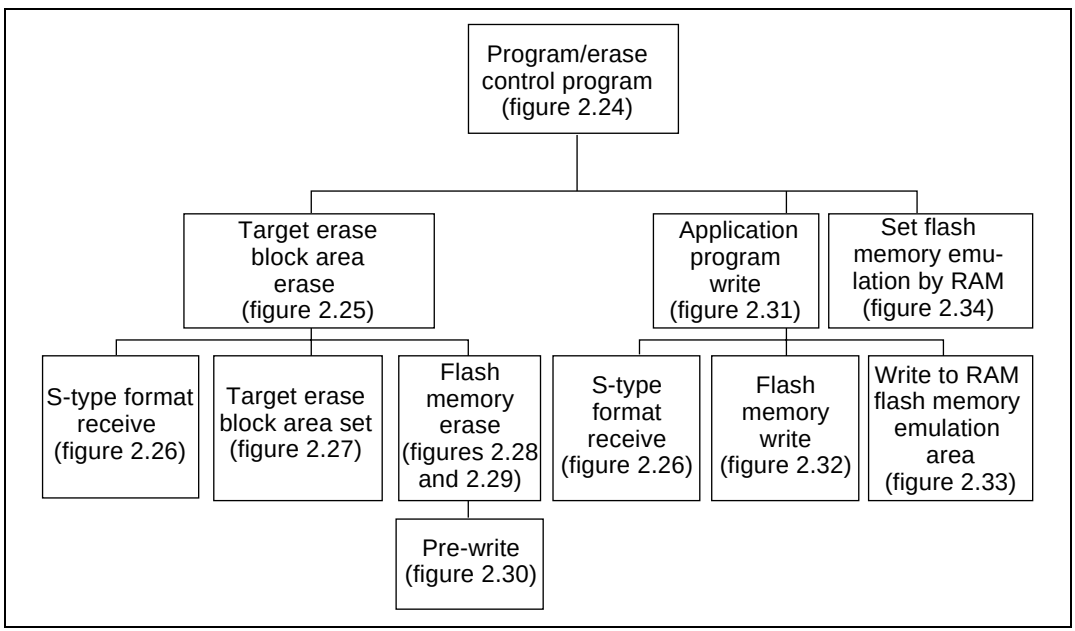


Figure 2.23 Program/Erase Control Program Configuration

Figure 2.24 shows the management of the entire programming control program.

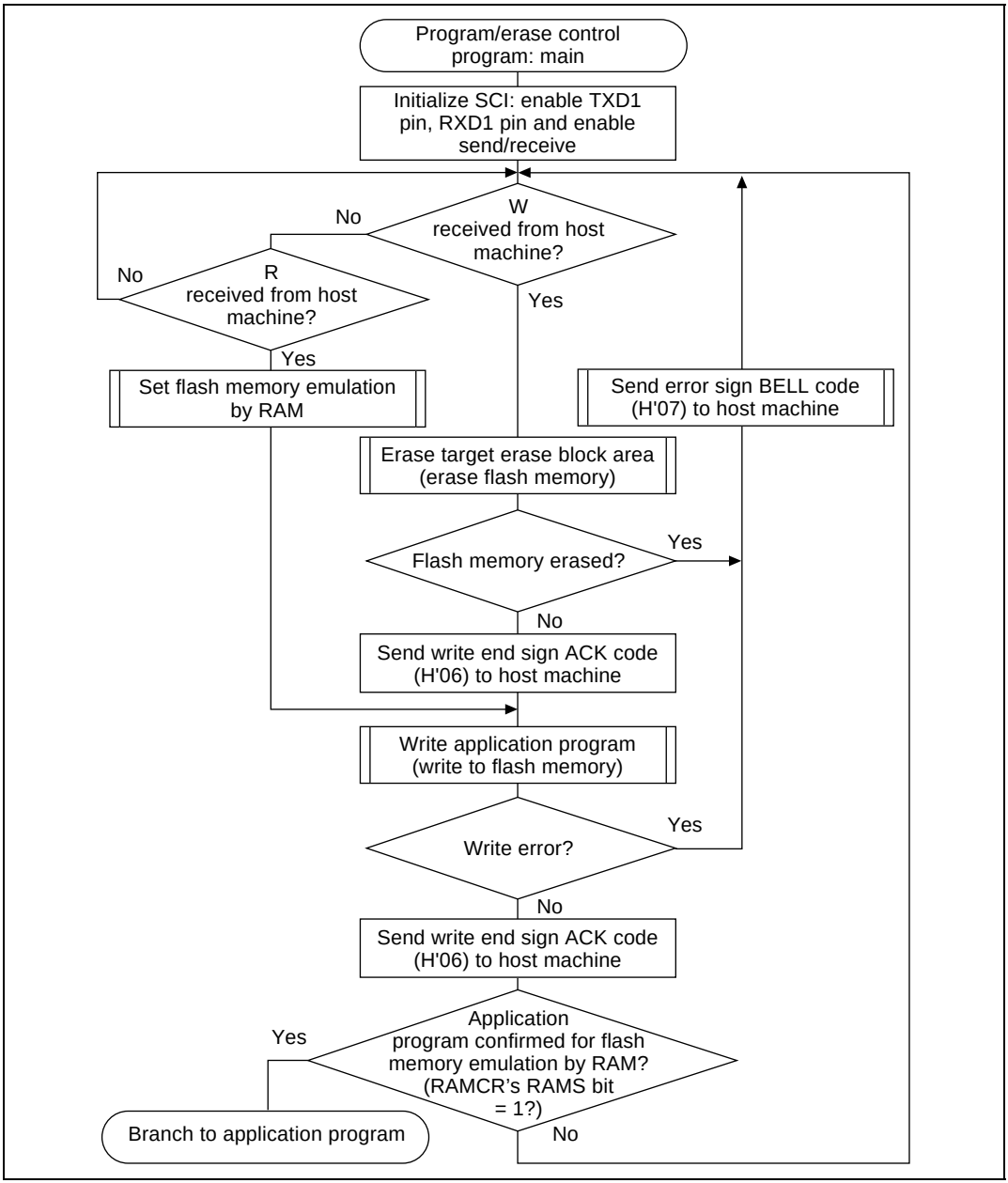


Figure 2.24 Program/Erase Control Program: (Main) Flowchart

Figure 2.25 shows the management of flash memory erasure.

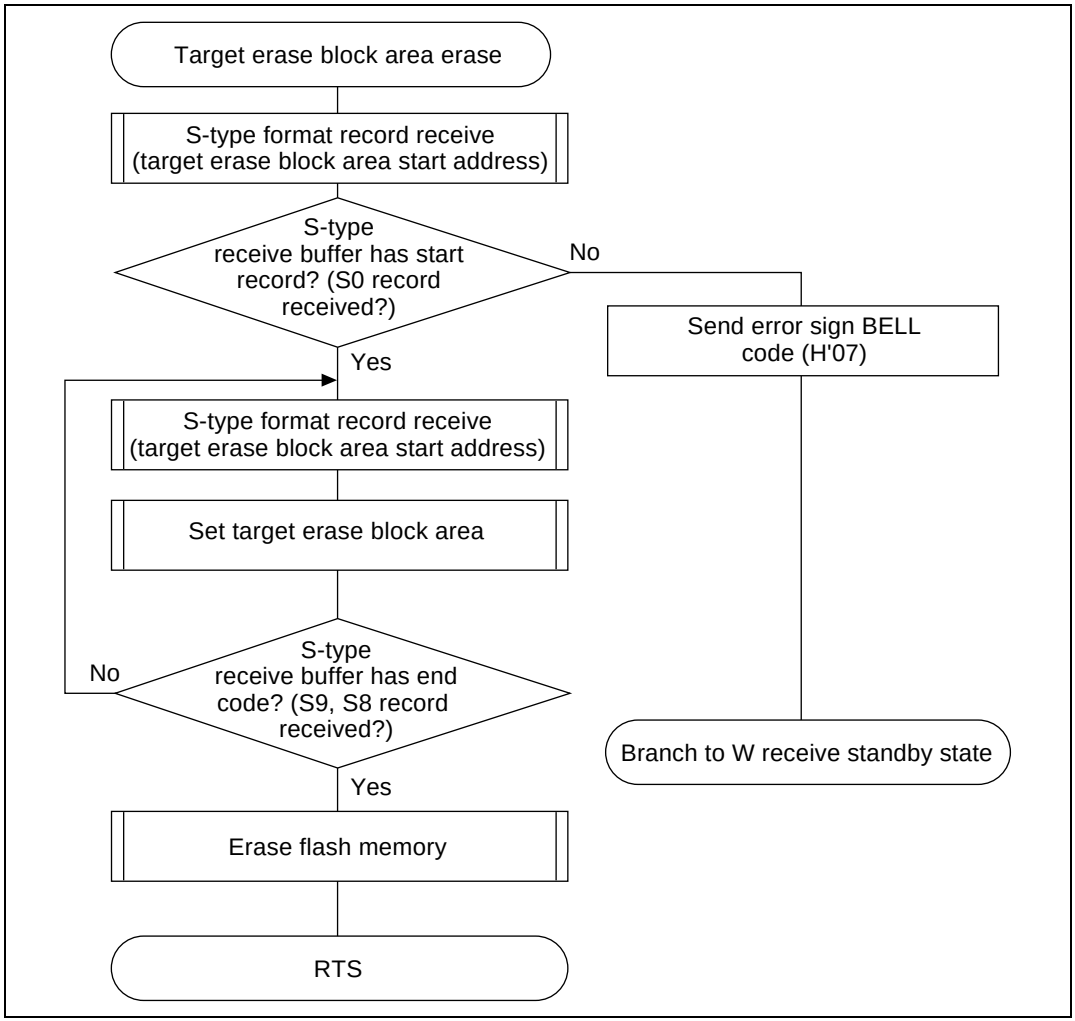


Figure 2.25 Target Erase Block Area Erase Flowchart

Figure 2.26 shows the S-type format record receive process.

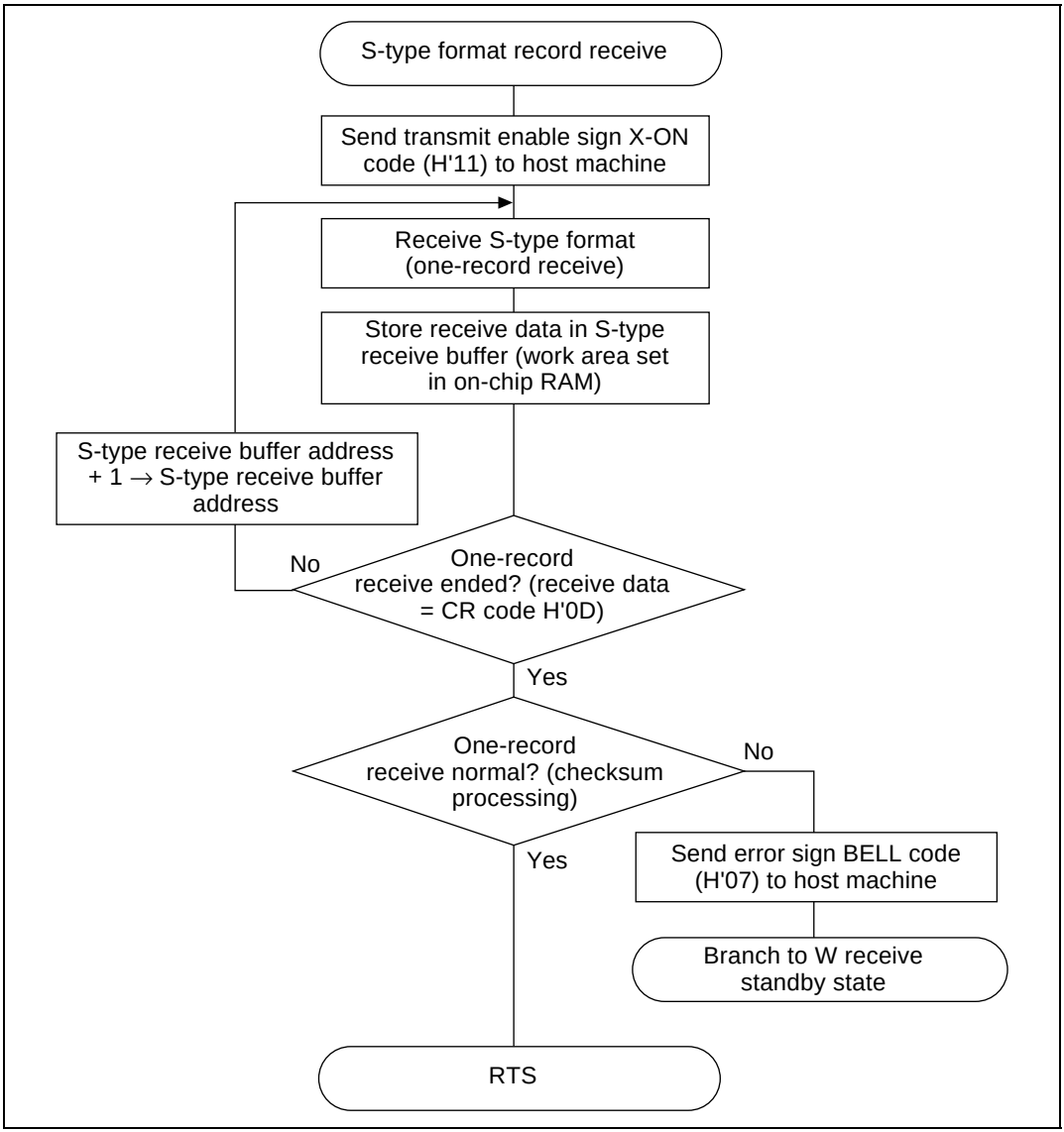


Figure 2.26 S-Type Format Record Receive Flowchart

Figure 2.27 shows how to set erase block registers (EBR1, EBR2) for received S-type format single record (target erase block start address).

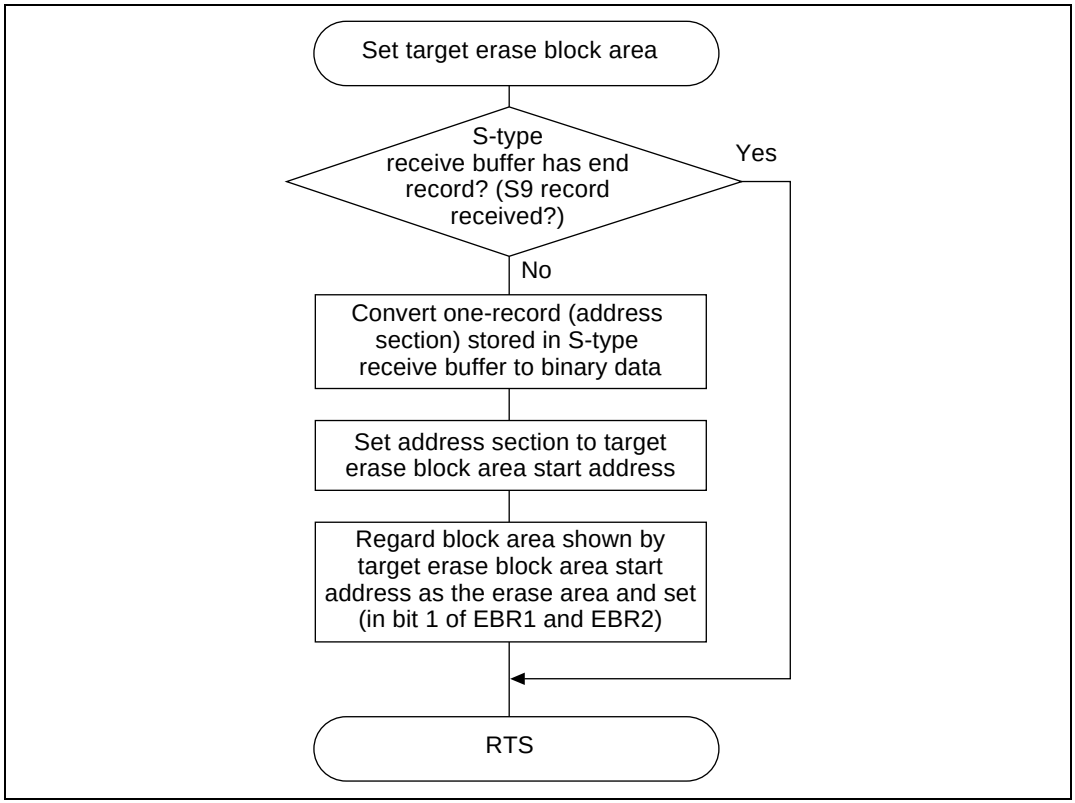


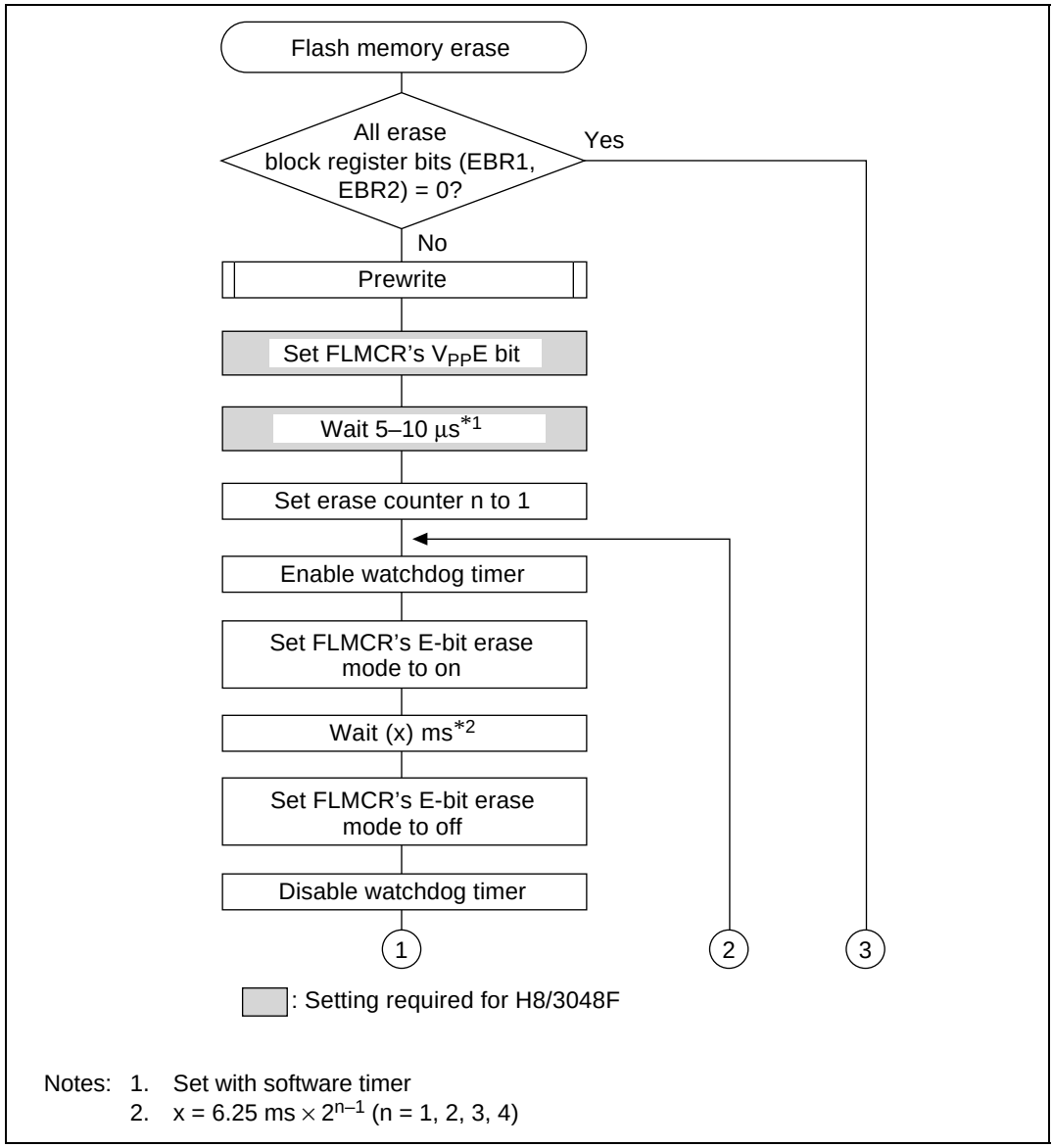
Figure 2.27 Set Target Erase Block Area Flowchart

Figure 2.28 shows how to erase the block area (indicated by a 1 in the erase block register) and conducts erase verify.

Set the timer's overflow cycle to the WDT overflow times listed in table 2.9.

Table 2.9 Overflow Cycles

Frequency	Value
10 MHz to 16 MHz	H'A57F
2 MHz to 10 MHz	H'A57F
1 MHz to 2 MHz (H8/3048F only)	H'A57D



Notes: 1. Set with software timer
2. $x = 6.25 \text{ ms} \times 2^{n-1}$ (n = 1, 2, 3, 4)

Figure 2.28 Flash Memory Erase (No. 1) Flowchart

Figure 2.29 shows the flash memory erase (no. 2) process.

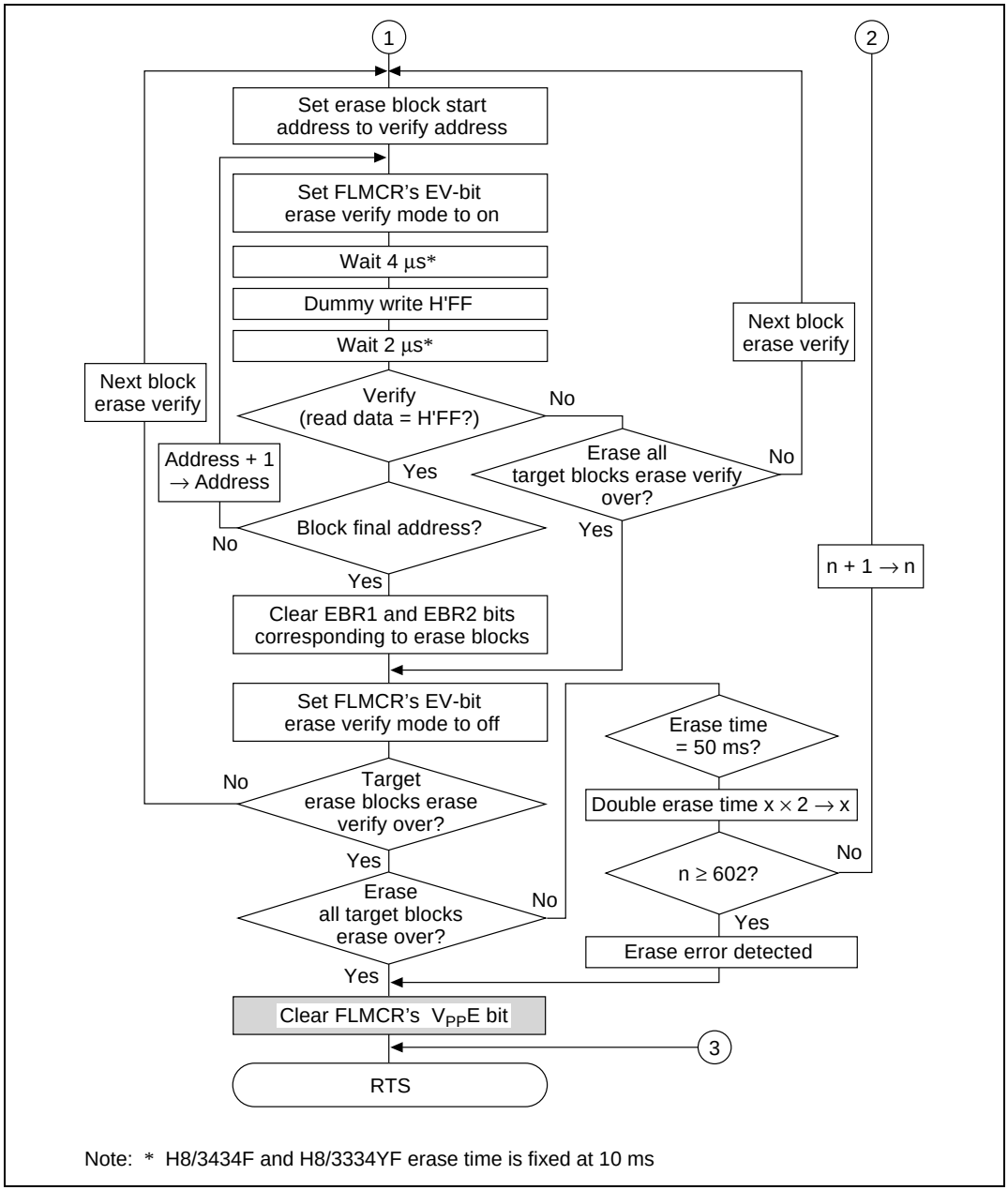
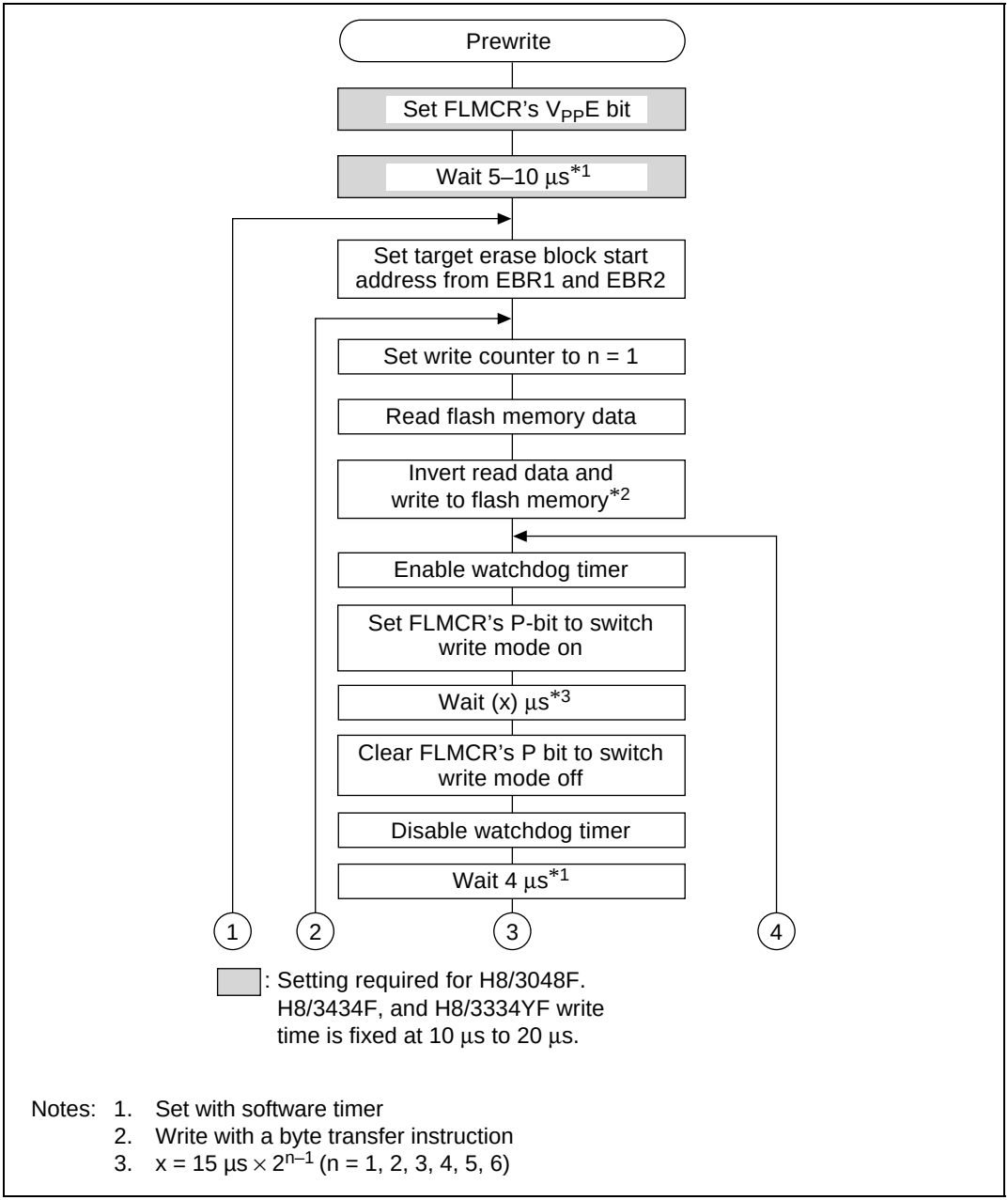


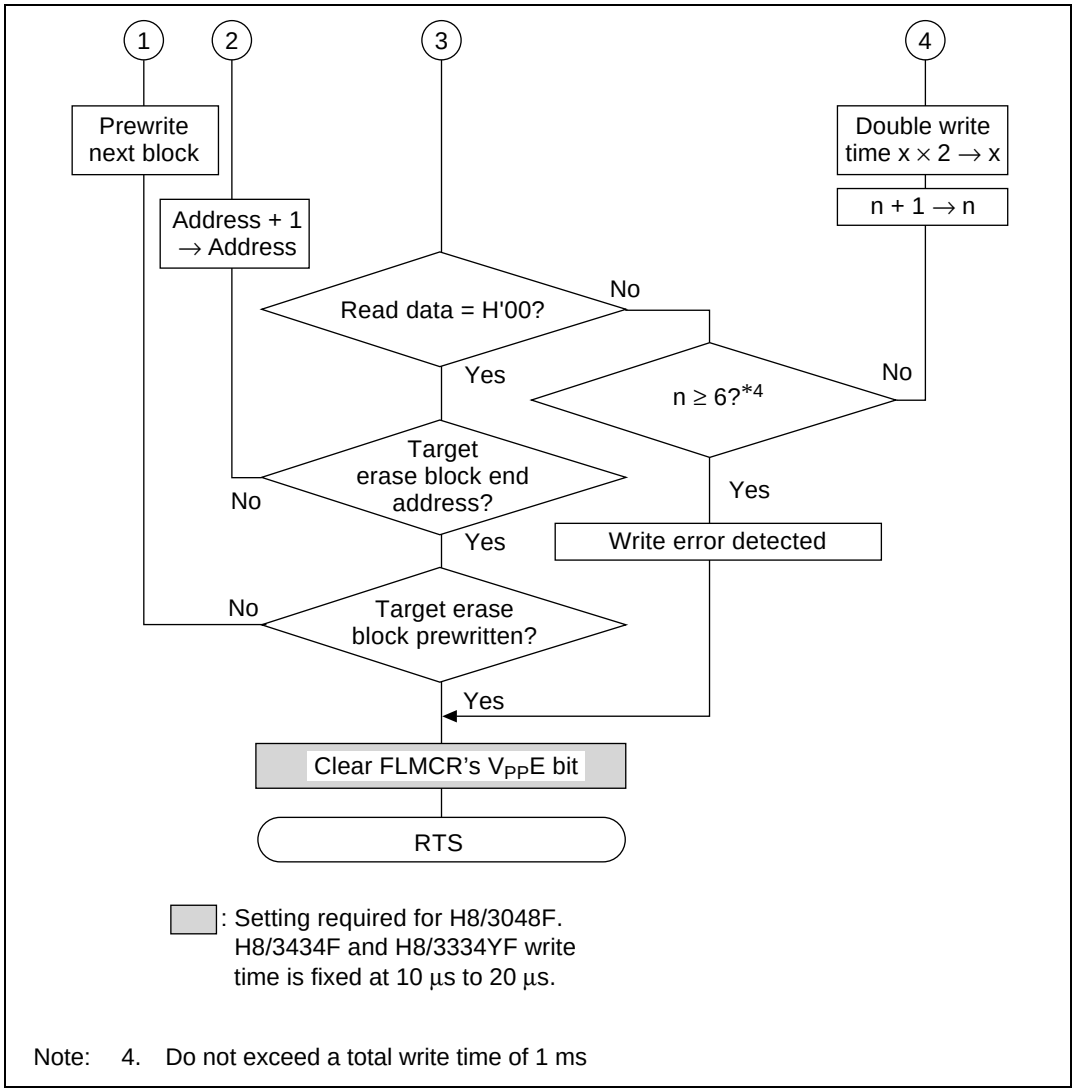
Figure 2.29 Flash Memory Erase (No. 2) Flowchart

Figure 2.30 shows how to write H'00 to the entire target erase block area.



Notes: 1. Set with software timer
2. Write with a byte transfer instruction
3. $x = 15\ \mu s \times 2^{n-1}$ (n = 1, 2, 3, 4, 5, 6)

Figure 2.30 Prewrite Flowchart



Note: 4. Do not exceed a total write time of 1 ms

Figure 2.30 Prewrite Flowchart (cont)

Figure 2.31 shows how to manage the application program write.

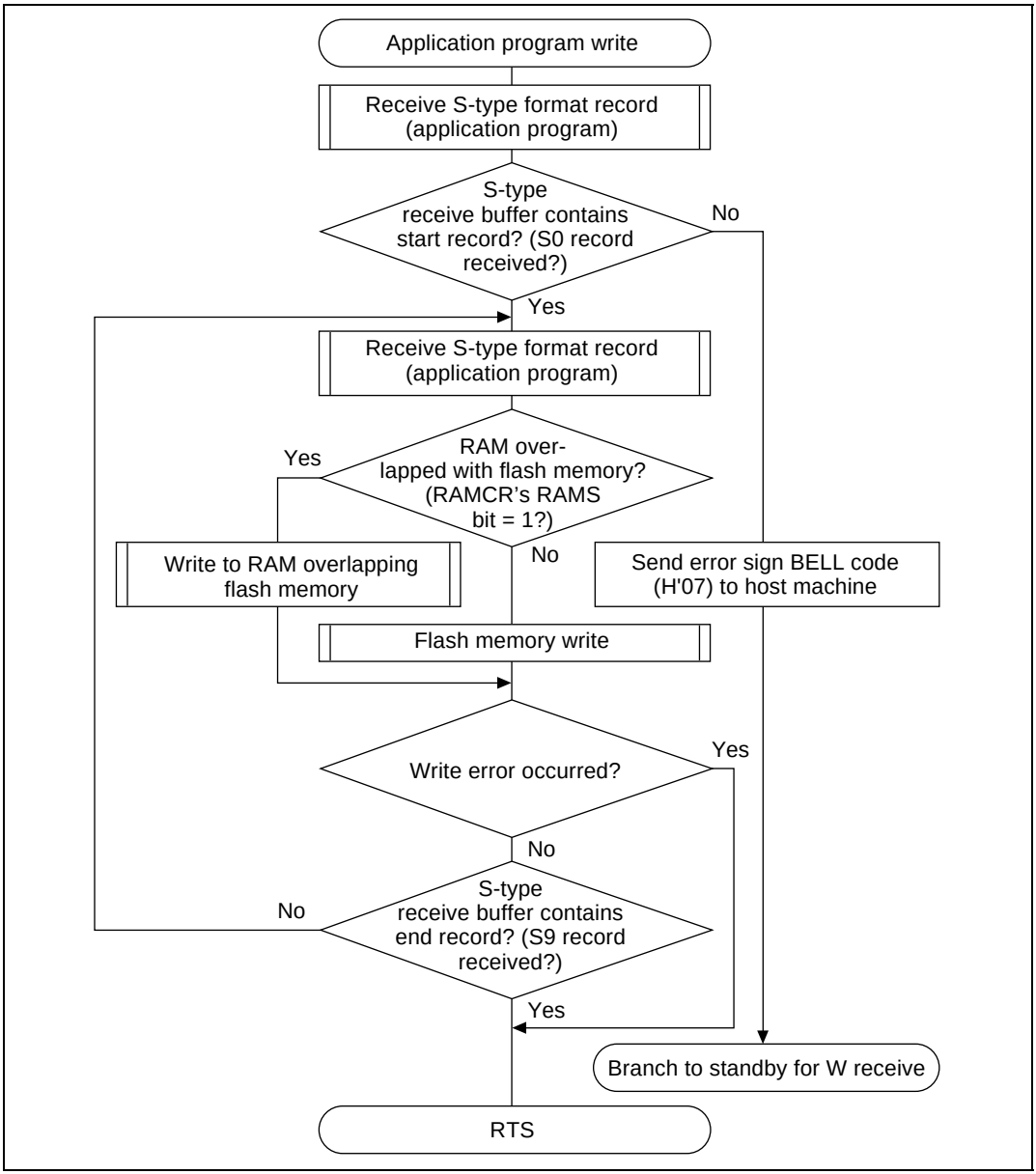


Figure 2.31 Application Program Write Flowchart

Figure 2.32 shows how to convert the application program in S-type format record buffer to binary data and writes it into flash memory.

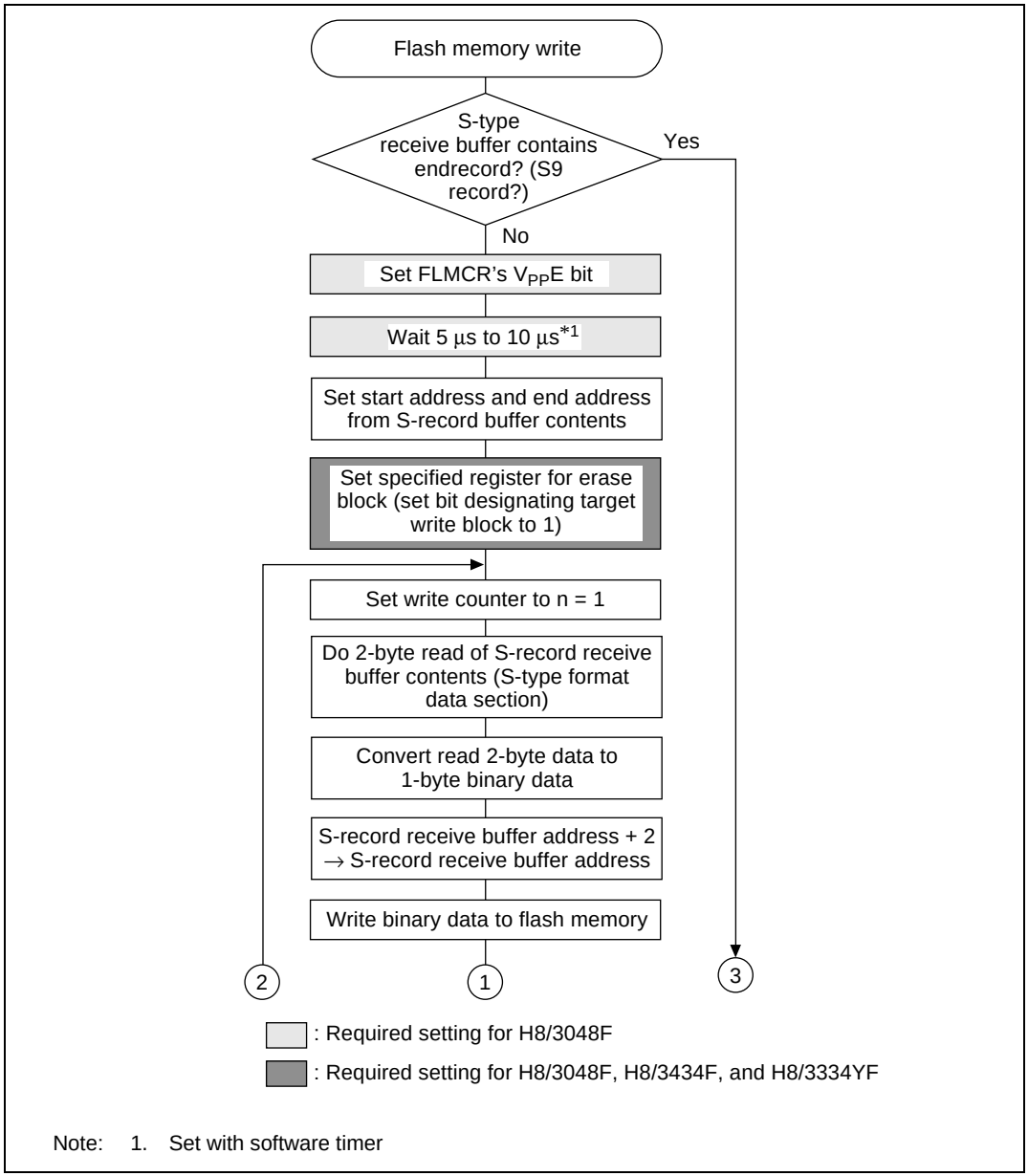
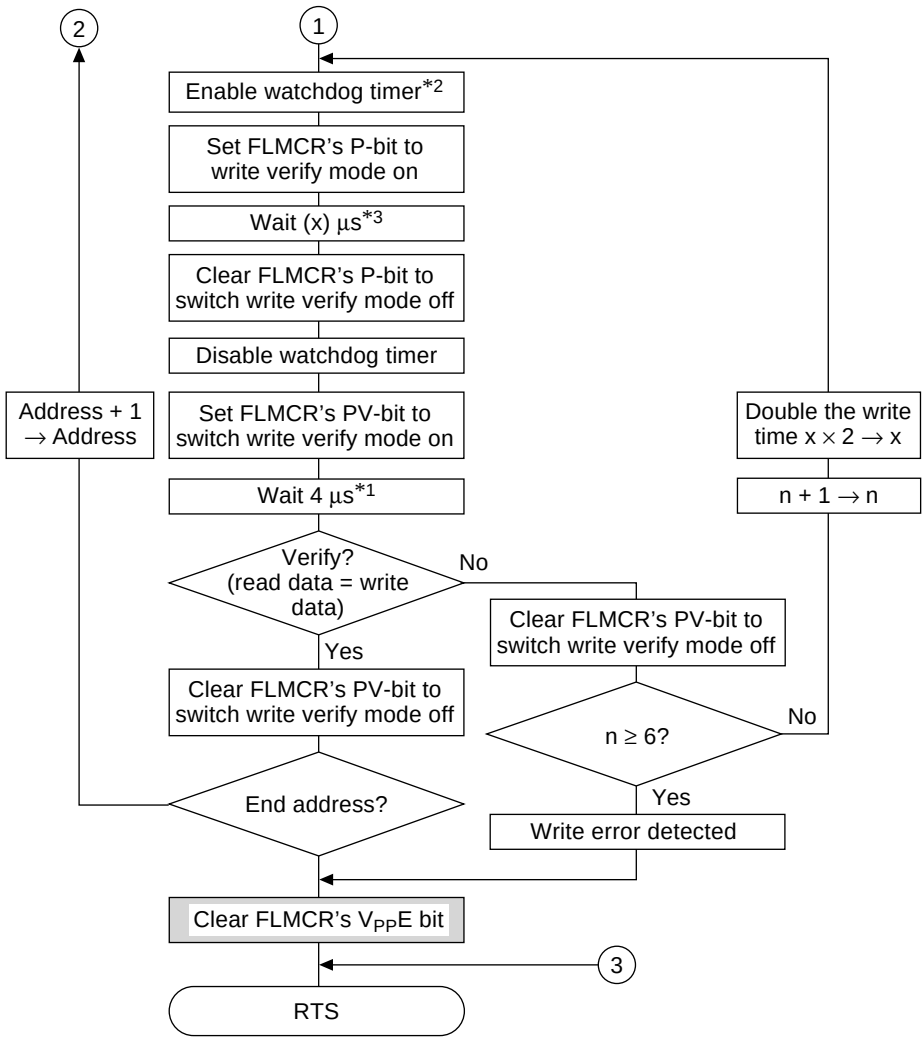


Figure 2.32 Flash Memory Write Flowchart



Notes: Setting required for H8/3434F and H8/3334YF write time is fixed at 10 to 20 ms
Overwrite required for H8/538F (products before June 95)

1. Set with software timer
2. Set timer overflow cycle (CKS2 = 0, CKS1 = 0, CKS0 = 1)
3. $x = 15\ \mu s \times 2^{n-1}$ (n = 1, 2, 3, 4, 5, 6)

Figure 2.32 Flash Memory Write Flowchart (cont)

Figure 2.33 shows how to write the application program to the RAM area emulating the flash memory area during flash memory emulation by RAM.

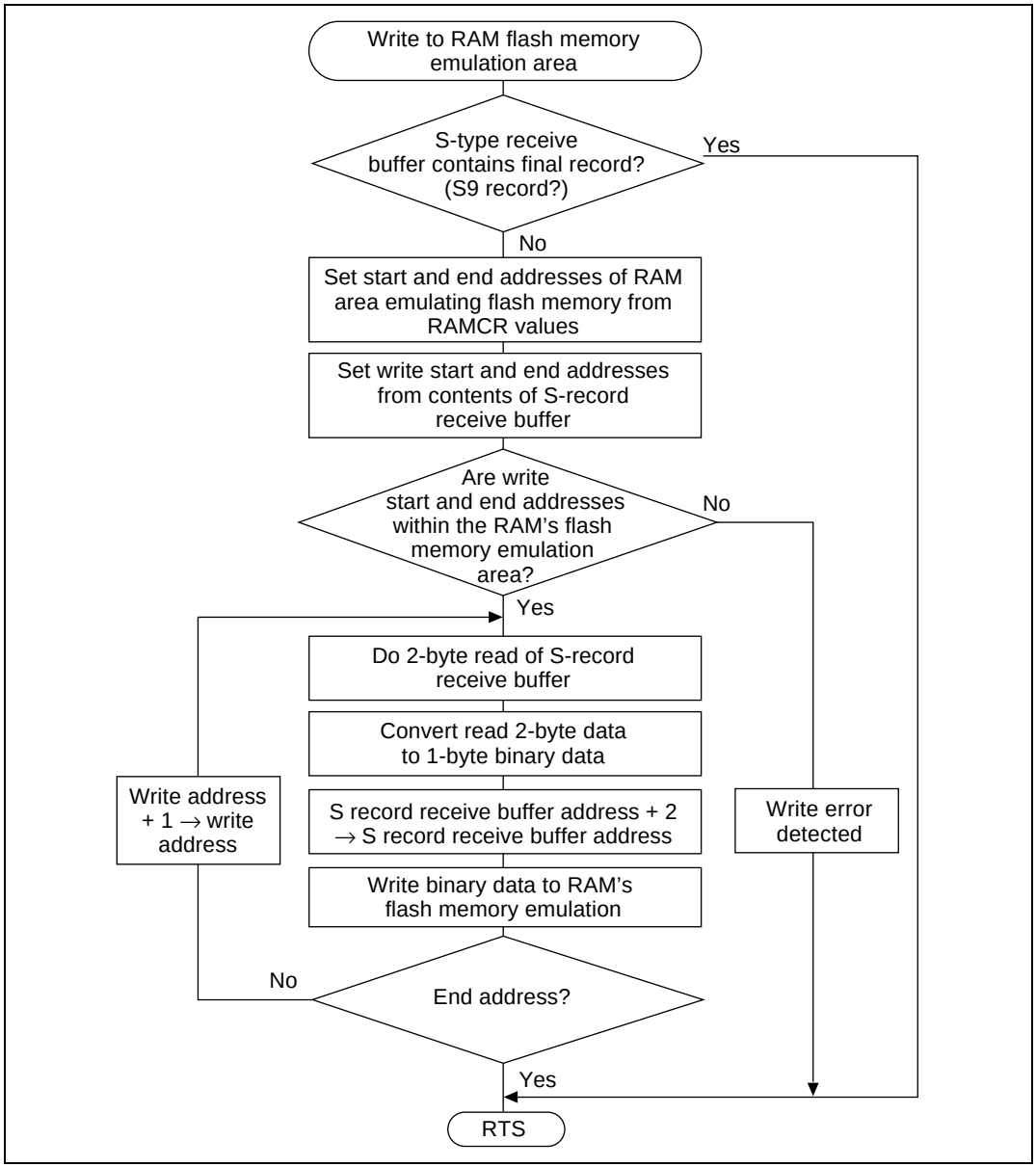


Figure 2.33 Write to RAM Overlapping Flash Memory Flowchart

Figure 2.34 shows how to set flash memory emulation by RAM.

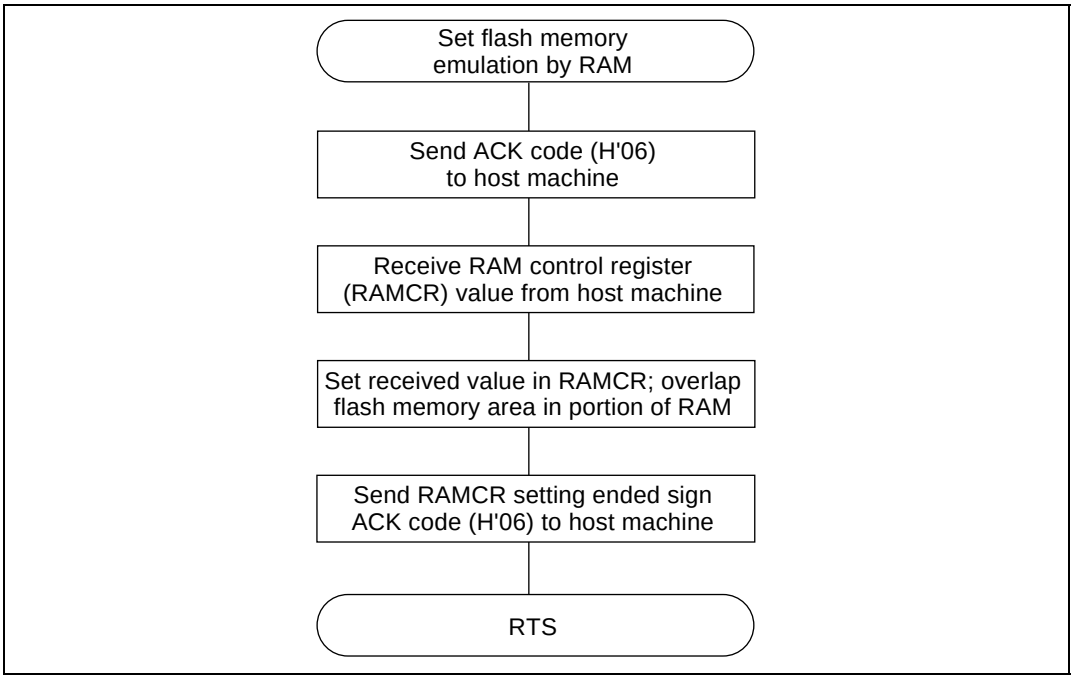


Figure 2.34 Set Flash Memory Emulation by RAM Flowchart

Section 3 Examples of Use with User Machine

3.1 User Machine for On-Board Programming

The type of circuitry shown in figure 3.1 is needed to conduct on-board programming/erasure for the F-ZTAT microcomputer in the user machine using the adapter board. Parts 1 to 3 in figure 3.1 are described in sections 3.1.1 to 3.1.3.

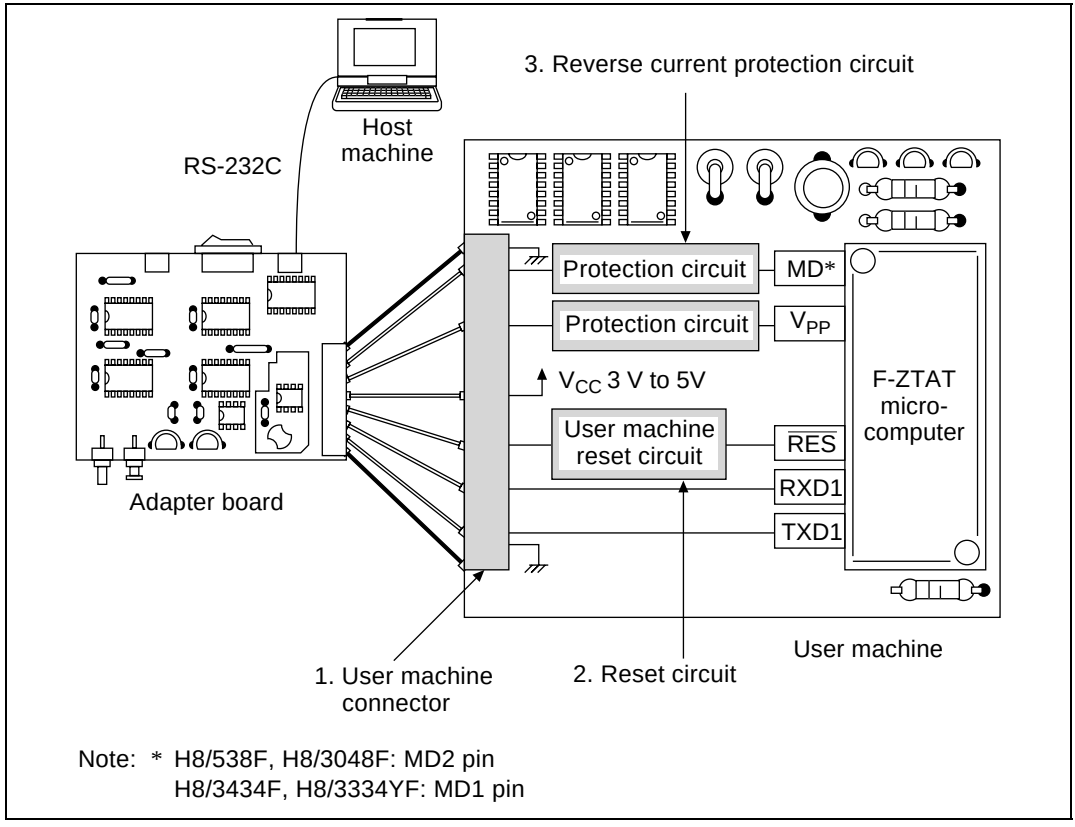


Figure 3.1 User Machine for On-Board Programming/Erasure

3.1.1 User Machine Connector

Attach the adapter board to the connector on the user machine as shown in figure 3.2.

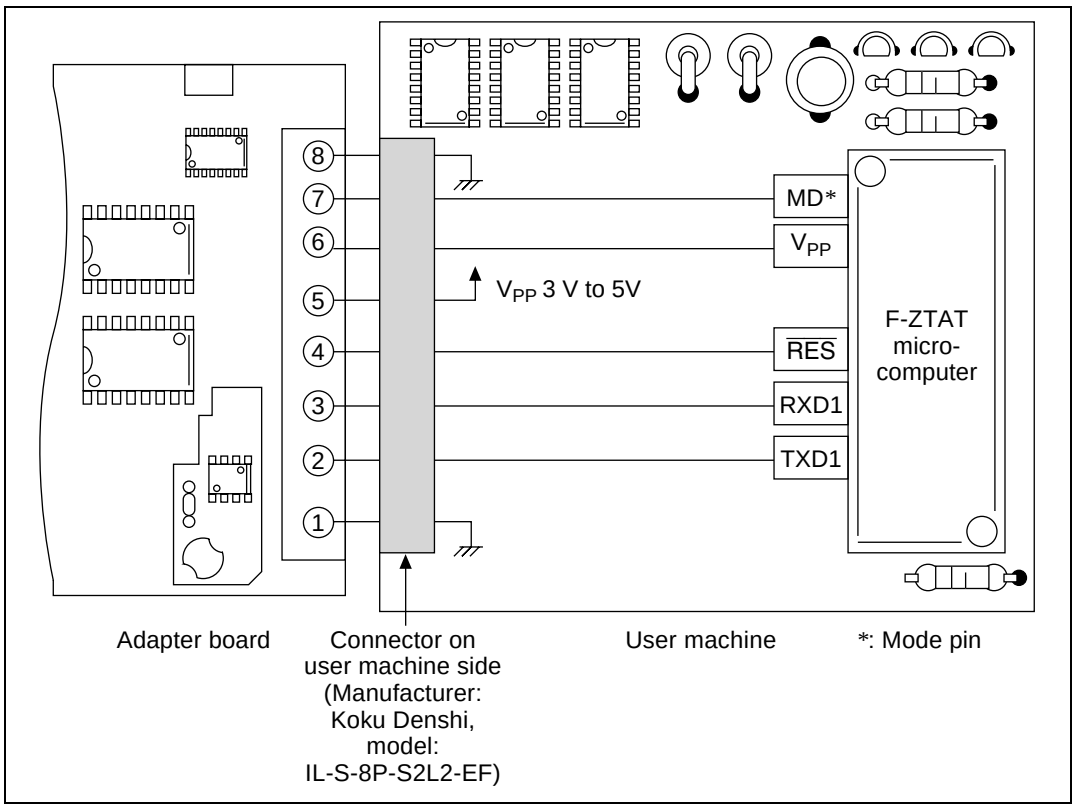


Figure 3.2 User Machine Connector Attachment

3.1.2 Reset Circuit

Connect the adapter board's reset pin to the user machine reset circuit as shown in figure 3.3.

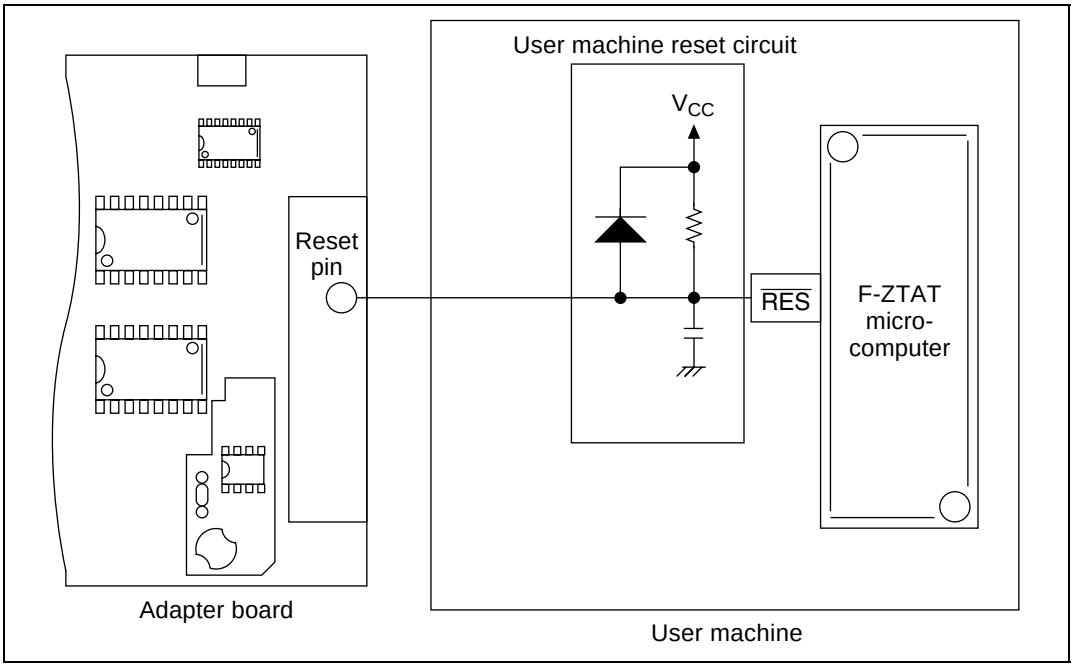


Figure 3.3 Reset Circuit

3.1.3 Reverse Current Prevention Circuit

When inserting a pull-up resistor at the F-ZTAT microcomputer's Vpp pin, it is necessary to insert a diode to prevent reverse current in the Vcc line when 12 V is applied from the adapter board (figure 3.4). The mode pin must also have a diode when a pull-up resistor is connected (mode pin set to 1) in order to set the microcomputer's operation mode. (When conducting a pull-down to GND (mode pin set to 0), insert the resistor and connect to GND.) Also connect a by-pass capacitor near the Vpp pin.

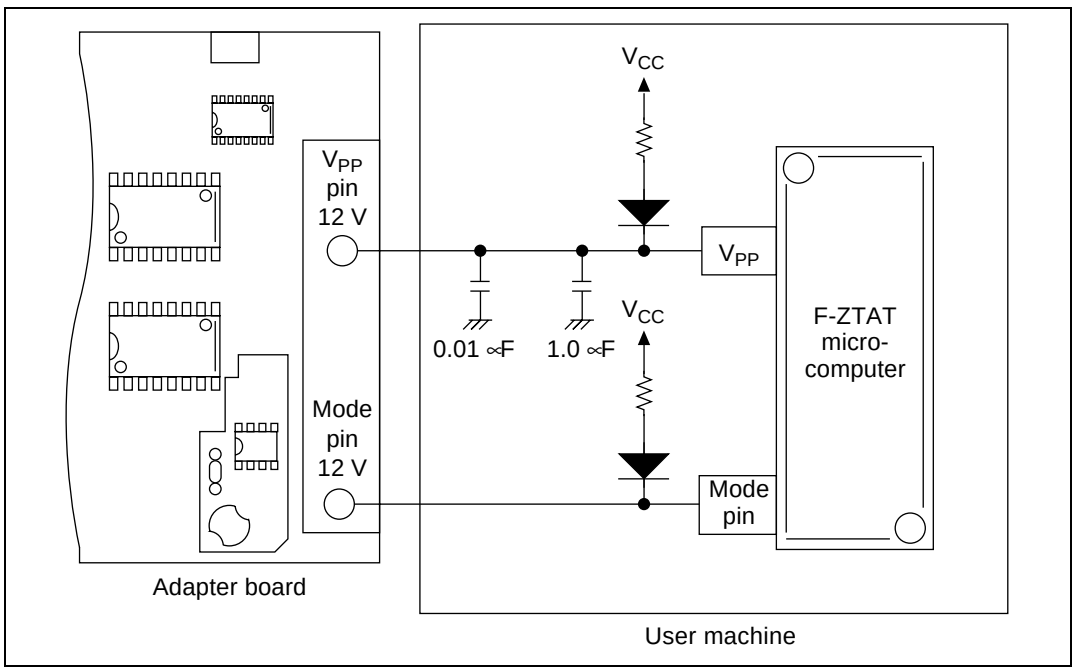


Figure 3.4 Reverse Current Prevention Circuit

Note: With the H8/538F and H8/3048F, the Vpp pin and WDT reset output ($\overline{\text{RESO}}$) are combined. Take care when using as a reset output pin, as a delay is caused in the reset output rise and fall due the effect of the pull-up resistor and by-pass capacitor connected to the Vpp pin.

3.2 SCI Switching Circuit Example

When conducting on-board programming in boot mode, the boot program loaded in the F-ZTAT microcomputer uses SCI channel 1 (TXD1, RXD1) to interface with the host machine. Employing SCI1 with the user system therefore requires an SCI1 switching circuit in the user machine. If you use SCI1 in user program mode, and employ PC I/F software and the adapter board, an SCI1 switching circuit is also required. The SCI switching circuit is detailed in sections 3.2.1 and 3.2.2.

3.2.1 SCI Switching Circuit Configuration

Figure 3.5 shows the SCI switching circuit configuration. During on-board programming, the circuit detects 12 V applied to the Vpp pin and switches from user system SCI to the programming SCI. At the end of a programming operation, the absence of 12 V at the Vpp pin is detected, and the circuit switches back from the programming SCI to user system SCI.

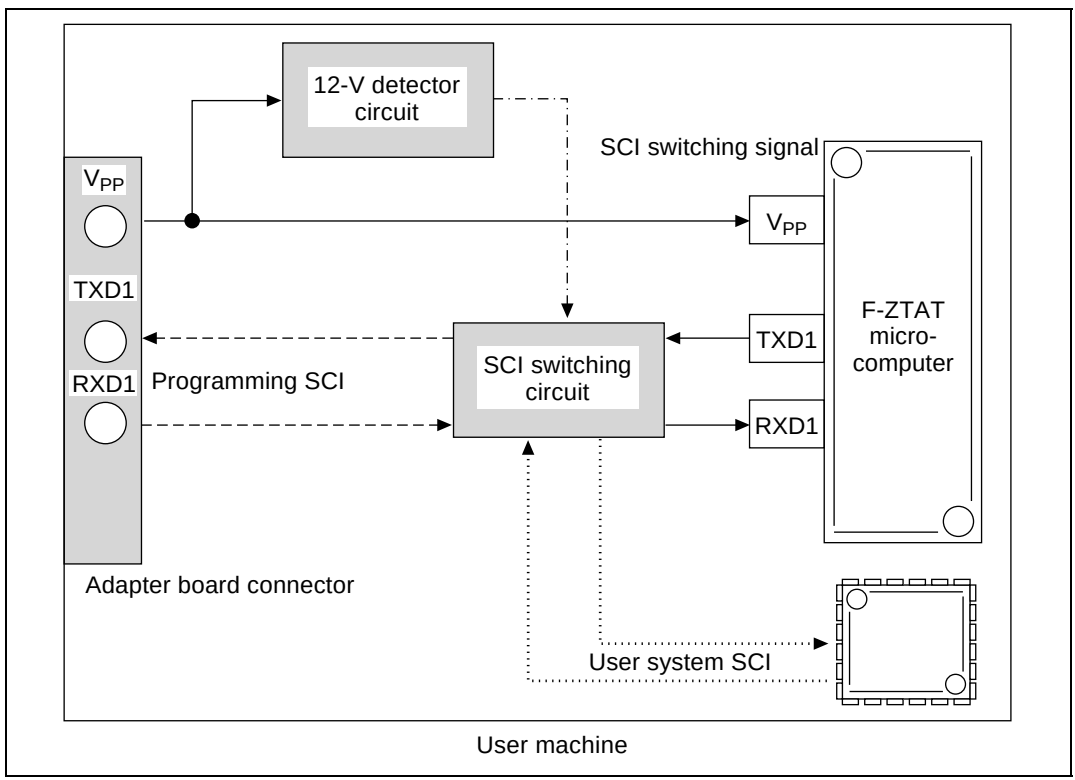


Figure 3.5 SCI Switching Circuit Configuration

3.2.2 SCI Switching Circuit Operation

Hardware Specification:

- Detects 12 V applied to the Vpp pin during on-board programming.
- On detecting 12 V, outputs SCI switching circuit switching signal.
- SCI switching circuit inputs switching signal to switch SCIs.

Circuit Diagram: Figure 3.6 shows the SCI switching circuit operating at Vcc = 5 V. The Vcc monitor ciruit and 12 V detection circuit are sample circuits based on Vcc= 5 V. If used with Vcc less than 5 V, therefore, the circuits will need to be revised.

If the H8/538F or H8/3048F Vpp pin is not used as the $\overline{\text{RESO}}$ pin by the user system, when the SCI switching circuit in the circuit example shown in figure 3.6 is configured, the Vpp pin should be connected to the 12 V detection circuit. (The Vcc monitor circuit need not be connected.)

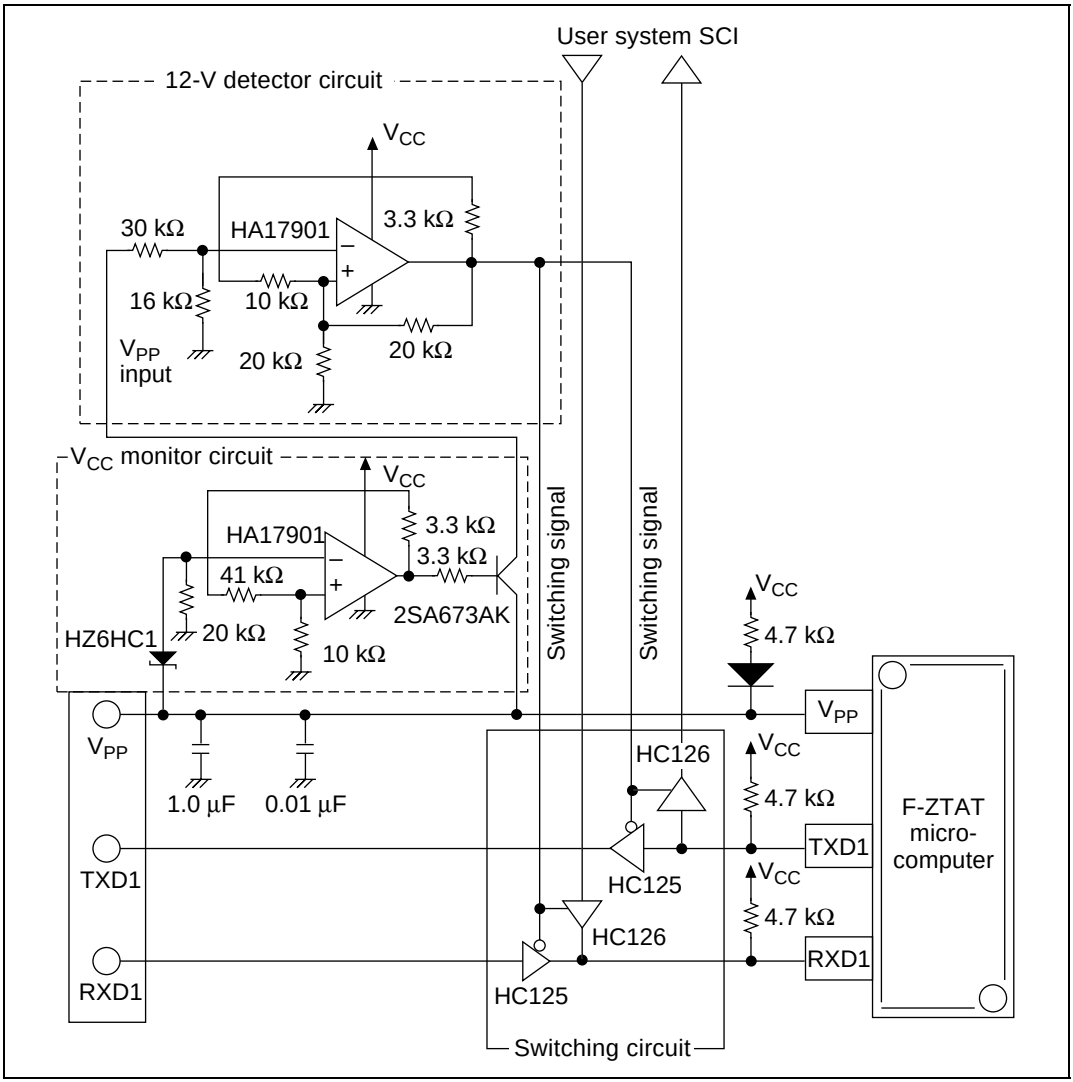


Figure 3.6 SCI Switching Circuit Diagram

Hardware Operation:

- The Vcc monitoring circuit outputs Vpp voltage to the 12-V detector circuit when 12 V is applied (approx. 6.5 V) to the Vpp pin.
- The 12-V detector circuit senses 12 V applied to the Vpp pin (approx. 10.9 V) and outputs a low level switching signal to the SCI switching circuit. When a voltage of about 7.6 V or less is detected, the circuit outputs a high level switching signal to the SCI switching circuit. Figure 3.7 shows the input/output characteristics of the 12-V detector circuit.

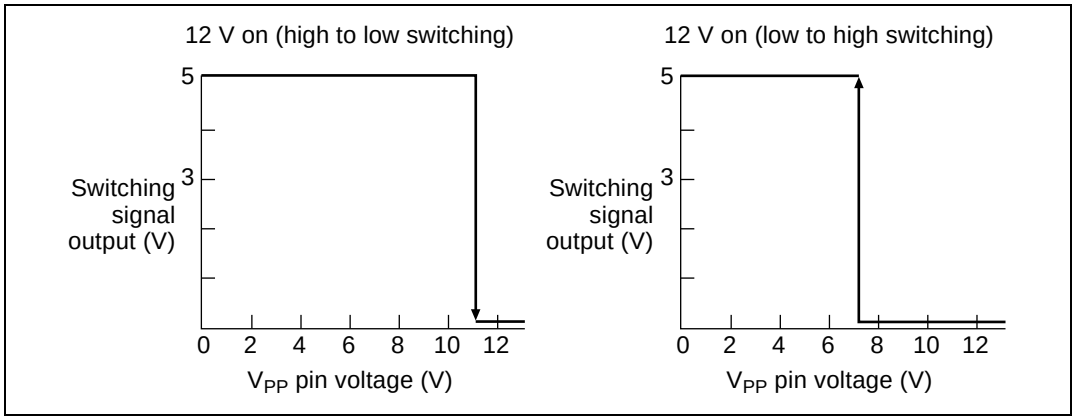


Figure 3.7 12-V Detector Circuit I/O Characteristics

- The SCI switching circuit inputs a switching signal from the 12-V detector circuit, and switches to the user system SCI if the level is high, and to the programming SCI if the level is low.

3.3 Reset Buffer Circuit Example

The reset buffer circuit switches between the signal from the reset switch in the user machine and the reset signal input from the adapter board during on-board programming. Figure 3.8 shows the reset buffer circuit configuration.

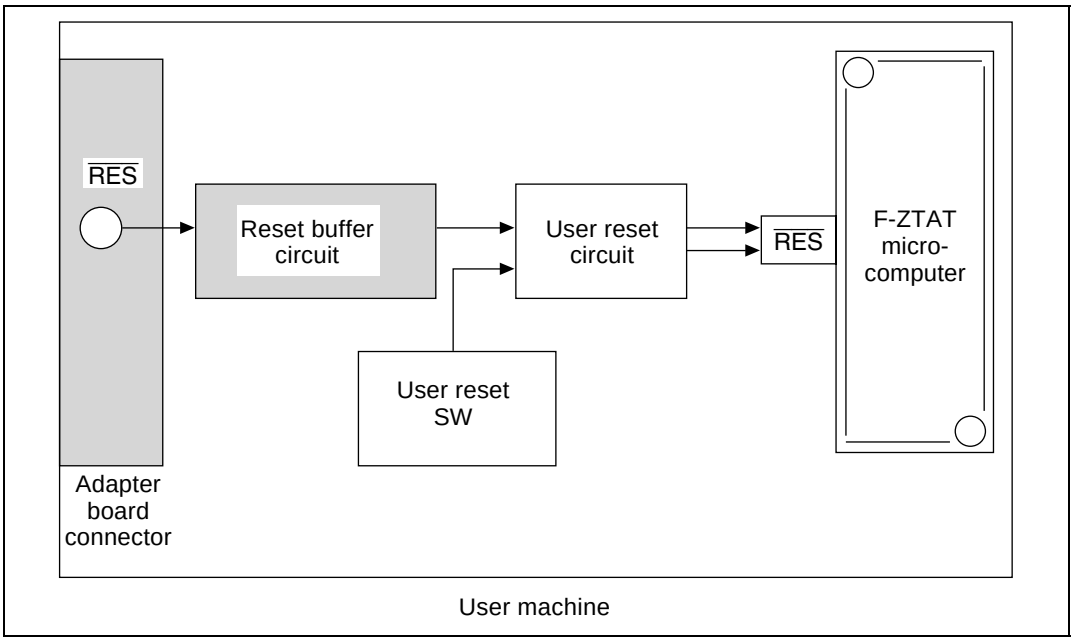


Figure 3.8 Reset Buffer Circuit Configuration

3.3.1 Reset Buffer Circuit Operation

Hardware Specification: Switches between reset signal from the adapter board and the user system reset signal.

Figure 3.9 shows the circuit diagram.

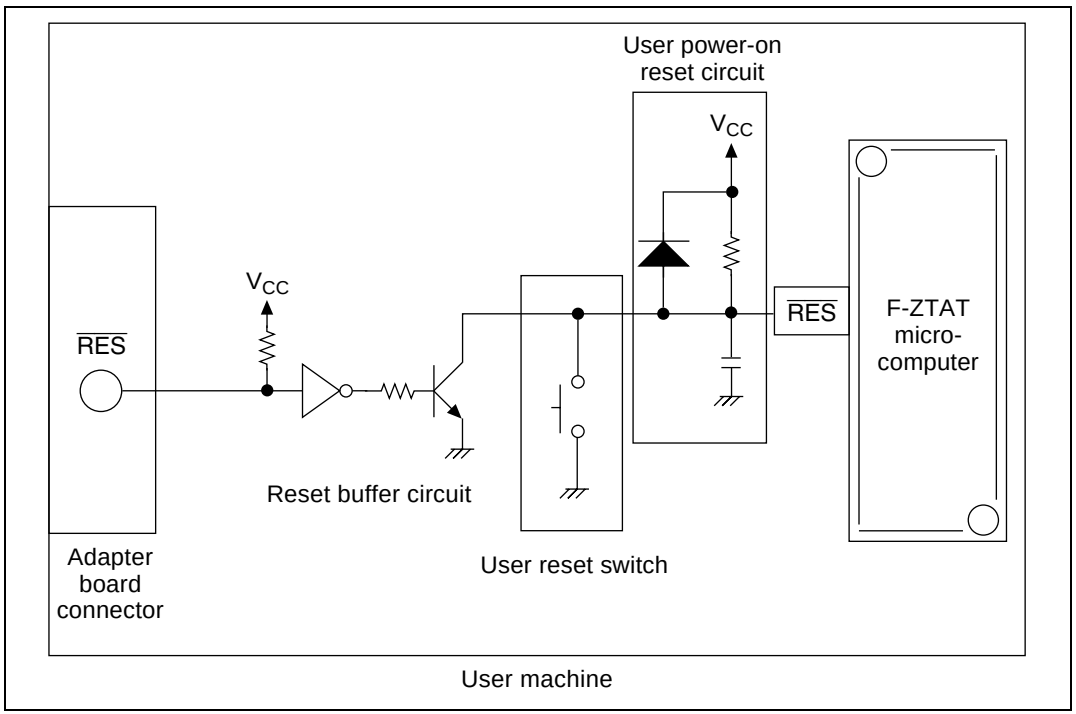


Figure 3.9 Reset Buffer Circuit Diagram

Hardware Operation: The reset buffer circuit inputs a reset signal from the adapter board and switches the F-ZTAT microcomputer's reset pin high and low by switching the base of the transistor (2SCI213) on/off (table 3.1).

Table 3.1 RESET Buffer Circuit Operation

Adapter Board Reset Signal Input	HC04 Output	Transistor On/Off	F-ZTAT Reset Pin
High	Low	Off	High
Low	High	On	Low
High impedance*	Low	Off	High

Note: * When adapter board and user machine are not connected.

Section 4 On-Board Programming Methods

4.1 On-Board Programming Methods

This section details the operation method when writing application programs to the F-ZTAT microcomputer in the user system employing boot mode and user program mode. For more information on the operation method for the adapter board and PC I/F software see the relevant user manual.

4.1.1 On-Board Programming Preparation

Connect the user machine and adapter board, and the host machine. See section 3.1, User Machine for On-Board Programming, for the connection method for the user machine and adapter board.

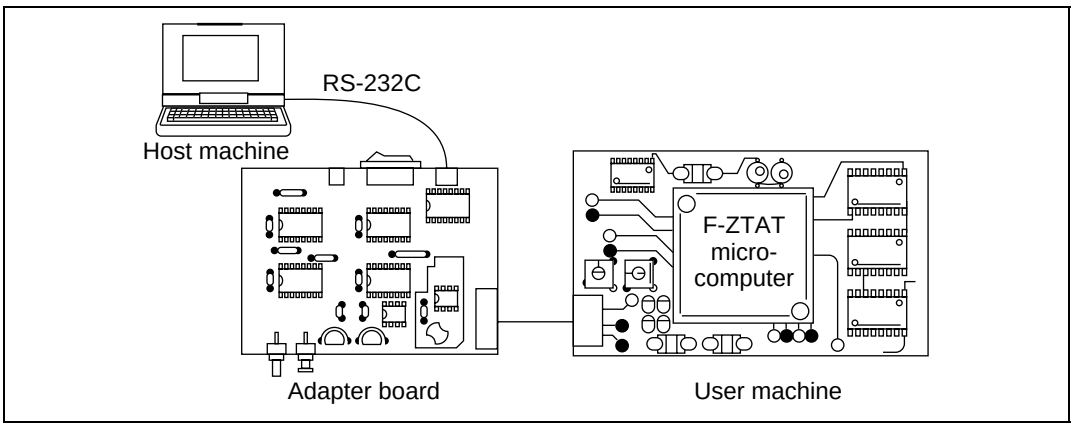


Figure 4.1 User Machine/Adapter Board and Host Machine Connections

Set the adapter board jumper pin to supply power to the adapter board either from the user side or from the 5-V (DC) supply. When supplying power from the 5-V (DC) connect to the 5-V (DC) connector on the adapter board.

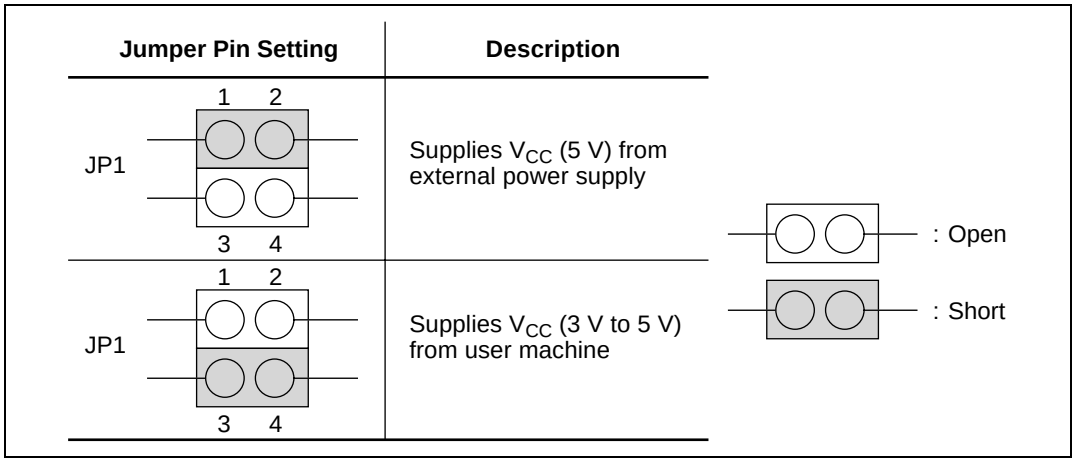


Figure 4.2 Jumper Pin Settings

Note: When you supply power to the adapter board from the user machine, note that the adapter board's current consumption is 500 mA (5-V supply) and 900 mA (3-V supply). Be sure to check the capacity of the power supplied.

4.1.2 Programming in Boot Mode

Programming in boot mode is described in steps 1 to 7 below. You will need the adapter board and PC I/F software (version 2.0).

1. Connect the user machine and adapter board and host machine. See section 4.1.1, On-Board Programming Preparation, for user machine/adapter board details.

2. Switch on the user machine power. When supplying adapter board power from an external source, switch on the adapter board power switch. The adapter board's POWER ON LED will light (green).

3. Set the adapter board's mode switch to boot mode (figure 4.3).

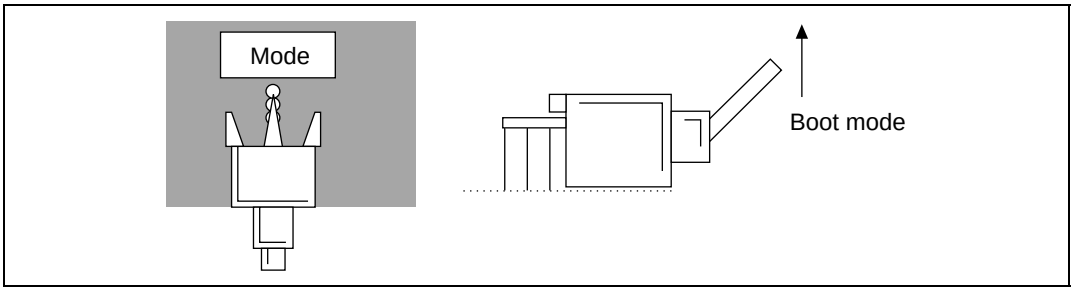


Figure 4.3 Programming Mode Switch Setting

4. Start the PC I/F software on the host machine. The PC I/F software operation method (1) for boot mode is shown below:

```
A>FLASH (RET) ---------------------------------------- (a)
F-ZTAT MICRO COMPUTER ON-BOARD PURGE/WRITE TOOL Ver2.0
Copyright(c) Renesas Technology Corp.
Licensed Material of Renesas Technology Corp.
Boot Program Mode (Y/N)?   Y------------------------- (b)
<User Board Setting in Boot Program Mode>------------- (c)
Charge 12 V at Vpp and MODE pin!
(Boot Program Mode)
And then release RESET signal.
Input any key!
```

Description:

a. Start up PC I/F software.

b. Enter Y for boot mode.

c. The hardware setting sequence for boot mode startup is displayed.

5. Press the adapter board's transfer switch to apply 12 V to the Vpp and mode pins. When 12 V is applied the adapter board's Vpp ON LED lights (red). The F-ZTAT microcomputer starts the boot program.

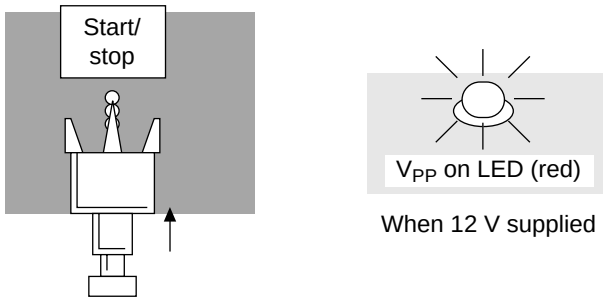


Figure 4.4 Programming Start Operation

6. Operate PC I/F software from the host machine. The PC I/F software operations (2) for boot mode is shown below:

```
Input any key!--------------------------- (a)
Send the Boot program to MCU------------- (b)
**************************** ----------------- (c)
Finish sending the User program!--------- (d)

: W FILENAME.MOT------------------------- (e)

Transfer data address OOOOXXXX----------- (f)
: Q               (RET)------------------ (g)
```

Description:

a. Input any key.

b. Display shows that automatic bit rate matching for the F-ZTAT microcomputer is under way and that the program/erase control program is being sent.

c. A string of asterisks (*) is displayed while the boot program erases all areas of flash memory.

d. Display shows that transfer of the program/erase control program to the F-ZTAT microcomputer is complete.

e. Input the application program filename using the W command.

f. Display shows that the application program is being transferred.

g. End PC I/F software with the Q command.

7. Press the adapter board's transfer switch to stop the 12-V supply to the Vpp pin and mode pin. The Vpp ON LED (red) goes off. The F-ZTAT microcomputer in the user machine starts the application program.

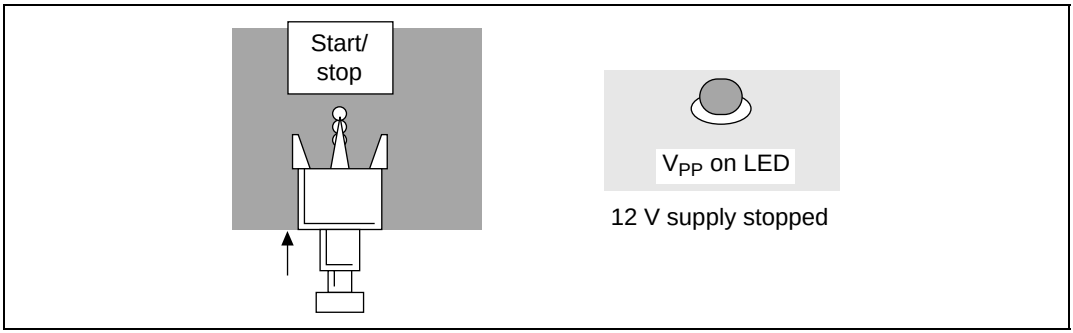


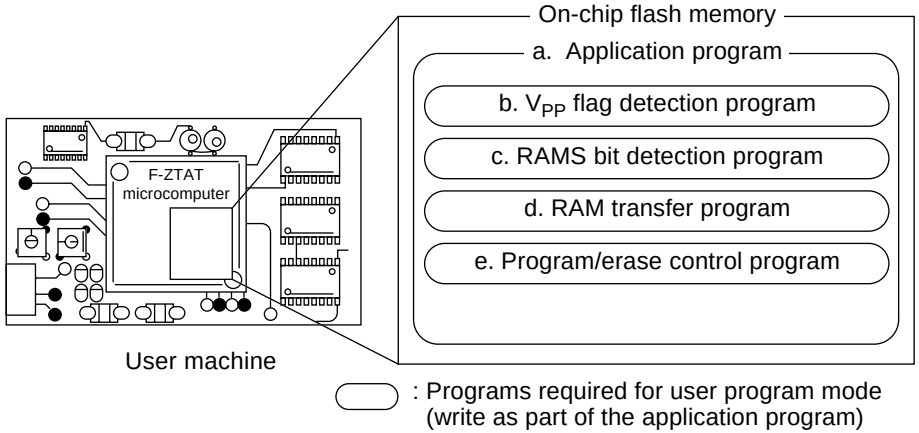
Figure 4.5 End of Programming Operation

4.1.3 User Program Mode Preparation

Preparation for user program mode with PC I/F software (version 2.0) is described in steps 1 to 4 below.

1. Programs required for user program mode

   The programs shown in figure 4.6 are needed for user program mode. First write these programs with the PROM writer in boot mode as part of the application program. Processing in each of the programs listed in figure 4.6 is described in figure 4.7.



Note: Programs required for user program (write as part of the application program).

Figure 4.6 Programs Required for User Program Mode

Description:

a. Application program: Controls the user system (program the user creates)

b. Vpp flag detection program: Detect the Vpp flag in the flash memory control register (FLMCR) (Vpp = 12 V) created by user.

c. RAMS bit detection program: Detects RAMS bit in the RAM control register (RAMCR) signifying that the flash memory emulation by RAM application program is running. (Created by user.) This is not required when not using flash memory emulation by RAM. Note that PC I/F software cannot be used with the H8/3434 and H8/3334YF in flash memory emulation by RAM since the RAM area for transfer of the program/erase control program is too small.

d. RAM transfer program: Transfers the program/erase control program to RAM during user program mode startup (created by user).

e. Program/erase control program: Controls receiving of application programs operating in RAM and write/erase to flash memory during user program mode (program controlling write/erase operations of PC I/F software).

2. User program mode startup procedure: Figure 4.7 shows this procedure.

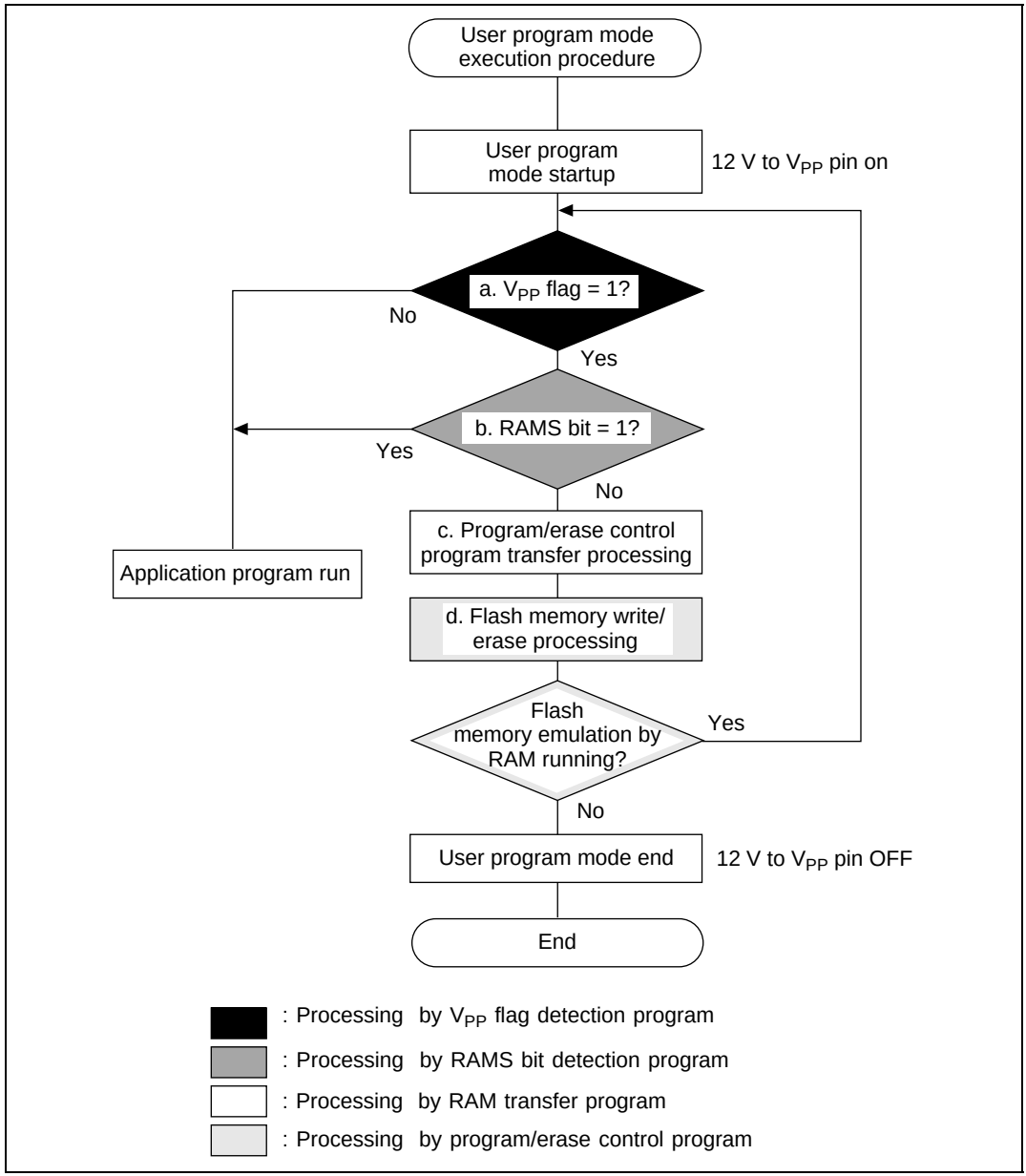


Figure 4.7 User Program Mode Startup Procedure

Description:

a. The Vpp flag detection program detects the Vpp flag in the flash memory control register (FLMCR). User program mode is started up when the Vpp flag = 1 (Vpp pin = 12 V).

b. The RAMS bit detection program detects the RAMS bit in the RAM control register (RAMCR). If the RAMS bit = 1, the application program to check parameters and other data in flash memory emulation by RAM is started up. (In the case of H8/3434F and H8/3334YF, it is necessary to perform a logical OR on the RAMS bit and RAM0 bit in addition to checking the RAMS bit.) Note that this is only required during flash memory emulation by RAM. PC I/F software cannot be used with the H8/3434F and H8/3334YF in flash memory emulation by RAM since the RAM area for transfer of the program/erase control program is too small.

c. The RAM transfer program transfers the PC I/F software program/erase control program written in flash memory to RAM. After transfer, the program/erase control program in RAM is started up. The PC I/F software program/erase control program operates in the F-ZTAT microcomputer's on-chip RAM area (RAM area for transfer of the program/erase control program during boot mode). When transferring the program/erase control program to the RAM area during user program mode, transfer to the on-chip RAM area (e.g., when operation mode = 7, operation is at RAM area addresses H'FF300 to H'FFF0F.)

d. The program/erase control program erases the flash memory block area to which you are writing the application program, receives the application program from the host machine, and writes it to flash memory. When running flash memory emulation by RAM, the control program overlaps a portion of RAM to flash memory (RAMCR setting), writes the application program received from the host machine, and then starts up the application program.

3. Transfer rate setting

   In user program mode, set the F-ZTAT microcomputer transfer rate (SCI ch1) with the RAM transfer program or program/erase control program. The host machine can be set to 9600, 4800, and 2400 bps.

4. Writing program/erase control program to flash memory

   The write address for the PC I/F software program/erase control program is fixed in the F-ZTAT microcomputer's on-chip RAM area (in boot mode, the RAM area for transfer of the program/erase control program). Therefore, when writing the program/erase control program to flash memory with PC I/F software, it is necessary to specify an offset (change the write address to an address in flash memory). The following is a description of how to write to flash memory the program/erase control program for the H8/3048F. With the H8/3048F (operation mode = 7), the write address of the on-chip RAM area is H'FF300 to H'FFF0F. For details of the write method in boot mode, please refer to section 4.1.2, Programming in Boot Mode.

```
Boot Program Mode (Y/N)?   Y
<User Board Setting in Boot Program Mode>
Charge 12 V at Vpp and MODE pin!
(Boot Program Mode)
And then release RESET signal.
Input any key!
Send the Boot program to MCU
****************************
Finish sending the User program!

:W USER.MOT (RET)------------------------ (a)

Transfer data address 0000XXXX

:O FFF20700 (RET)------------------------ (b)
:W FLASH.SUB (RET)----------------------- (c)

Transfer data address 0000XXXX

:Q--------------------------------------- (d)
```

Description:

a. Input the filename of the application program with the W command.

b. Specify the write address offset with the O command. In this case the program/erase control program write address changes to flash memory address H'1FA00. Specify the offset 32-bit hexadecimal code.

Example: H'000FF300 + offset = H'0001FA00
offset = H'0001FA00 to H'000FF300
= H'FFF20700 (2's complement)

c. Enter the program/erase control program filename with the W command.

d. End PC I/F software operation with the Q command.

4.1.4 Programming in User Program Mode

Programming in user program mode is described in steps 1 to 7 below. You will need the adapter board and PC I/F software (version 2.0).

1. Connect the user machine and adapter board and host machine. See section 4.1.1, On-Board Programming Preparation, for user machine to adapter connection board details.

2. Switch on the user machine power. When supplying adapter board power from an external source, switch on the adapter board power switch. The adapter board's POWER ON LED will light (green).

3. Set the adapter board's mode switch to user program mode (figure 4.8).

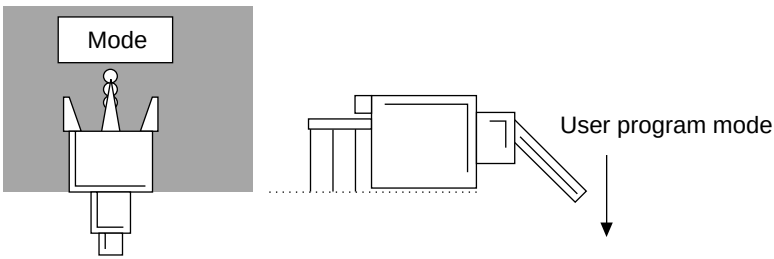


Figure 4.8 Programming Mode Switch Setting

4. Start the PC I/F software on the host machine. The PC I/F software operation method (1) for user program mode is as follows:

```
A>FLASH (RET) ---------------------------------------- (a)
F-ZTAT MICRO COMPUTER ON-BOARD PURGE/WRITE TOOL Ver2.0
Copyright(c) Renesas Technology Corp.
Licensed Material of Renesas Technology Corp.
Boot Program Mode (Y/N)?   N------------------------- (b)

<User Board Setting in Boot Program Mode>------------ (c)
Charge 12 V at Vpp and MODE pin!
(User Program Mode)
Input any key!
```

Description:

a. Start up PC I/F software.

b. Enter No (N) to select user program mode.

c. The hardware setting sequence for user program mode startup is displayed.

5. Press the adapter board's transfer switch to supply 12 V to the Vpp pin. The adapter board's Vpp on LED (red) lights at this time. The F-ZTAT microcomputer goes into user program mode (figure 4.9).

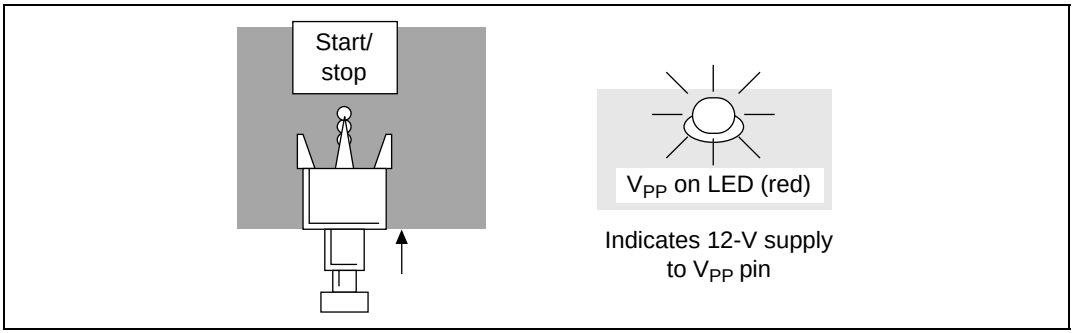


Figure 4.9 Start Programming Operation

6. Operate PC I/F software on the host machine. The PC I/F software operation method in user program mode (2) is as follows:

```
BAUDRATE  (1:9600 2:4800 3:2400) 1------------ (a)
Input any key!-------------------------------- (b)
: W FILENAME.MOT------------------------------ (c)

Erase Block address 00000000–00003FFF(Y/N)?Y--- (d)
                :
                :
Transfer data address 0000XXXX---------------- (e)
: Q ------------------------------------------ (f)
```

Description:

a. Set the host machine transfer rate. In this case the transfer rate is 9600 bps.

b. Enter any key. The host machine goes to command input state.

c. Enter the filename of the application program with the W command.

d. Enter Y. Select erase for the flash memory block area you want to write the application program to. During user program mode, the flash memory is erased by the program/erase control program.

e. A "Sending application program" message is displayed.

f. End PC I/F software operation with the Q command.

7. Press the adapter board's transfer switch to stop the 12-V supply to the Vpp pin and mode pin. The Vpp ON LED (red) goes off (figure 4.10). The F-ZTAT microcomputer in the user machine starts the application program.

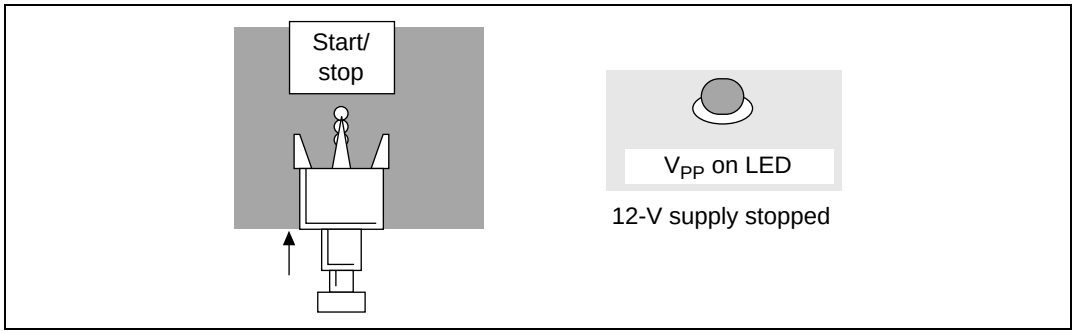


Figure 4.10 End of Programming Operation

4.1.5 Operation Method for Flash Memory Emulation by RAM

The operation method for flash memory emulation by RAM in user program mode is described in 1 to 10 below, using H8/3048 as an example. You will need the adapter board and PC I/F software (version 2.0).

1. Connect the user machine and adapter board and host machine. See section 4.1.1, On-Board Programming Preparation, for user machine to adapter connection board details.

2. Switch on the user machine power. When supplying adapter board power from an external source, switch on the adapter board power switch. The adapter board's POWER ON LED will light (green).

3. Set the adapter board's mode switch to user program mode (figure 4.11).

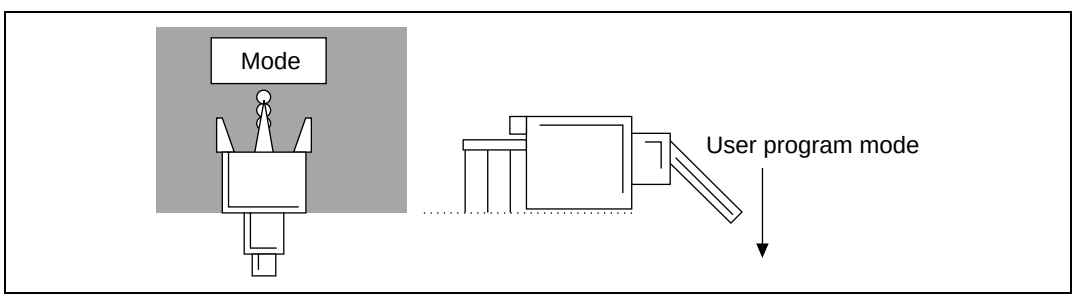


Figure 4.11 Programming Mode Switch Setting

4. Start the PC I/F software on the host machine. The PC I/F software operation method (1) for flash memory emulation by RAM is as follows:

```
A>FLASH (RET) ---------------------------------------- (a)
F-ZTAT MICRO COMPUTER ON-BOARD PURGE/WRITE TOOL Ver2.0
Copyright(c) Renesas Technology Corp.
Licensed Material of Renesas Technology Corp.
Boot Program Mode (Y/N)?   N------------------------- (b)

<User Board Setting in Boot Program Mode>------------- (c)
Charge 12 V at Vpp pin!
(User Program Mode)
Input any key!
```

Description:

a. Start up PC I/F software.

b. Enter N to select user program mode.

c. The hardware setting sequence for user program mode startup is displayed.

5. Press the adapter board's transfer switch to supply 12 V to the Vpp pin. The adapter board's Vpp ON LED (red) lights at this time (figure 4.12). The F-ZTAT microcomputer goes into user program mode.

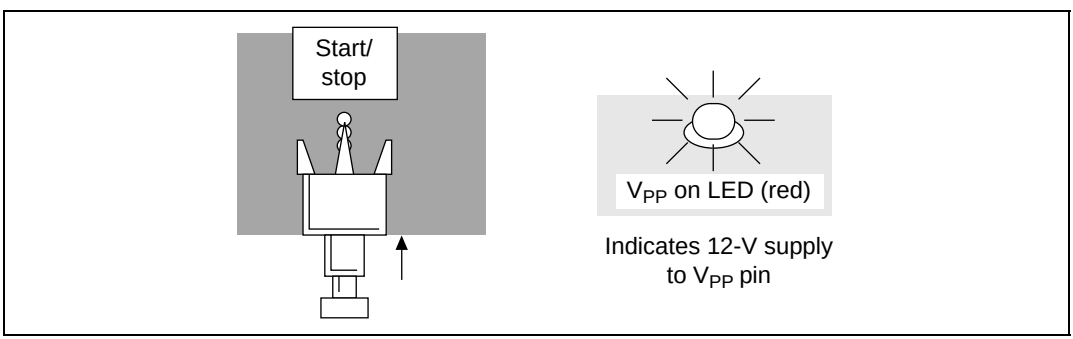


Figure 4.12 Transfer Switch Operation

6. Operate PC I/F software on the host machine. The PC I/F software operation method in flash memory emulation by RAM (2) is as follows:

```
BAUDRATE  (1:9600 2:4600 3:2400) ?1 (RET)------------ (a)
Input any key!-------------------------------------- (b)
: R (RET)------------------------------------------- (c)
RAM Emulation 0001F000 0001F1FF (Y/N) ?Y------------- (d)

: W FILENAME.MOT 1F000 1F1FF (RET)------------------------(e)
Transfer data address 0000XXXX----------------------------(f)
:
```

Description:

a. Set the host machine transfer rate. In this case the transfer rate is 9600 bps.

b. Enter any key. The host machine goes to command input state.

c. Overlap flash memory and portion of RAM with the R command.

d. Input Y to overlap flash memory area addresses H'1F000 to H'1F1FF in a portion of RAM (H8/3048F sets RAMCR).

e. Enter the application program with the W command, and write data to addresses H'1F000 to H'F1FF. (Note: During flash memory emulation by RAM, data write is only valid for the flash memory area overlapping the RAM portion.)

f. A “Sending application program” is displayed sent to addresses H'1F000 to H'F1FF. The write operation takes up a portion of the overlapped RAM.

7. The F-ZTAT microcomputer in the user machine starts the application program when the Vpp pin has 12 V supplied to it (figure 4.13).

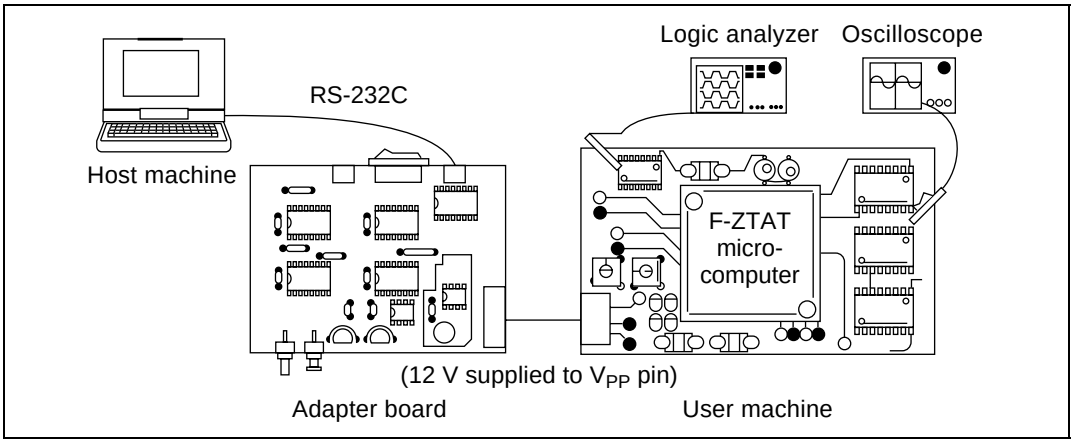


Figure 4.13 Application Program Startup

8. When changing or fixing data, and writing overlapping RAM contents to flash memory, reset the F-ZTAT microcomputer in the user machine (with the user machine's reset switch) and write in user program mode.

   RAMCR is initialized with reset signal input and cancels RAM overlap (figure 4.14).

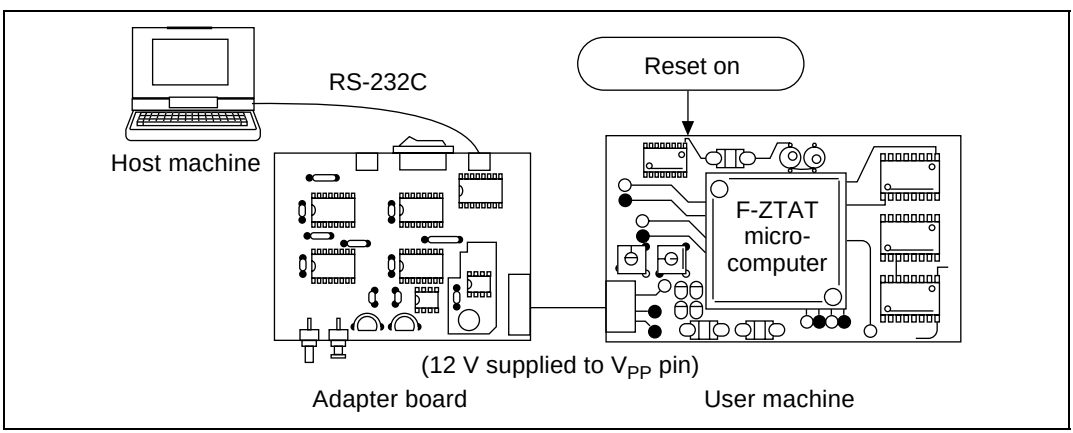


Figure 4.14 User Program Mode Startup by User Machine's Reset Switch

9. In flash memory emulation by RAM, when rewriting data, perform step 6 above. When writing overlapping RAM contents to flash memory, operate PC I/F software as follows:

```
: R– (RET) ------------------------------------------ (a)
: W FILENAME.MOT 1F000 1F1FF (RET)------------------- (b)
Erase Block address 0001F000–0001F1FF(Y/N)?Y---------- (c)
                :
                :
Transfer data address 0000XXXX----------------------- (d)
: Q ------------------------------------------------- (e)
```

Description:

a. Cancel flash memory emulation by RAM.

b. Enter the application program with the W command, and write to addresses H'1F000 to H'1F1FF.

c. Enter Y. Select flash memory block area erase for the application program write operation. The program/erase control program erases the specified block area of flash memory.

d. The “Sending application program” is displayed.

e. End PC I/F software operation with the Q command.

10. Press the adapter board’s transfer switch to stop the 12-V supply to the Vpp pin and mode pin. The Vpp ON LED (red) goes off (figure 4.15). The F-ZTAT microcomputer in the user machine starts the application program.

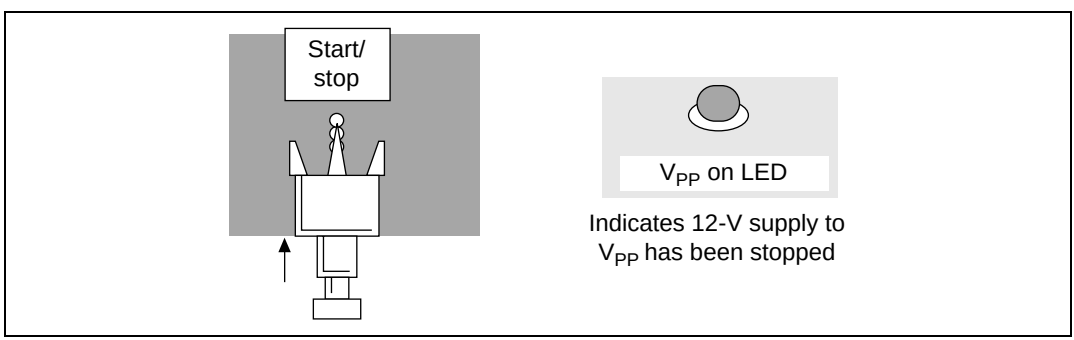


Figure 4.15 End of Programming Operation

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