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H8/36077 Group

External Clock Backup Function

Introduction

This application note describes how to switch the clock source between the on-chip oscillator and the external clock. First, the on-chip oscillator, then the external clock is used as the clock source. Thereafter, when the LSI detects that the external oscillation is stopped, the external clock backup function switches the clock source back to the on-chip oscillator.

Target Device

H8/36077 Group MCU

Contents

1. Specifications

- The state transition of the system clock is shown in figure 1.
- In the initial state, the LSI operates using the system clock whose clock source is the on-chip oscillator.
  - ① To confirm the operation, initially set the PCR20 bit of the PCR2 register to 1 to set the P20 pin as an output port.
  - ② Switch the clock source from the on-chip oscillator to the external clock.
  - ③ To confirm the operation, set the P20 bit of the PDR2 register to 0.
  - ④ Stop external oscillation. Use the external clock backup function to switch the clock source to the on-chip oscillator.
  - ⑤ To confirm the operation, set the P20 bit of the PDR2 register to 1.

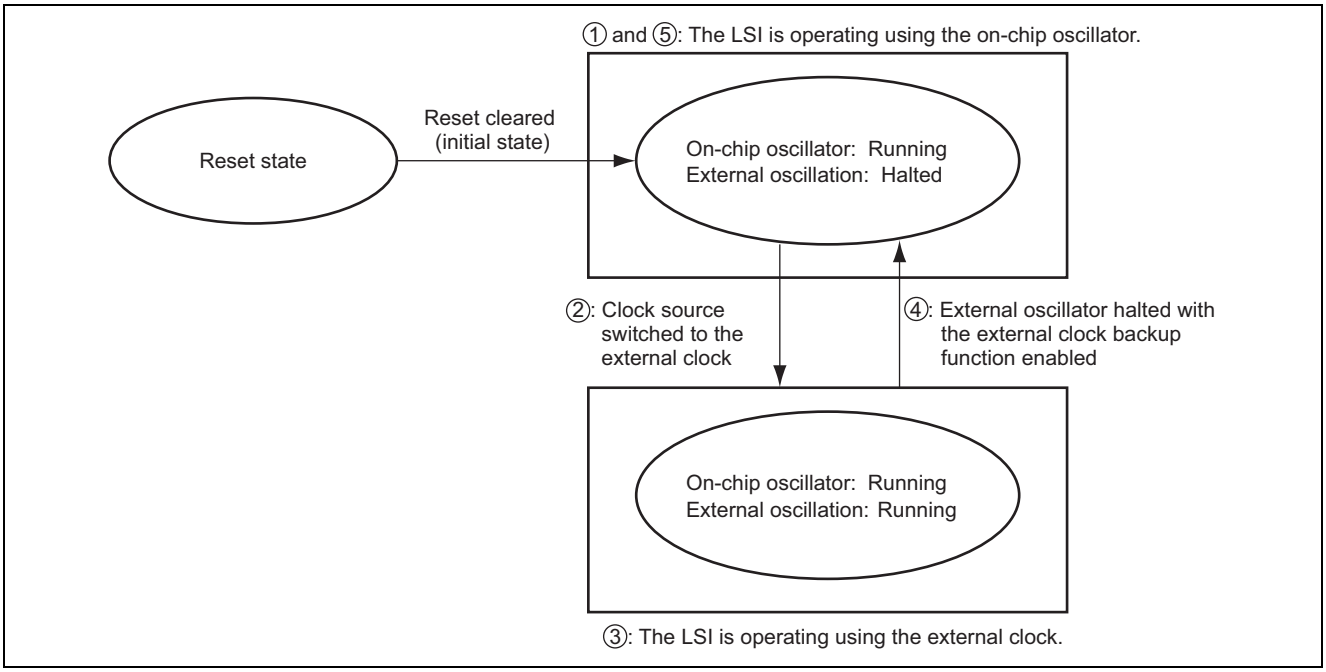


Figure 1 State Transition of the System Clock

2. Description of Functions Used

2.1 Functions Used

This sample task switches the system clock source. Figure 2 shows a block diagram of the clock pulse generator. This section describes the components in the clock pulse generator and the functions used in the sample task.

- System clock (ϕ)
  The basic clock used to operate the CPU and the peripheral modules.
- Prescaler S (PSS)
  A 13-bit counter that uses the system clock (ϕ) as the source. Prescaler S is incremented for each cycle.
- Timer Control/Status Register WD (TCSRWD)
  An 8-bit readable/writable register. This register controls watchdog timer operation.
- Clock Control Status Register (CKCSR)
  CKCSR selects the port C function, controls switching of the system clock source, and indicates the state of the selected system clock source.
- Port Control Register 2 (PCR2)
  PCR2 selects input or output bit by bit for the pins that will be used as the general I/O ports of port 2.
- Port Data Register 2 (PDR2)
  PDR2 is a general I/O port data register for port 2.

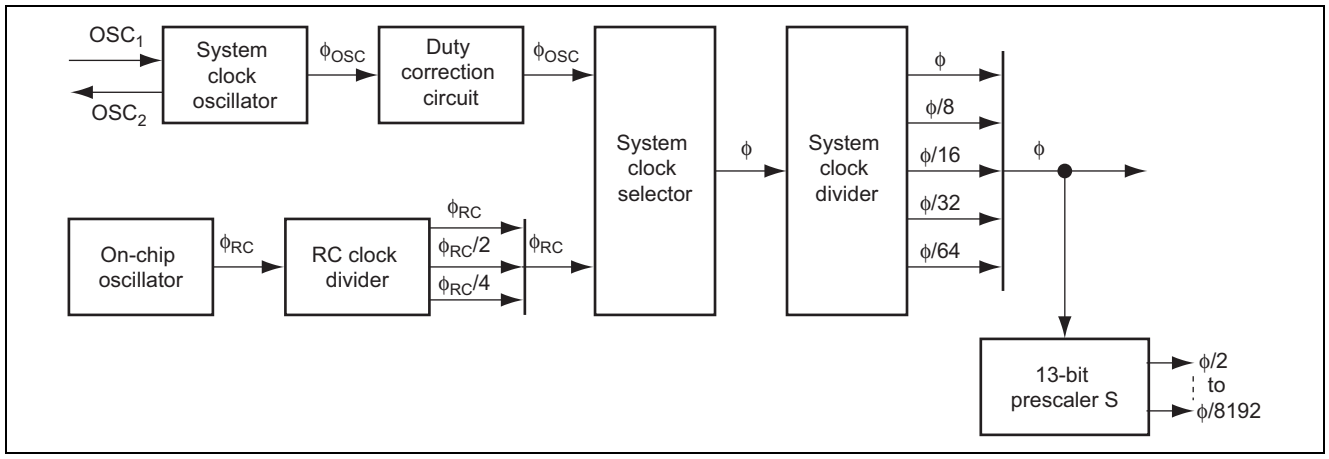


Figure 2 Block Diagram of the Clock Pulse Generator

2.2 Function Assignment

Assignment of functions used in this sample task is shown in table 1. As shown in table 1, functions are assigned to switch the clock source from the on-chip oscillator to the external clock. Thereafter, the external oscillation is stopped, and the external clock backup function switches the clock source to the on-chip oscillator.

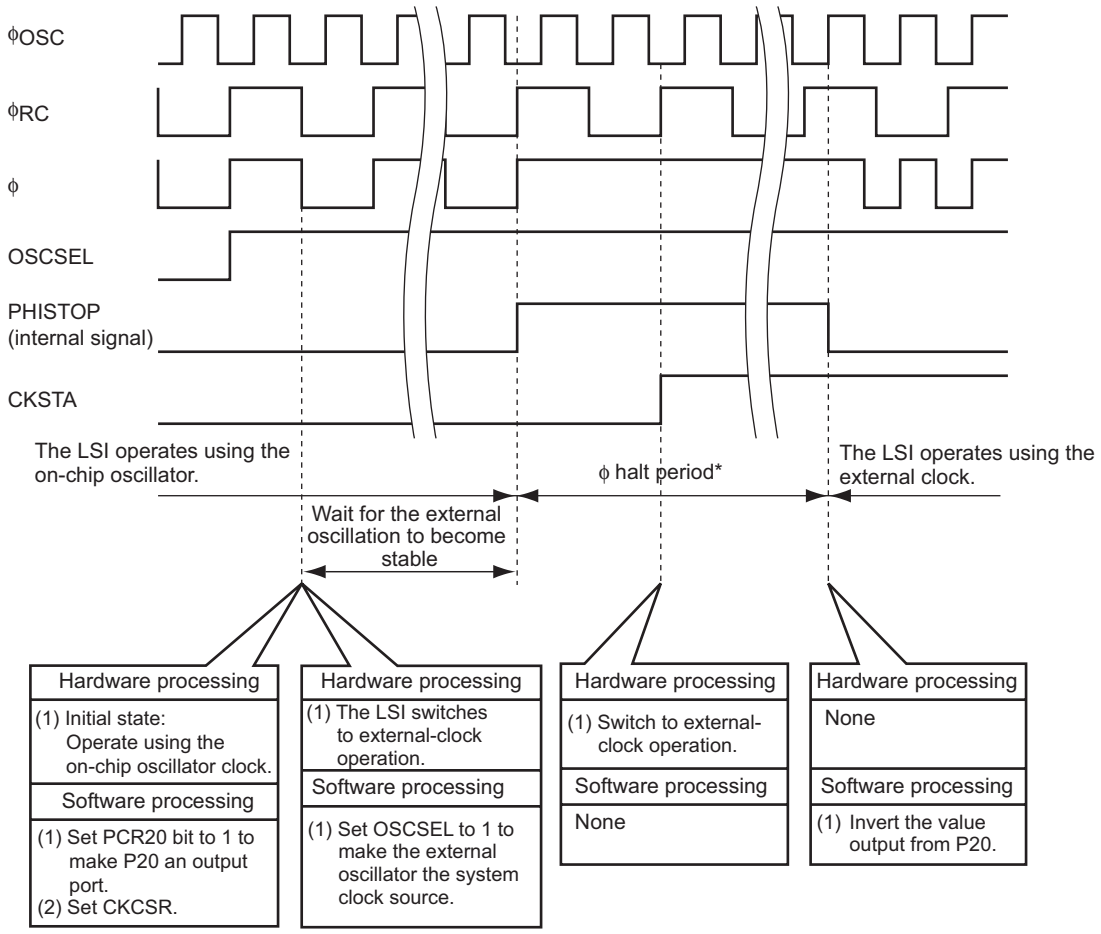
Table 1 Assignment of Functions

Element	Description
CKCSR	Selects the function of port C, switches the system clock source between the on-chip oscillator and the external clock, and indicates the state of the selected system clock source.
PCR2	Used to set the P20 pin as an output port. The P20 pin is used to check operation.
PDR2	Indicates the output value of the P20 pin. The P20 pin is used to check operation.

3. Principles of Operation

3.1 Timing for Switching from the On-chip Oscillator to the External Clock

Figure 3 illustrates the hardware and software processing for switching the clock source from the on-chip oscillator to the external clock. When the program is initiated, the LSI operates on a system clock using the on-chip oscillator as the clock source. To confirm the operation, the P20 bit of the PDR2 register is set to 1 by the program, and the P20 pin is set as an output port. When the clock source is switched to the external clock, the program clears the P20 bit of the PDR2 register to 0 to confirm the operation.



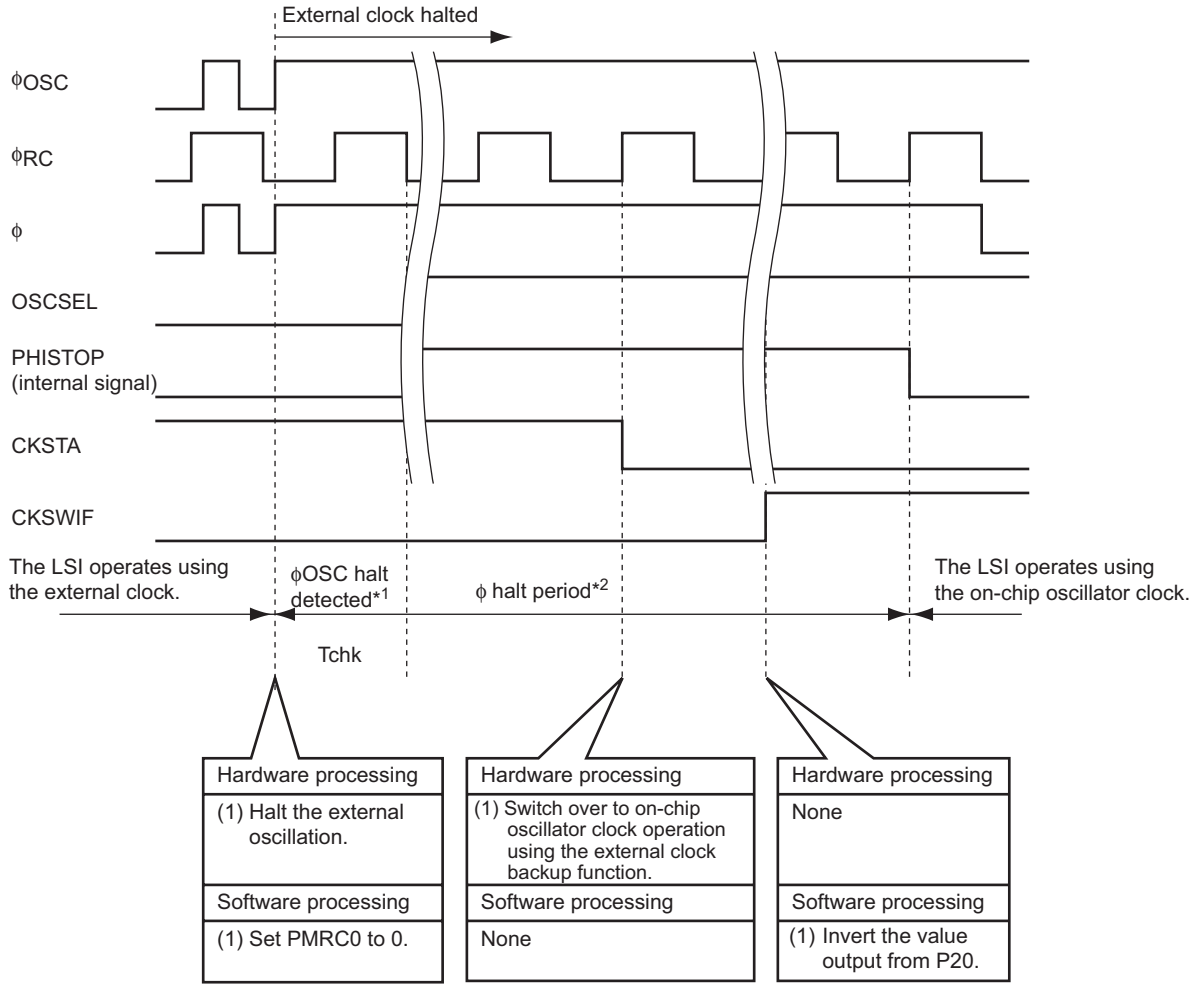
[Legend]
φOSC : External clock
φRC : On-chip oscillator clock
φ : System clock
OSCSEL : Bit 4 of CKCSR
PHISTOP : System clock stop control signal
CKSTA : Bit 0 of CKSTA

Note: * The system clock (φ) halt period ends when six φRC cycles have elapsed after φ is halted then the rising edge of the subsequent φOSC cycle is detected.

Figure 3 Timing for Switching from the On-Chip Oscillator to the External Clock

3.2 Timing for Using the External Clock Backup Function

Figure 4 illustrates the software and hardware processing for using the external clock backup function to switch the system clock source from the external clock to the on-chip oscillator. When the source clock is switched from the external clock to the on-chip oscillator, the P20 bit of the PDR2 register is set to 1 by the program to confirm the operation.



[Legend]
φOSC : External clock
φRC : On-chip oscillator clock
φ : System clock
OSCSEL : Bit 1 of CKCSR
PHISTOP : System clock stop control signal
CKSTA : Bit 0 of CKSTA
CKSWIF : Bit 2 of CKSTA

Notes: *1. $44 \times \phi RC \leq Tchk \leq 48 \times \phi RC$
*2. The system clock (φ) halt period starts when φ is halted and continues until the rising edge of the seventh φRC cycle.

Figure 4 Timing for Using the External Clock Backup Function

4. Description of Software

4.1 Description of Modules

Table 2 is a list of modules used in this sample task.

Table 2 Description of Modules

Function Name	Description
main	Sets CKCSR, switches system clock sources, and sets the P20 pin as an output port.
swckint	Handles exceptions regarding the switching of clock sources.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers Used

The internal registers used in this sample task are described below.

- Clock Control Status Register (CKCSR) Address: H'F734

Bit	Bit Name	Setting Value	R/W	Function
7	PMRC1	1	R/W	Port C Function Select Bits 1 and 0
6	PMRC0	1	R/W	**PMRC1** / **PMRC0** / **PC1** / **PC0** 0 / 0 / I/O / I/O 1 / 0 / CLKOUT / I/O 0 / 1 / I/O / OSC1 (external clock) 1 / 1 / OSC2 / OSC1
5	OSCBAKE	1	R/W	External Clock Backup Enable 0: External clock backup is disabled. 1: External clock backup is enabled. When this bit is set to 1, the external oscillation detection circuit is enabled. If the CPU detects that the external oscillation has stopped while the LSI is driven by the external clock, the system clock source is automatically switched to the on-chip oscillator regardless of the value of bit 4 of this register.
4	OSCSEL	0	R/W	LSI System Clock Select When OSCBAKE is set to 0: The OSCSEL bit is used to forcibly select the system clock source of the LSI. 0: Selects the on-chip oscillator as the system clock source. 1: Selects the external clock as the system clock source. When OSCBAKE is set to 1: The OSCSEL bit is used to switch the clock source from the on-chip oscillator to the external clock. When the OSCSEL bit is set to 1 while the LSI is using the on-chip oscillator as the system clock source, the system clock source is switched to the external clock. [Setting condition] • When 1 is written to the OSCSEL bit while the CKSWIF bit is set to 0 [Clearing conditions] • When 0 is written to the OSCSEL bit • When an external oscillation halt is detected while OSCBAKE = 1
3	CKSWIE	0	R/W	Clock Switchover Interrupt Enable When this bit is set to 1, the clock switchover interrupt request is enabled.

Bit	Bit Name	Setting Value	R/W	Function
2	CKSWIF	0	R/W	Clock Switchover Interrupt Request Flag [Setting condition] • When the system clock source is switched from the external clock to the on-chip oscillator [Clearing condition] • When 1 is read from this bit and then 0 is written to it
1	OSCHLT	1	R	External Oscillation Halt Detection Flag When OSCBAKE is set to 1: The OSCHLT bit indicates the result of external oscillation detection. 0: The external oscillation is active. 1: The external oscillation is inactive. When OSCBAKE is set to 0: The OSCHLT bit is meaningless. The bit is always read as 1.
0	CKSTA	0	R	LSI System Clock Status 0: The LSI operates by the on-chip oscillator. 1: The LSI operates by the external clock.

- Port Data Register 2 (PDR2) Address: H'FFD5

Bit	Bit Name	Setting Value	R/W	Function
0	P20	0	R/W	Stores an output value for port 2. If PDR2 is read while the PCR2 bits are set to 1, the value stored in PDR2 is read. If PDR2 is read while the PCR2 bits are cleared to 0, the corresponding pin state is read regardless of the value stored in PDR2.

- Port Control Register 2 (PDR2) Address: H'FFD5

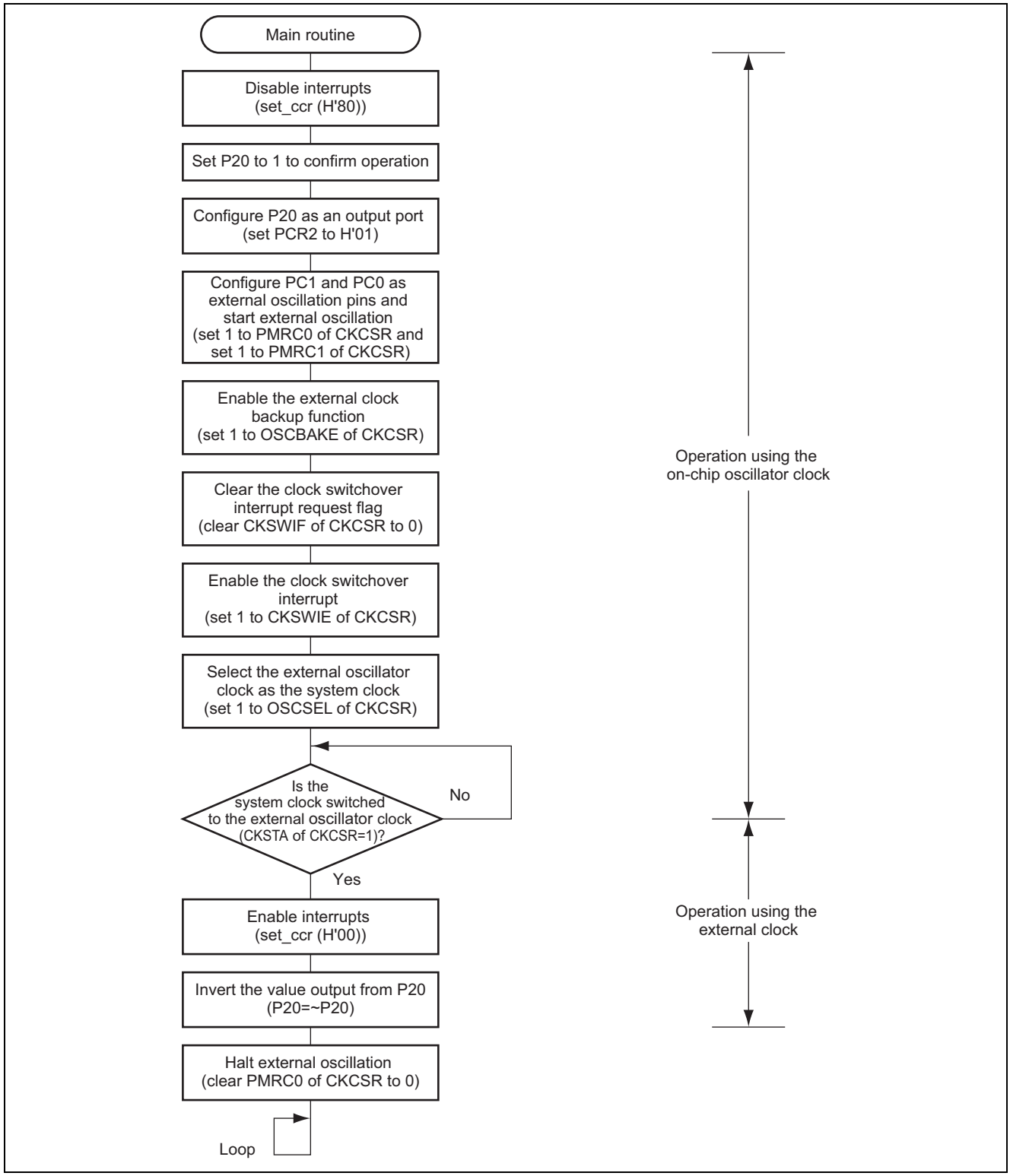
Bit	Bit Name	Setting Value	R/W	Function
0	PCR20	1	W	When the P20 pin functions as a general I/O port, setting the PCR20 bit to 1 makes the pin an output port, while clearing the bit to 0 makes the pin an input port.

4.4 RAM Usage

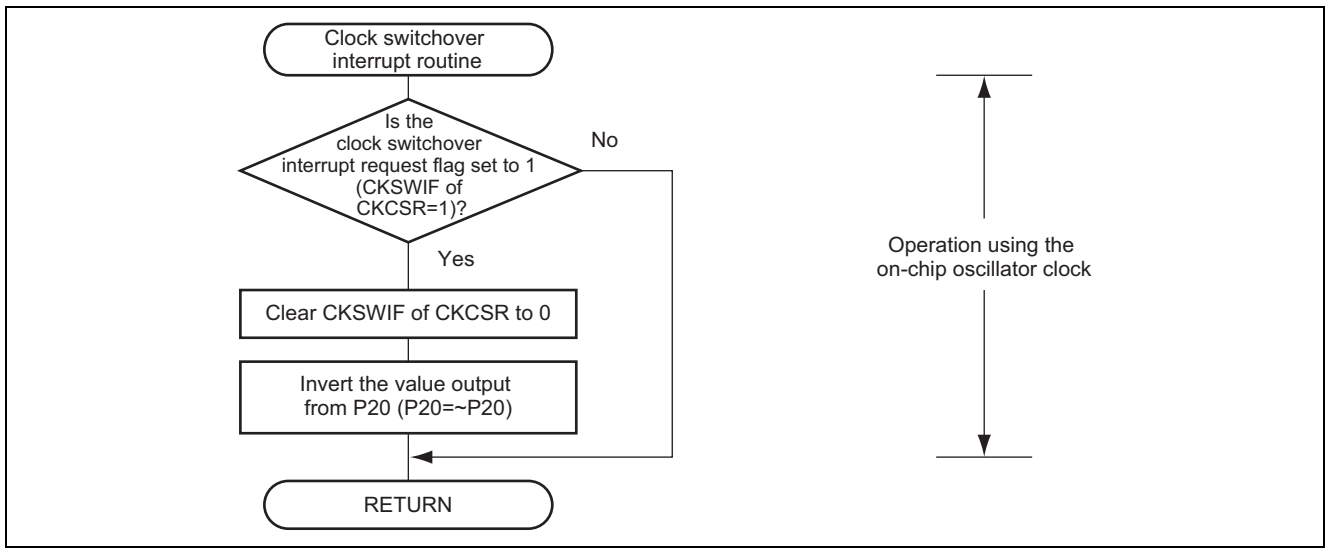
No RAM is used in this sample task.

5. Flowcharts

5.1 Main Routine



5.2 Clock Switchover Interrupt Routine



6. Program Listing

```
/************************************************************************************/
/*                                                                                  */
/*  H8/300H Series -H8/36077-                                                       */
/*  Application Note                                                                */
/*                                                                                  */
/*  'The External Clock Stop Detection'                                             */
/*                                                                                  */
/*  Function                                                                        */
/*  : Internal Ring OSC                                                             */
/*                                                                                  */
/*  <The external clock vessel>                                                     */
/*  External Clock : 10MHz                                                          */
/*  Internal Clock : 20MHz                                                          */
/*                                                                                  */
/*  <The built-in ring>                                                             */
/*  External Clock : 10MHz                                                          */
/*  Internal Clock : 10MHz                                                          */
/*                                                                                  */
/*  Sub Clock      : 32.768kHz                                                      */
/*                                                                                  */
/************************************************************************************/

#include    <machine.h>

/************************************************************************************/
/*  Symbol Definition                                                               */
/************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7                                             */
    unsigned char   b6:1;       /* bit6                                             */
    unsigned char   b5:1;       /* bit5                                             */
    unsigned char   b4:1;       /* bit4                                             */
    unsigned char   b3:1;       /* bit3                                             */
    unsigned char   b2:1;       /* bit2                                             */
    unsigned char   b1:1;       /* bit1                                             */
    unsigned char   b0:1;       /* bit0                                             */
};

#define CKCSR     *(volatile unsigned char *)0xF734  /* Clock Control Status Register*/
#define CKCSR_BIT (*(volatile struct BIT *)0xF734)   /* Clock Control Status Register*/
#define PMRC1     CKCSR_BIT.b7                       /* Port C                       */
#define PMRC0     CKCSR_BIT.b6                       /* Function Choice              */
#define OSCBAKE   CKCSR_BIT.b5                       /* External Clock Back Up Enable*/
#define OSCSEL    CKCSR_BIT.b4                       /* LSI Move Clock Select        */
#define CKSWIE    CKCSR_BIT.b3                    /* Clock Switching Interrupt Enable*/
#define CKSWIF    CKCSR_BIT.b2              /* Clock Switching Interrupt Request Flag*/
#define OSCHLT    CKCSR_BIT.b1              /* The External Clock Stop Detection Flag*/
#define CKSTA     CKCSR_BIT.b0                           /* LSI Move Clock Status  */
#define PCR2      *(volatile unsigned char *)0xFFE5      /* Port Control Register 2*/
#define PCR2_BIT  (*(volatile struct BIT *)0xFFE5)       /* Port Control Register 2*/
#define PCR20     PCR2_BIT.b0                        /* Port Control Register 2 bit 0*/
#define PDR2      *(volatile unsigned char *)0xFFD5          /* Port Data Register 2*/
```

```
#define PDR2_BIT  (*(volatile struct BIT *)0xFFD5)           /* Port Data Register 2*/
#define P20       PDR2_BIT.b0                          /* Port Data Register 2 bit 0*/


/*****************************************************************************/
/*  Function Define                                                          */
/*****************************************************************************/
extern void INIT (void);                        /* SP set                    */
void main ( void );                             /* Main Function             */
void swckint (void);                            /* Switch Clock Interrupt    */

/*****************************************************************************/
/*  Vector Address                                                           */
/*****************************************************************************/
#pragma section     V1                          /* Vector Section Set        */
void (*const VEC_TBL1[])(void) = {              /* 0x00 Reset                */
    INIT
};
#pragma section     V2                          /* Vector Section Set        */
void (*const VEC_TBL2[])(void) = {              /* 0x44 Clock Exchange Interrupt    */
    swckint
};
#pragma section                                 /* P                         */

/*****************************************************************************/
/*  Main Program                                                             */
/*****************************************************************************/
void main ( void )
{
    set_ccr(0x80);                              /* Interrupt Disable         */
    P20 = 1;                                    /* For The Movement Confirmation    */
    PCR2 = 0x01;                                /* P20 --> Output            */

    CKCSR |= 0xC0;                              /* Set Port C                */
    OSCBAKE = 1;                                /* Set External Clock Back Up Enable */
    CKSWIF = 0;                                 /* Clear CKSWIF Flag         */
    CKSWIE = 1;                                 /* Switch Clock Interrupt Enable    */
    OSCSEL = 1;                                 /* Change to External Clock  */

   while(CKSTA == 0);                           /* Change to External Clock ?       */

    set_ccr(0x00);                              /* Interrupt Enable          */

    P20 = ~P20;                                 /* For The Movement Confirmation    */

    PMRC0 = 0;                                  /* Stop External Clock       */

    while(1);
}
```

```
/*****************************************************************************/
/*  Switch Clock Interrupt                                                   */
/*****************************************************************************
*/
void swckint (void)
{
   if(CKSWIF==1){                          /* Change to Internal Clock?      */
     CKSWIF = 0;                           /* Clear CKSWIF Flag              */
     P20 = ~P20;                           /* For The Movement Confirmation  */
   }
}
```

- Link Addressing

Section Name	Address
CV1	H'0000
CV2	H'0044
P	H'0100
C$BSEC	
C$DSEC	
D	
R	H'FB80
B	

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.07.05	—	First edition issued

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