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April 1st, 2010
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SH7730 Group
Example of Writing Back from theOperand Cache

Introduction
This application note describes the operation of writing back from the operand cache of the SH7730. Please refer to this document when the operand cache is enabled in copy-back mode and data in external memory must match data in the operand cache (in cases like DMA transfer for areas where caching is enabled).

Target Device
SH7730

Contents

1. Preface............................................................................................................................ 2
2. Description of the Sample Application........................................................................... 3
3. Listing of Sample Program............................................................................................. 9
4. Documents for Reference............................................................................................ 15
1. Preface

1.1 Specifications
The sample program handles the operation of writing back from the operand cache by using the intrinsic function ocbp().

1.2 Modules Used
- Instruction and operand caches

1.3 Applicable Conditions
- Evaluation board The AP-SH4A-1A board incorporates the SH7730 with SH-4A CPU core is available from AlphaProject Co., Ltd.
  - External memory (area 0) 4-MB NOR-type flash memory: S29AL032D70TFI04 from Spansion
  - (area 3) 32-MB SDR-SDRAM (16 MB × 2): K4S281632F-UC75 from Samsung
- MCU SH7730 (R8A77301)
- Operating frequency
  - Internal clock: 266.66 MHz
  - SuperHyway bus clock: 133.33 MHz
  - Bus clock: 66.66 MHz
  - Peripheral clock: 33.33 MHz
- Bus width for area 0 16-bit fixed (with the MD3 pin at the low level)
- Clock operating mode Mode 2 (with the MD0 pin at the low level and MD1 pin at the high level)
- Endian Big endian (with the MD5 pin at the low level)
- Toolchain SuperH RISC engine Standard Toolchain Ver.9.1.1.0 from Renesas Technology
- Compiler options Default settings of High-performance Embedded Workshop
  - -cpu=sh4a -debug -optimize=0 -noinline
  - -gbr=auto -macsave=0 -save_cont_reg=0 -chgincpath -errorpath
  - -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0
  - -struct_alloc=1 -nologo

1.4 Related Application Note
The operation of the reference program for this document was confirmed with the setting conditions described in the SH7730 Group Application Note SH7730 Example of Initialization (REJ06B0848). Please refer to that document in combination with this one.
2. Description of the Sample Application

2.1 Overview of the SH7730 Cache Memory

Table 1 Overview of the SH7730 Cache Memory

<table>
<thead>
<tr>
<th>Item</th>
<th>Instruction Cache</th>
<th>Operand Cache</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td>32 Kbytes</td>
<td>32 Kbytes</td>
</tr>
<tr>
<td>Type</td>
<td>4-way set-associative, virtual address index/physical address tag</td>
<td>4-way set-associative, virtual address index/physical address tag</td>
</tr>
<tr>
<td>Line size</td>
<td>32 bytes</td>
<td>32 bytes</td>
</tr>
<tr>
<td>Number of entries</td>
<td>256 entries/way</td>
<td>256 entries/way</td>
</tr>
<tr>
<td>Write mode</td>
<td>—</td>
<td>Copy-back/write-through selectable</td>
</tr>
<tr>
<td>Replacement method</td>
<td>Least-recently-used (LRU) algorithm</td>
<td>Least-recently-used (LRU) algorithm</td>
</tr>
</tbody>
</table>

2.2 Setting up the Caches

2.2.1 Processing for Cache Settings

For the procedure to follow in setting up the cache control register (CCR), see the SH7730 Group Application Note: Examples of Cache Memory Settings (REJ06B0851).
2.3 Operation by the Sample Program

2.3.1 Overview of Processing

Figure 1 shows the flow of processing by the sample program.

Figure 1   Flow of Processing by the Sample Program
(1) A value (H'00) is written to 8,192 bytes (one way: 32 bytes × 256 entries = 8,192 bytes) of external memory while the operand cache is disabled (CCR.OCE = 0).

(2) The instruction cache or the operand cache is enabled in copy-back mode. A value (H'55) is written to 8,192 bytes of external memory in the cacheable P1 area. Since the cache is enabled in copy-back mode at this point, all data are written to the operand cache instead of external memory. As a result, if data from access to the cacheable P1 area (data in the operand cache) are compared with data from access to the non-cacheable P2 area (data in external memory), they will not match.
(3) Writing back from the operand cache is executed. After this is done, the data from access to the non-cacheable P2 area (data in external memory) are compared with the value $\text{H'55}$. A match indicates that writing back was successful.

Figure 4  Program Description (3)
2.3.2 Processing to Write Back from the Operand Cache
The procedure for writing back from the operand cache is described below.

![Procedure Diagram]

**Figure 5 Procedure for Writing Back from the Operand Cache**

Notes:
1. This sample program should be executed in privileged mode.
2. In this sample program, the exception/interrupt block (BL) bit is set to 1 during the operation of writing back from the operand cache. This prevents interrupt handling that might lead to access to external memory for which data would have to be written back. In general, the prevention of unanticipated access due to the handling of interrupts to memory areas for which writing back is in progress must be taken into account on the system side. In this sample program, however, interrupts are prohibited so that unanticipated access occurs.
2.4 Allocation of Sections in the Sample Program

The compiler extended function: #pragma section is used to change the section name of the function that handles the cache control register. In this sample program, the program area for the cache_set_ccr() function is changed to the PnonCache section. This ensures that only the PnonCache section will be placed in a cache-disabled space while other program sections are placed in cache-enabled spaces. Allocation of sections (address specification) is specified by options of the linker.

Table 2 gives information on sections in the sample program.

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Application of Section</th>
<th>Allocation Address (Virtual Address)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>Program area (in case of non specified)</td>
<td>0x0000 3000 Area P0 (caching is enabled, MMU address can be translated)</td>
</tr>
<tr>
<td>C</td>
<td>Constant area</td>
<td></td>
</tr>
<tr>
<td>C$BSEC</td>
<td>Address structure for non-initialized data area</td>
<td></td>
</tr>
<tr>
<td>C$DSEC</td>
<td>Address structure for initialized data area</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>Initialized data (initial value)</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>Non-initialized data area</td>
<td>0x0C00 0000</td>
</tr>
<tr>
<td>R</td>
<td>Initialized data area</td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>Stack area</td>
<td>0x0FFF F9F0 Area P1 (caching is enabled, MMU address cannot be translated)</td>
</tr>
<tr>
<td>INTHandler</td>
<td>Exception/interrupt handler</td>
<td>0x8000 0800</td>
</tr>
<tr>
<td>VECTTBL</td>
<td>Reset vector table</td>
<td></td>
</tr>
<tr>
<td>INTTBL</td>
<td>Interrupt vector table</td>
<td></td>
</tr>
<tr>
<td>PIntPRG</td>
<td>Interrupt mask table</td>
<td></td>
</tr>
<tr>
<td>SP_S</td>
<td>Stack area for handler of TLB miss</td>
<td>0x8FFF FDF0 Area P2 (caching is disabled, MMU address cannot be translated)</td>
</tr>
<tr>
<td>RSTHandler</td>
<td>Reset handler</td>
<td>0xA000 0000 Area P3 (caching is enabled, MMU address cannot be translated)</td>
</tr>
<tr>
<td>PResetPRG</td>
<td>Reset program</td>
<td></td>
</tr>
<tr>
<td>PnonCache</td>
<td>Program area (cache disabled access)</td>
<td></td>
</tr>
</tbody>
</table>
3. Listing of Sample Program

The listing for a sample program that implements the flow of processing shown in figure 1 is given below.

1. Sample Program Listing: "sh7730.c"

```c
#include <machine.h>
#include "cache.h"   /* Add cache function */
#include "typedefine.h"

void main(void);
#endif
/* ==== Macro definition ==== */
/* ---- Addresses of areas in SDRAM ---- */
#define D_SDRAM_ADDR1 (unsigned char *)(0x0c000000)  /* Cacheable area */
#define D_SDRAM_ADDR2 (unsigned char *)(0xac000000)  /* Non-cacheable area */
/* ==== Prototype declaration ==== */
void main(void);

/*''FUNC COMMENT''**************************** Technical reference data ***************/
/* System Name : SH7730 Sample Program
* File Name : sh7730.c
* Abstract : Sample Program of Write-Back Operation for the SH7730 Cache
* Version : Ver 1.00
* Device : SH7730
* Tool-Chain : SuperH RISC engine Standard Toolchain Ver.9.1.1.0
* OS : None
* H/W Platform : The AP-SH4A-1A board incorporates the SH7730 with SH4A-CPU core
* is available from AlphaProject Co., Ltd.
* Description : Sample program of write-back operation for the SH7730 cache
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***********************************************************************/

#include <machine.h>
#include "cache.h"   /* Add cache function */

void main(void);
#endif
/* --- Addresses of areas in SDRAM --- */
#define D_SDRAM_ADDR1 (unsigned char *)(0x0c000000)  /* Cacheable area */
#define D_SDRAM_ADDR2 (unsigned char *)(0xac000000)  /* Non-cacheable area */
/* --- Prototype declaration --- */
void main(void);

/*''FUNC COMMENT''**************************** Technical reference data ***************/
```

---

REJ06B0853-0100/Rev.1.00  March 2009  Page 9 of 17
Example of Writing Back from the Operand Cache

*                           : 0x0c000000 with 0x00.
*                           : Fill the external memory with 0x00.
*                           : 2.
*                           : Enable the operand cache to fill 8,192-byte data from
*                           : 0x0c000000 with 0x55.
*                           : Fill the operand cache with 0x55.
*                           : 3.
*                           : Compare the 8,192 bytes from 0x0c000000 (operand cache)
*                           : with the 8,192 bytes from 0xAC000000 (external memory) to
*                           : illustrate how a mismatch between the data in the external
*                           : memory and the data in the operand cache is generated.
*                           :
*                           :
*                           : 4.
*                           : ocbp() is used to perform write-back operation
*                           : in the operand cache.
*                           :
*                           : 5.
*                           : After the write-back operation, the 8,192 bytes from
*                           : 0xAC000000 (external memory) are compared with Hx55.
*                           : Matching means that writing back succeeded.
*                           :
*                           :
*                           : 3.
*                           : Program operation is based on the assumption that function
*                           : main is called while the instruction/operand caches are
*                           : disabled. In the example of initial settings, which should
*                           : be made before calling the main() function described below,
*                           : the instruction and operand caches are enabled.
*                           : In response to this, delete the processing to enable
*                           : the instruction/operand cache from the sample code for
*                           : initialization, and then call this sample program.
*                           :
*                           :
*                           :
* Disclaimer                : Program operation is based on the assumption that function
*                           : main is called while the instruction/operand caches are
*                           : disabled. In the example of initial settings, which should
*                           : be made before calling the main() function described below,
*                           : the instruction and operand caches are enabled.
*                           : In response to this, delete the processing to enable
*                           : the instruction/operand cache from the sample code for
*                           : initialization, and then call this sample program.
*                           :
*                           :
*                           :
* Argument                  : none
* Return Value              : none
* Calling Functions         :

***FUNC COMMENT END**********************************************************/

void main(void)
{
    int i;
    unsigned char *ptr1, *ptr2;
    /* ==== Caution ==== */
    /* ==== It is assumed that the processing below is executed while  ==== */
    /* ==== the IC/OC is disabled.            ==== */
    /* ==== Data are written from the cacheable P0 area while the OC is disabled. ==== */
    /* ==== External memory is filled with 0x00.        ==== */
    /*ptr1 = D_SDRAM_ADDR1;   /* Cacheable area (P0) */
    for(i=0; i<8192; i++){
        *ptr1++ = 0;
    }
    /* ==== The IC/OC is enabled. ==== */
    cache_set_ccr(D_CACHE_I_ON | D_CACHE_O_ON);
    /* ==== Data are written from the cacheable P0 area while the OC is enabled. ==== */
    /* ==== The operand cache is filled with 0x55.        ==== */
    /* An amount of data that will not lead to writing back (8,192 bytes) is written to cache */
    ptr1 = D_SDRAM_ADDR1;   /* Cacheable area (P0) */
    for(i=0; i<8192; i++){
        *ptr1++ = 0x55;
    }
    /* ==== Set1 ==== */
}
Example of Writing Back from the Operand Cache

/* ==== Comparison between cacheable area and non-cacheable area ==== */
ptr1 = D_SDRAM_ADDR1; /* Cacheable area (P0) */
ptr2 = D_SDRAM_ADDR2; /* Non-cacheable area (P2) */

/* The program code under Check1 below is to ensure that writing back from */
/* the operand cache does not proceed before cache_set_purge() is executed. */
/* The Check1 program is executed under the following conditions: */
/* 1. By using the calculation below (calculation of comparison with maximum cache */
/* capacity), the amount of data written into the cache is small enough, relative */
/* to the maximum cache capacity, that writing back will not be generated. */
/* 2. Cache entries for stack, literal, and data by program operation other than */
/* the above setting of 0x55 (Set1) and cache entries produced by the above */
/* setting of 0x55 (Set1)do not lead to more cache entries than the number */
/* corresponding to the setting for number of ways in the RAMCR. */
/* As a result, the Check1 program will not go into an infinite loop due to */
/* the generation of write-back operation. */
/* If the Check1 program does go into an infinite loop, focus on the amount of */
/* data being written into the cache as described above, and the writing of */
/* entries to the cache for the stack area, literals, and data produced by */
/* program operation other than the above setting of 0x55 to identify the */
/* factor that is leading to write-back operations. */

/* Calculation of comparison with maximum cache capacity */
/* Amount to be written into the cache (8,192 bytes) */
/* < Maximum cache capacity: 32,768 bytes */
/* = line size (32 bytes) x number of entries (4) x number of ways (4) */
/* ==== Check1 ==== */
for(i=0; i<8192; i++){
    if(*ptr1++ == *ptr2++){
        while(1){ /* Mistake in operand cache setting */
        }
    }
}
/* ==== Check1 ==== */
/* ==== Write-back in the operand cache ==== */
cache_set_purge();
/* ==== Comparison between cacheable area and non-cacheable area ==== */
ptr2 = D_SDRAM_ADDR2; /* Non-cacheable area (P2) */

/* The Check2 program below confirms whether data have been written to external */
/* memory by the write-back operation for the operand cache (cache_set_purge()). */
/* ==== Check2 ==== */
for(i=0; i<8192; i++){
    if(*ptr2++ != 0x55){
        while(1){ /* Failure of writing back from the operand cache */
        }
    }
}
/* ==== Check2 ==== */
while(1){ /* program end */
}
### Example of Writing Back from the Operand Cache

#### 2. Sample Program Listing: "cache.c"

```c
#include <machine.h>
#include "iodefine.h"
#include "cache.h"

/* === FILE COMMENT ===*
* System Name : SH7730 Sample Program
* File Name : cache.c
* Abstract : Sample Program for Setting the SH7730 Cache
* Version : Ver 1.00
* Device : SH7730
* Tool-Chain : SuperH RISC engine Standard Toolchain Ver.9.1.1.0
* OS : None
* H/W Platform : The AP-SH4A-1A board incorporates the SH7730 with SH4A-CPU core
*                is available from AlphaProject Co., Ltd.
* Description : Sample program for setting the SH7730 cache
* Operation :
* Disclaimer :
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* History : 27.May.2008 Ver. 1.00 First Release
/** FILE COMMENT END **/

#include <machine.h>
#include "iodefine.h"
#include "cache.h"

---snip---

/* === FUNC COMMENT ===*
* ID : 
* Outline : Writing back from the cache
* Include : 
* Declaration : void cache_set_purge(void)
* Description : 8,192 bytes of data are written back to 
*                the addresses from the start of the data area.
* Argument : none
* Return Value : none
* Calling Functions :
/** FUNC COMMENT END **/

void cache_set_purge(void)
{

    unsigned long addr = 0xC000000;
    unsigned int i;

    /* ===== Setting the exception/interrupt block (BL) bit ===== */
    set_cr(get_cr() | 0x10000000);

    /* ===== Writing back all entries ===== */
    for(i=0; i<256; i++)
    {
        ocbp((void *)addr); /* Invalidation and writing back of a cache block */
        addr +=0x20;
    }

    /* ===== Releasing the exception/interrupt block (BL) bit ===== */
    set_cr(get_cr() & ~(0x10000000));
}
```
3.1 Results of Execution

3.1.1 State before Write-Back Operation

Figures 6 and 7 show data dumped from external memory and from the operand cache before the write-back operation. Figures 6 and 7 illustrate how data in the cache line and in external memory do not match. We can also see this in the value of the U bits (1) in figure 7.

Figures 6 and 7 below were obtained from the memory and operand-cache windows of the High-performance Embedded Workshop.

![Figure 6](image1.png)  
Figure 6  External Memory Area before Write-Back Operation

![Figure 7](image2.png)  
Figure 7  Operand Cache Area before Write-Back Operation
3.1.2  State after Write-Back Operation

If the ocbp() intrinsic function is called to invalidate the cache and execute writing back from the cache while the V bit is 1 (indicating that the cache line contains valid data) and the U bit is 1 (indicating that data in the cache line and in external memory do not match), data dumped from external memory and from the operand cache are as shown in figures 8 and 9. That is to say, both the U and V bits are 0 for the cache entries and the data from the cache line have been written back to external memory.

Figures 7 and 8 below were obtained from the memory and operand-cache windows of the High-performance Embedded Workshop.

<table>
<thead>
<tr>
<th>Address</th>
<th>+0</th>
<th>+4</th>
<th>+8</th>
<th>+C</th>
<th>ASCII</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACO000000</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>UUUUUUUU</td>
</tr>
<tr>
<td>ACO000010</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>UUUUUUUU</td>
</tr>
<tr>
<td>ACO000020</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>UUUUUUUU</td>
</tr>
<tr>
<td>ACO000030</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>UUUUUUUU</td>
</tr>
<tr>
<td>ACO000040</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>UUUUUUUU</td>
</tr>
<tr>
<td>ACO000050</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>55555555</td>
<td>UUUUUUUU</td>
</tr>
</tbody>
</table>

Figure 8  External Memory Area after Write-Back Operation

Figure 9  Operand Cache Area after Write-Back Operation
4. Documents for Reference

- Software Manual
  SH-4A Software Manual (REJ09B0003)
  The most up-to-date versions of the documents are available on the Renesas Technology Website.

- Hardware Manual
  SH7730 Group Hardware Manual (REJ09B0359)
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