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SH7206 Group

Example of Setting the SCIF for UART Transmission

Introduction

This application note presents an example of configuring the serial communication interface with FIFO (SCIF) for UART transmission.

Target Device

SH7206

Contents

1. Overview

1.1 Specifications

- Channel 0 of the SCIF is initialized as a transmission module in UART mode, and character strings are transmitted.

1.2 MCU Functions Used

- SCIF channel 0

1.3 Conditions for Application

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock: 200 MHz
  Bus clock: 66.67 MHz
  Peripheral clock: 33.33 MHz
- C compiler: SuperH RISC engine Family C/C++ Compiler Package: Version 9.00
  (from Renesas Technology Corp.)
- Compiler options: Default setting of HEW (-cpu=sh2a -gbr=auto -debug -global_volatile=0 -opt_range=all
  -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note "Example of SH7206 Initial Configuration". Please refer to that note in combination with this one.

2. Description of Sample Application

This sample application uses the serial communication interface with FIFO (SCIF).

2.1 Summary of MCU Functions Used

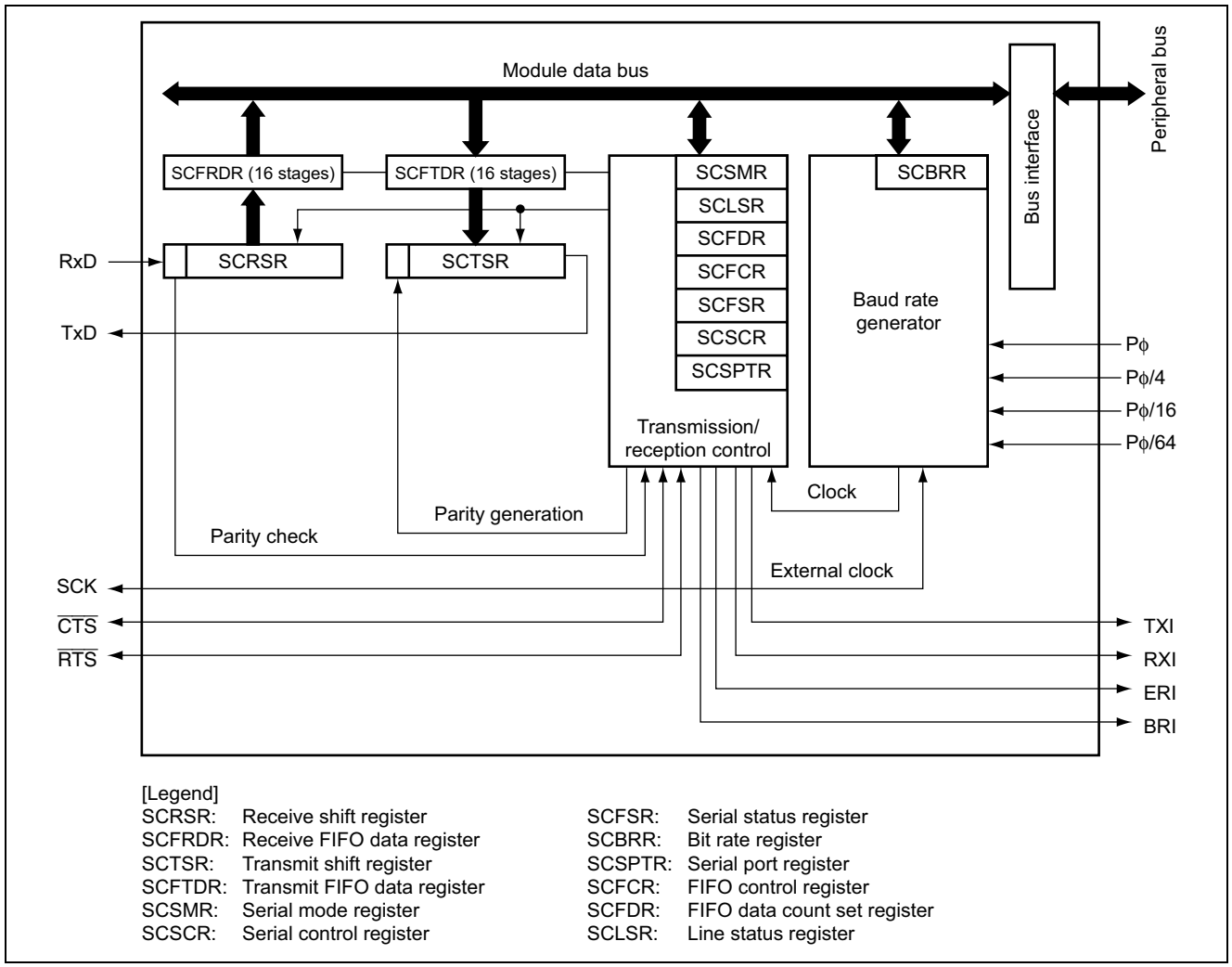
In asynchronous mode (UART), the SCIF adds start and stop bits to character data and transmits/receives them, while establishing synchronization for each character. The start and stop bits indicate the start and end of communication, respectively. Either the internal clock signal or the external clock signal input from the SCK pin can be selected as a clock source. Communication mode can be specified in terms of data transfer format, transfer rate, and others.

Table 1 summarizes the features of UART communication by the SCIF, and figure 1 shows a block diagram of the SCIF.

Table 1 Summary of SCIF (Asynchronous Mode)

Item	Function
Number of channels	4 (SCIF0 to SCIF3)
Clock source	Internal clock: Pϕ, Pϕ/4, Pϕ/16, or Pϕ/64 (Pϕ: Peripheral clock) External clock: Clock input from the SCK0 to SCK3 pins (The SCIF is driven by the clock input from the pin divided by 16.)
Data format	Transfer data length: 7 or 8 bits Bit transfer order: LSB first Start bit: 1 bit Stop bit: 1 or 2 bits Parity bit: Even, odd, or none
Baud rate	Internal clock: 62.94 bps to 1031.25 kbps (Pϕ = 33 MHz) External clock: 515.625 kbps at maximum (when Pϕ = 33 MHz and externally input clock = 8.25 MHz)
Error detection	Parity, framing, and overrun errors
Interrupt requests	• Transmit FIFO data empty interrupt (TXI) • Break interrupt (BRI) • Receive FIFO data full interrupt (RXI) • Receive error interrupt (ERI)
Others	• Break can be detected. • Clock supply to unused channels can be stopped to save power. • Built-in modem control functions (RTS and CTS) are available on channel 3. • The number of valid data bytes in the transmit and receive FIFO data registers and the number of receive errors of the receive data in the receive FIFO data register can be ascertained.

Note: * For details on the SCIF, refer to section 15, Serial Communication Interface with FIFO (SCIF), in the SH7206 Group Hardware Manual.



[Legend]

SCRSR:	Receive shift register	SCFSR:	Serial status register
SCFRDR:	Receive FIFO data register	SCBRR:	Bit rate register
SCTSR:	Transmit shift register	SCSPTR:	Serial port register
SCFTDR:	Transmit FIFO data register	SCFCR:	FIFO control register
SCSMR:	Serial mode register	SCFDR:	FIFO data count set register
SCSCR:	Serial control register	SCLSR:	Line status register

Figure 1 Block Diagram of SCIF

2.2 Procedure for Setting the MCU Modules

This section describes the basic setting procedures of the SCIF for UART mode (asynchronous) communication. Figures 2 and 3 show an example flow of initial settings for UART mode transmission, and figure 4 shows an example flow of UART mode transmission processing.

For details on the settings of individual registers, refer to the SH7206 Group Hardware Manual.

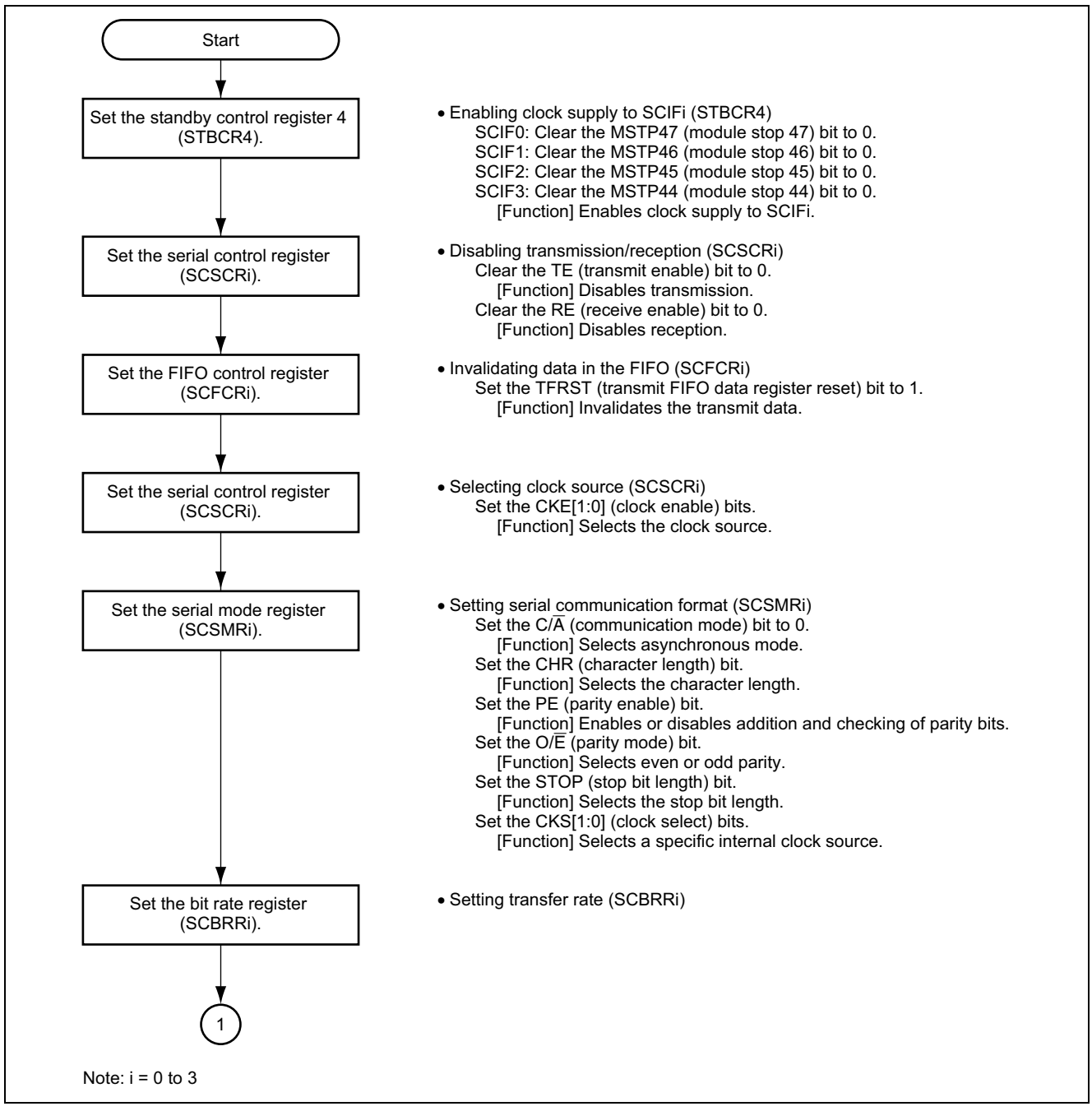
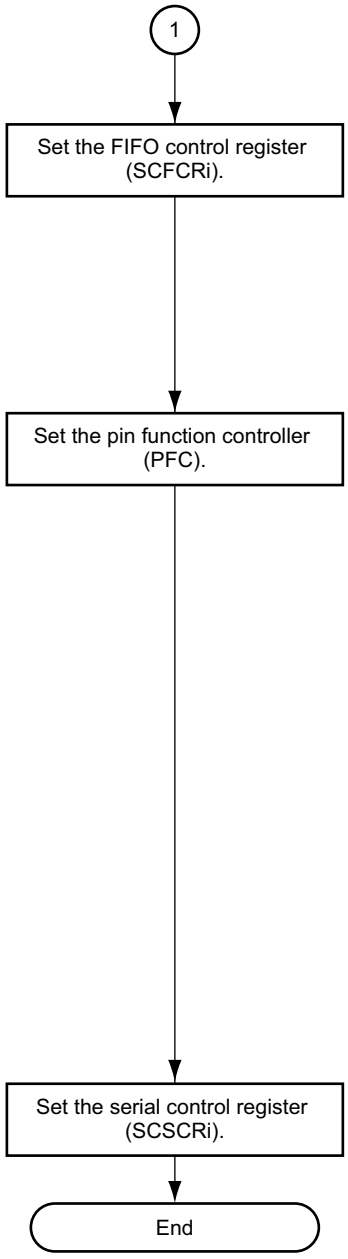


Figure 2 Example Flow of Initial Settings for UART Mode Transmission (1)



• Setting the number of stages in the FIFO to be used, enabling/disabling modem control signals, and canceling FIFO reset state (SCFCRi)
  Set the TTRG[1:0] (transmit FIFO data trigger) bits.
    [Function] Selects the transmit trigger number.
  Set the MCE (modem control enable) bit.
    [Function] Enables or disables modem control signals ($\overline{CTS}$ and $\overline{RTS}$).
  Clear the TFRST (transmit FIFO data register reset) bit to 0.
    [Function] Disables resetting of the transmit FIFO.
  Clear the LOOP (loop-back test) bit to 0.
    [Function] Disables loop-back test.

• Setting the multiplexed pins as serial communication pins (PACRL1, PACRL2, PECRL2, PECRL3)
SCIF0:
  Set the PA1MD (PA1 mode) bits to B'001.
    [Function] Selects TxD0 pin function.
  Set the PA2MD (PA2 mode) bits to B'001.
    [Function] Selects SCK0 pin function.
SCIF1:
  Set the PA4MD (PA4 mode) bits to B'001.
    [Function] Selects TxD1 pin function.
  Set the PA5MD (PA5 mode) bits to B'001.
    [Function] Selects SCK1 pin function.
SCIF2:
  Set the PE10MD (PE10 mode) bits to B'010.
    [Function] Selects TxD2 pin function.
  Set the PE8MD (PE8 mode) bits to B'10.
    [Function] Selects SCK2 pin function.
SCIF3:
  Set the PE5MD (PE5 mode) bits to B'010 or the PE12MD (PE12 mode) bit to B'11.
    [Function] Selects TxD3 pin function.
  Set the PE11MD (PE11 mode) bits to B'100.
    [Function] Selects CTS3 pin function.
  Set the PE6MD (PE6 mode) bits to B'010 or the PE9MD (PE9 mode) bits to B'011.
    [Function] Selects SCK3 pin function.

• Enabling transmission (SCSCRi)
  Set the TE (transmit enable) bit to 1.
    [Function] Enables transmission.

Note: i = 0 to 3

Figure 3 Example Flow of Initial Settings for UART Mode Transmission (2)

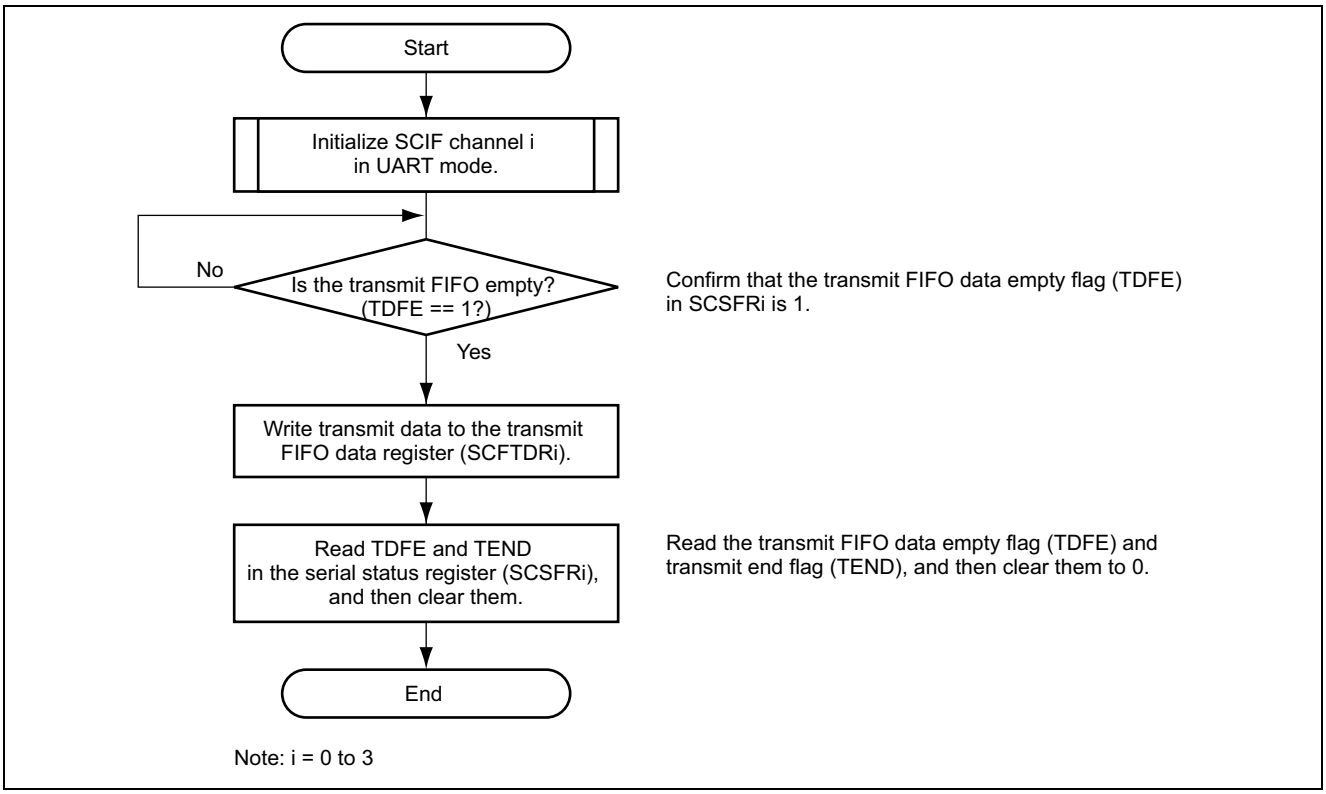


Figure 4 Example Flow of UART Mode Transmission Processing

2.3 Operation of Sample Program

The sample program uses the SCIF channel 0 in UART mode and transmits character strings. The transmit FIFO data empty flag is checked, and if the flag is set (the transmit FIFO is empty), one byte of data is written. After data has been written, the transmit end flag and the transmit FIFO data empty flag are cleared.

Table 2 shows the communication function settings of the sample program, and figure 5 shows the timing of the sample program operation.

Table 2 Communication Function Settings of Sample Program

Communication Format	Function Setting
Communication mode	UART (asynchronous)
Channel used	Channel 0
Interrupts	Not used
Transfer rate	115.2 kbps
Data size	8 bits
Parity	None
Stop bit	1 bit
Modem control	RTS/CTS function disabled
Bit transfer order	LSB first
Transmit FIFO data trigger	0

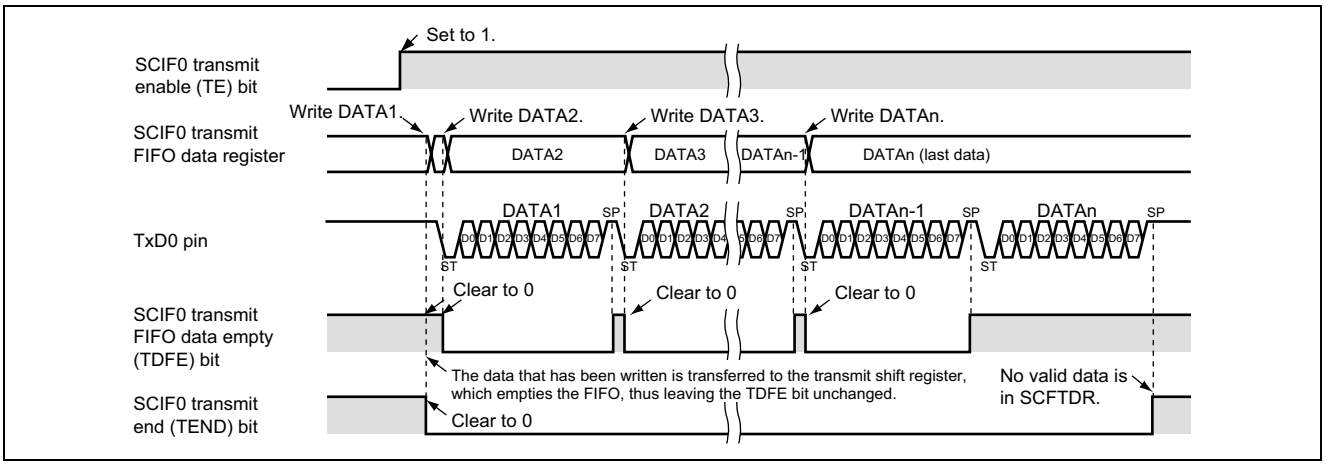


Figure 5 Timing of Sample Program Operation

2.4 Register Settings and Processing Sequence of Sample Program

The sample program initializes the SCIF channel 0 in UART mode, and then outputs the character string data in 1-byte units.

Table 3 shows the register settings related to the SCIF channel 0 made by the sample program. Figure 6 shows the processing flow of the sample program.

Table 3 Register Settings of Sample Program

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE040C	H'74	MSTP47 = 0: SCIF0 runs (clock is supplied).
Port A control register L1 (PACRL1)	H'FFFE3816	H'0010	PA1MD[2:0] = B'001: TxD0 output mode (SCIF0)
Serial mode register_0 (SCSMR_0)	H'FFFE8000	H'0000	• C/$\overline{A}$ = 0: UART mode • CHR = 0: 8-bit data • PE = 0: Parity bit addition disabled • STOP = 0: 1 stop bit • CKS[1:0] = B'00: Pϕ clock
Serial control register_0 (SCSCR_0)	H'FFFE8008	H'0000	• TE = 0: Transmission disabled • RE = 0: Reception disabled • CKE[1:0] = B'00: Internal clock (SCK is an input pin.)
		H'0020	TE = 1: Transmission enabled
FIFO control register_0 (SCFCR_0)	H'FFFE8018	H'0004	TFRST = 1: Reset operation for the transmit FIFO data register is enabled.
		H'0030	• TFRST = 0: Reset operation for the transmit FIFO data register is disabled. • TTRG[1:0] = B'11: Transmit FIFO data trigger number is 0. *
Bit rate register_0 (SCBRR_0)	H'FFFE8004	H'08	115.2 kbps

Note: * Transmit FIFO data trigger number is the number of remaining data bytes in the transmit FIFO which sets the transmit FIFO data empty (TDFE) flag in the serial status register (SCFSR).

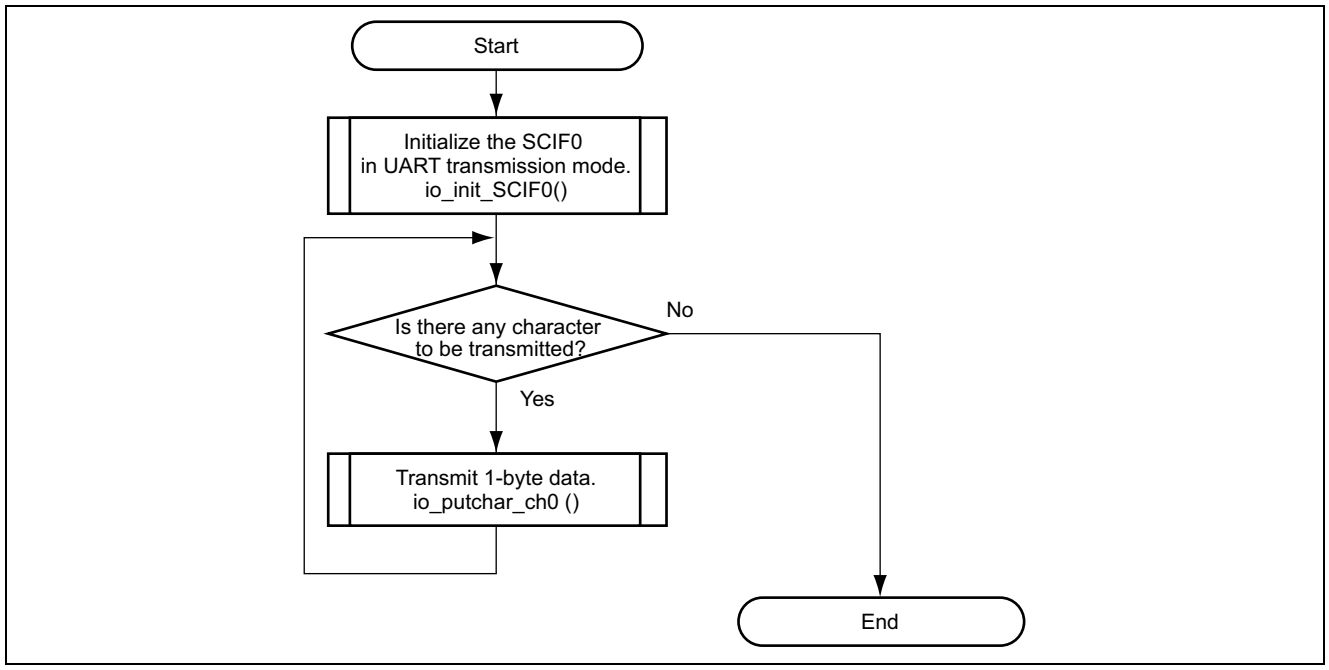


Figure 6 Processing Flow of Sample Program

3. Sample Program Listing

- Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*********************************************************************
*
*   System Name: SH7206 Sample Program
*   File Name  : main.c
*   Contents   : Sample program for asynchronous (UART) serial transmission by the
*                serial communication interface with FIFO (SCIF)
*   Version    : 1.00.00
*   Model      : M3A-HS60
*   CPU        : SH7206
*   Compiler   : SHC9.0.00
*
*   notes      : Sample program for asynchronous (UART) transmission by SCIF0
*              : Character string data is output from the TxD0 pin in a predetermined
*              : communication format.
*
*                <Caution>
*                This sample program is for reference
*                and its operation is not guaranteed.
*                Customers should use this sample program for technical reference
*                in software development.
*
*   Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
*   and Renesas Solutions Corp. All Rights Reserved
*
*   history    : 2004.11.04 ver.1.00.00
*""FILE COMMENT END""*********************************************************************/
#include "iodefine.h"                   /* iodefine.h is automatically created by HEW      */

/* ==== Prototype declaration ==== */
void main(void);
void io_init_SCIF0(int);
void io_putchar_ch0(unsigned char) ;

/* ==== Type declaration ==== */
/* SCIF baud rate setting */
typedef struct  {
    unsigned char scbrr;
    unsigned short scsmr;
} SH7206_BAUD_SET;

/* ---- Values for baud rate specification ---- */
enum{
    CBR_1200,
    CBR_2400,
    CBR_4800,
    CBR_9600,
    CBR_19200,
    CBR_31250,
    CBR_38400,
    CBR_57600,
    CBR_115200
};
```

- Sample Program Listing: main.c (2)

```
 53  /* ==== Register value table ==== */
 54  static SH7206_BAUD_SET scif_baud[] = {
 55      {214, 1},    /*   1200bps (-0.07%) */
 56      {106, 1},    /*   2400bps ( 0.39%) */
 57      {214, 0},    /*   4800bps (-0.07%) */
 58      {106, 0},    /*   9600bps ( 0.39%) */
 59      { 53, 0},    /*  19200bps (-0.54%) */
 60      { 32, 0},    /*  31250bps ( 0.00%) */
 61      { 26, 0},    /*  38400bps (-0.54%) */
 62      { 17, 0},    /*  57600bps (-0.54%) */
 63      {  8, 0}     /* 115200bps (-0.54%) */
 64  };
 65
 66  /*""FUNC COMMENT""*****************************************************************************
 67  * ID            :
 68  * Module summary: Main function of the sample program
 69  *                 (Asynchronous serial I/O transmission processing)
 70  *-------------------------------------------------------------------------------------------------
 71  * Include       : None
 72  *-------------------------------------------------------------------------------------------------
 73  * Declaration   : void main(void)
 74  *-------------------------------------------------------------------------------------------------
 75  * Functional description:
 76  *               : Initializes the SCIF0 for a predetermined communication format and
 77  *               : operating mode, and then carries out transmission in one- character units.
 78  *-------------------------------------------------------------------------------------------------
 79  * Argument      : None
 80  *-------------------------------------------------------------------------------------------------
 81  * Return value  : None
 82  *-------------------------------------------------------------------------------------------------
 83  * Notes         :
 84  *""FUNC COMMENT END""*************************************************************************/
 85  void main(void)
 86  {
 87      const unsigned char data[] = "SCIF sample\r\nHello\r\n";
 88                                          /* Character string to be transmitted             */
 89      const unsigned char *ptr;
 90
 91      /* ==== Initialize SCIF0 in UART transmission mode ==== */
 92      io_init_SCIF0(CBR_115200);          /* Bit rate: 115.2 kbps                           */
 93
 94      ptr = data;
 95      /* ==== Are there characters to be transmitted? ==== */
 96      while(*ptr != 0) {
 97          /* ==== Transmit 1-byte data ==== */
 98          io_putchar_ch0 (*ptr++);
 99      }
100
101      while (1) {
102          /* Program end */
103      }
104  }
```

- Sample Program Listing: main.c (3)

```
/*""FUNC COMMENT""*****************************************************************************
* ID             :
* Module summary: Initial setting of SCIF0 as an asynchronous (UART) transmit module
*-------------------------------------------------------------------------------------------------
* Include        : #include "iodefine.h"
*-------------------------------------------------------------------------------------------------
* Declaration    : void io_init_scif0(int bps)
*-------------------------------------------------------------------------------------------------
* Functional description:
*                : Initializes SCIF0.
*                : Asynchronous (UART)/ 8 bits / No parity/ 1 stop bit/ RTS/CTS disabled
*                : Baud rate is specified as argument bps.
*-------------------------------------------------------------------------------------------------
* Argument       : int bps : Value for baud rate specification
*-------------------------------------------------------------------------------------------------
* Return value   : None
*-------------------------------------------------------------------------------------------------
* Notes          : The baud rate setting values given in this program are those when the
*                : peripheral clock (Pphi) frequency is 33 MHz.
*                : If a different clock is used, the baud rate setting values must be changed.
*""FUNC COMMENT END""*************************************************************************/
void io_init_SCIF0(int bps)
{
    /* ==== Canceling power-down mode ==== */
    /* ---- Set standby control register 4 (STBCR4) ---- */
    CPG.STBCR4.BIT.MSTP47 = 0;          /* Start clock supply to SCIF0                    */

    /* ==== SCIF0 initialization ==== */
    /* ---- Set serial control register (SCSCRi) ---- */
    SCIF0.SCSCR.WORD = 0x0000;          /* Disable transmission/reception by SCIF0        */

    /* ---- Set FIFO control register (SCFCRi) ---- */
    SCIF0.SCFCR.BIT.TFRST = 1;          /* Reset transmit FIFO data register              */

    /* ---- Set serial control register (SCSCRi) ---- */
    SCIF0.SCSCR.BIT.CKE = 0x0;          /* B'00: Internal clock                           */

    /* ---- Set serial mode register (SCSMRi) ---- */
    SCIF0.SCSMR.WORD = scif_baud[bps].scsmr;
                                        /* Communication mode 0: Asynchronous mode        */
                                        /* Character length   0: 8-bit data               */
                                        /* Parity enable      0: Disable addition and checking */
                                        /* Parity mode        0: Even parity              */
                                        /* Stop bit length    0: 1 bit                    */
                                        /* Clock select       0: Table value              */

    /* ---- Set bit rate register (SCBRRi) ---- */
    SCIF0.SCBRR.BYTE = scif_baud[bps].scbrr;

    /* ---- Set FIFO control register (SCFCRi) ---- */
    SCIF0.SCFCR.WORD = 0x0030;      /* Transmit FIFO data trigger: 0 byte                 */
                                    /* Modem control enable: Disabled                     */
                                    /* Transmit FIFO data register reset: Disabled        */
                                    /* Loop-back test: Disabled                           */

    /* ==== Pin function controller (PFC) setting ==== */
    PORT.PACRL1.BIT.PA1MD = 1;      /* Set the PA1 pin as TxD0 (PACRL1)                   */

    /* ---- Set serial control register (SCSCRi) ---- */
    SCIF0.SCSCR.BIT.TE = 1;         /* Enable SCIF0 transmission                          */
}
```

- Sample Program Listing: main.c (4)

```
167  /*""FUNC COMMENT""*****************************************************************************
167  * ID            :
168  * Module summary: SCIF0 1-byte (one character) transmission processing
169  *-----------------------------------------------------------------------------------------------
170  * Include       : #include "iodefine.h"
171  *-----------------------------------------------------------------------------------------------
172  * Declaration   : void io_putchar_ch0(unsigned char c)
173  *-----------------------------------------------------------------------------------------------
174  * Functional description:
175  *               : Checks the transmit FIFO data empty flag in the SCIF0 serial
176  *               : status register (SCFSR0) to see if SCIF0 is ready for the next
177  *               : transmission (FIFO empty). If it is, transmits the 1-byte data
178  *               : passed as an argument.
179  *-----------------------------------------------------------------------------------------------
180  * Argument      : unsigned char c : Data for transmission
181  *-----------------------------------------------------------------------------------------------
182  * Return value  : None
183  *-----------------------------------------------------------------------------------------------
184  * Note          : None
185  *""FUNC COMMENT END""*************************************************************************/
186  void io_putchar_ch0 (unsigned char c)
187  {
188      /* ==== Check transmit FIFO empty (TDFE) flag in serial status register (SCFSR0) ==== */
189      while(SCIF0.SCFSR.BIT.TDFE == 0){
190          /* Wait until the TDFE flag is set */
191      }
192
193      /* ==== Write transmit data to transmit FIFO data register (SCFTDR0) ==== */
194      SCIF0.SCFTDR.BYTE = c;
195
196      /* ==== Read TDFE and TEND in serial status register (SCFSR0),
197                                                          and then clear the flags ==== */
198      SCIF0.SCFSR.WORD &= ~0x0060u ;
199  }
200  /* End of File */
```

4. Reference Documents

- SH-2A SH2A-FPU Software Manual (Rev.3.00)
  (Download the latest edition from the website of Renesas Technology Corp.)
- SH7206 Group Hardware Manual (Rev. 1.00)
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		Description	
Rev.	Date	Page	Summary
1.00	Sep.14.05	—	First edition issued

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