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SH7206 Group

Example of Setting the CPG to Change the Operating Frequency

Introduction

This application note presents an example of reconfiguration to change the operating frequency to demonstrate the usage of the SH7206 's clock pulse generator (CPG).

Target Device

SH7206

Contents

1. Overview

1.1 Specifications

- In the main function, the output on a port E pin is repeatedly inverted through software processing.
- In the NMI service routine, the settings of the clock pulse generator (CPG) are modified to change the operating frequency. Changing the operating frequency changes the speed of port E output inversion.
- A watchdog timer (WDT) is used to allow a time period for stabilization of the PLL circuit after the operating frequency is changed.

1.2 MCU Functions Used

- Clock pulse generator (CPG)
- Watchdog timer (WDT)
- NMI interrupt

1.3 Conditions for Application

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock: 200 MHz
  Bus clock: 66.67 MHz
  Peripheral clock: 33.33 MHz
- C compiler: SuperH RISC Engine Family C/C++ Compiler Package: version 9.00
  (from Renesas Technology Corp.)
- Compiler options: Default setting of HEW (-cpu = sh2a -debug –gbr = auto -global_volatile = 0
  -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1)

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note "Example of SH7206 Initial Configuration". Please refer to that note in combination with this one.

2. Description of Sample Application

This sample application applies the watchdog timer (WDT) to count the clock oscillation stabilization time after the operating frequency has been changed.

2.1 Summary of MCU Functions Used

When the frequency multiplier of the PLL circuit of the clock pulse generator (CPG) is changed, a certain amount of time is required for PLL operation to become stable. The built-in watchdog timer (WDT) is used to count this PLL stabilization time.

In changing the PLL frequency multiplier, rewriting the frequency control register of the CPG (FRQCR) will cause the internal activity of the CPU to halt and the WDT to start counting. When the WDT overflows, the CPG starts clock supply and thus the SH7206 resumes its operation.

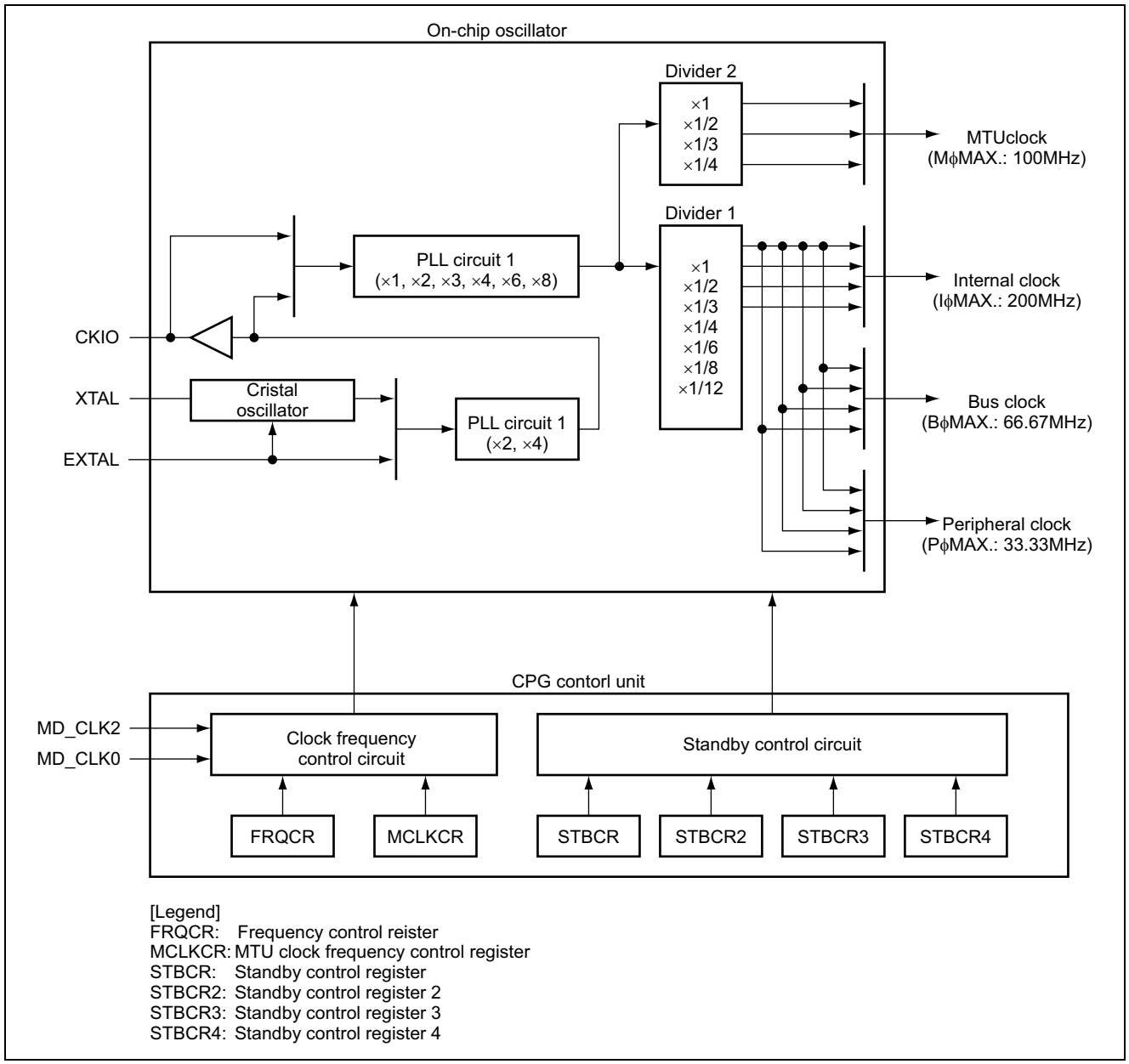
Tables 1 and 2 are summaries of CPG and WDT features. Figures 1 and 2 are schematic views of the CPG and WDT.

Table 1 Summary of CPG

Item	Function
Clock operating mode	Three modes (mode 2, mode 7)
Generated clock signals	Internal (Iϕ): Used by the CPU and cache Peripheral (Pϕ): Used by peripheral modules Bus (Bϕ): Used by the external bus interface MTU (Mϕ): Used by the MTU2S module
Frequency changing function	Frequencies of the internal and peripheral clocks can be changed independently through configuration of the PLL and divider circuits in the CPG.
Control of power down modes	Turns off the clocks in sleep mode and software standby mode. Stops individual modules in module standby modes.

Table 2 Summary of WDT

Item	Function
Number of channels	1
Counter	8-bit counter (up-counter only)
Timer mode	Watchdog timer mode or interval timer mode
Pin function	WDTOVF: Counter overflow signal output in watchdog timer mode
Clock source	Pϕ, Pϕ/64, Pϕ/128, Pϕ/256, Pϕ/512, Pϕ/1024, Pϕ/4096, Pϕ/16384 Pϕ: clock for on-chip peripheral modules
Method of activation	Watchdog timer/interval timer: Software activated Frequency changing process: Software activated Exiting from software standby mode: Interrupt detection



[Legend]
FRQCR: Frequency control reister
MCLKCR: MTU clock frequency control register
STBCR: Standby control register
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4

Figure 1 Schematic View of the CPG

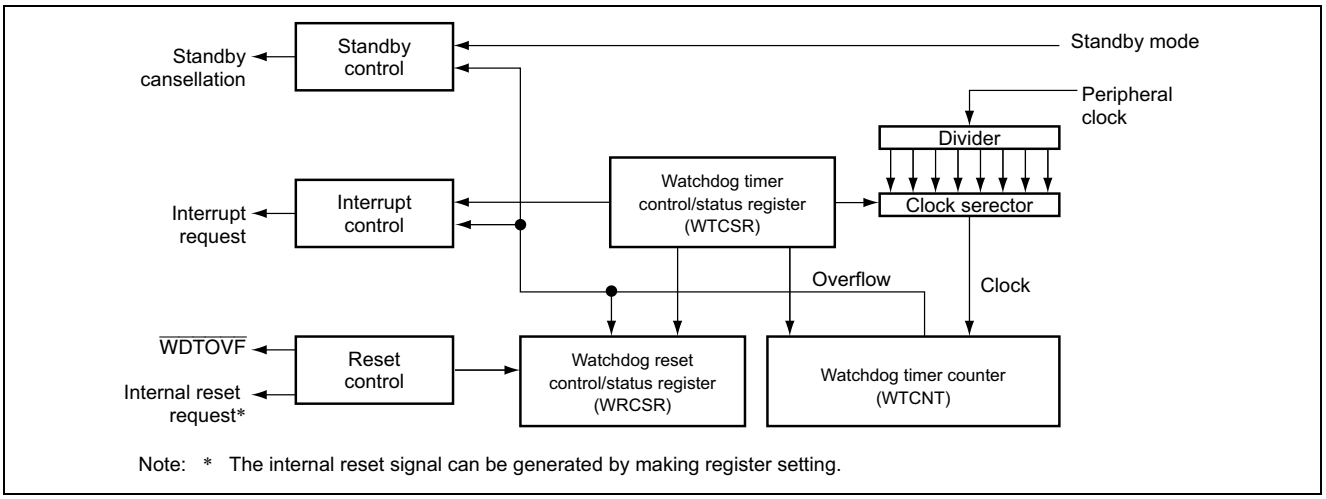


Figure 2 Schematic View of the WDT

2.2 Procedure for Setting the MCU Modules

Figure 3 shows the procedure for making settings to change the operating frequency. For details on setting the individual registers, consult the SH7206 Group Hardware Manual.

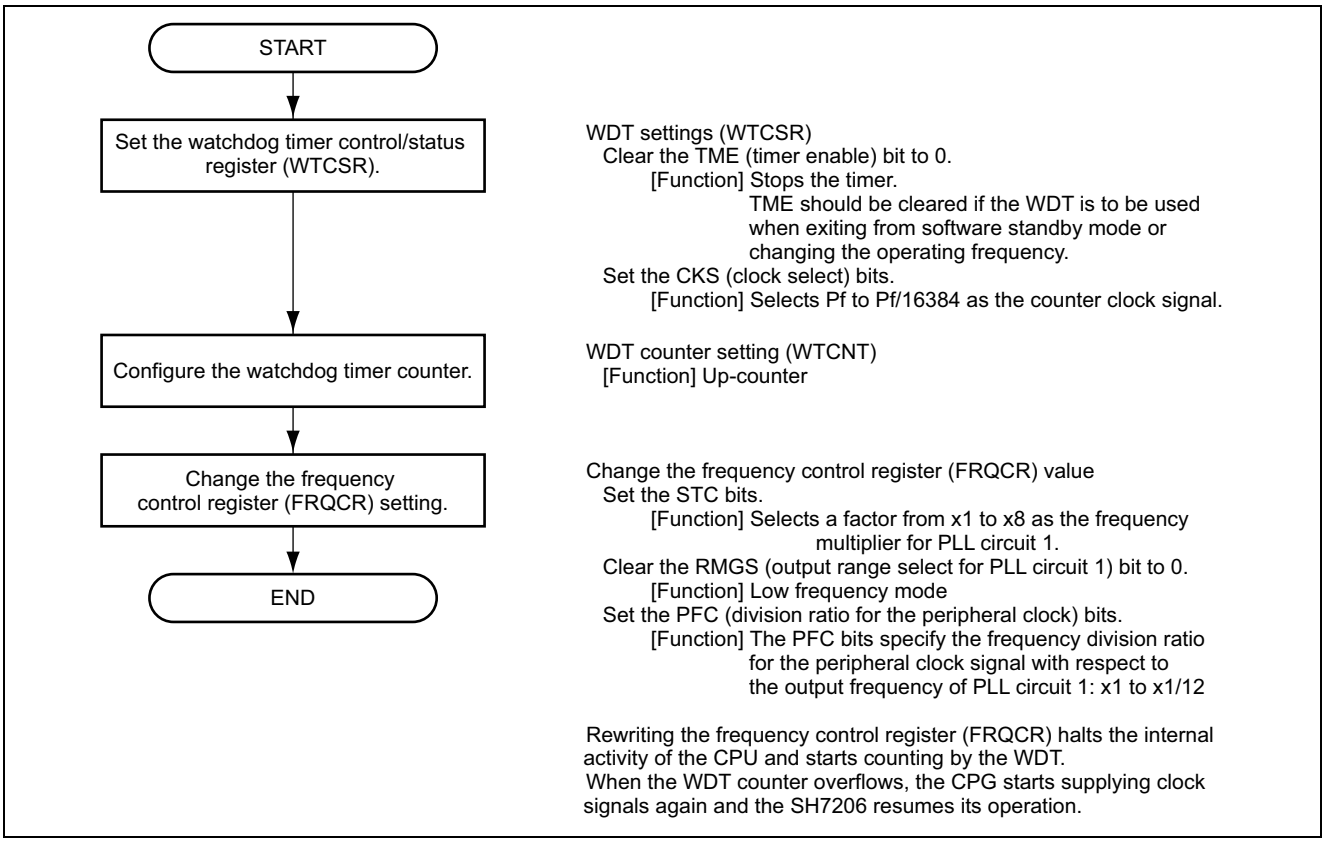


Figure 3 Example Flow for Settings to Change the Operating Frequency

2.3 Operation of Sample Program

The sample program repeatedly inverts the port pin state through software processing. When an NMI interrupt is input, the NMI service routine changes the operating frequency as shown in table 3. After the operating frequency has been changed, execution returns to the main function. The change of operating frequency changes the speed of port output inversion.

Figure 4 illustrates the timing of the sample program.

Table 3 Operating Frequencies Set by the Sample Program

	Clock Operating Mode	FRQCR Setting	Clock Ratio (I:B:P)	Operating Frequencies (I:B:P)
Initial operating frequency	Mode 2	H'120C	12:4:2	200 MHz : 66 MHz : 33 MHz
Operating frequency after change	Mode 2	H'1001	4:4:2	66 MHz : 66 MHz : 33 MHz

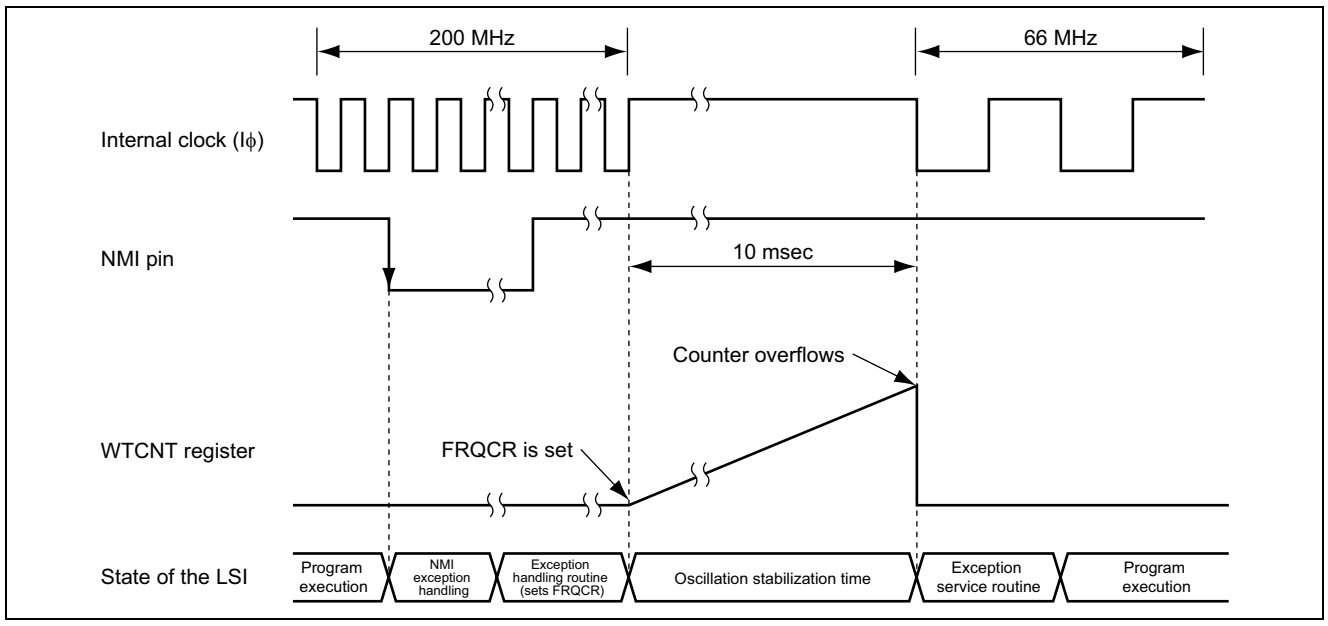


Figure 4 Timing of Sample Program Operation

2.4 Processing Sequence of Sample Program

The register values set when the operating frequency is to be changed are shown in table 4, and flowcharts of processing by the sample program are shown in figure 5.

Table 4 Register Settings for Changing the Operating Frequency

Register Name	Address	Setting	Description
Watchdog timer control/status register (WTCSR)	H'FFFE0000	H'A51E	TME = 0: Timer is disabled CKS[2:0] = B'110: Pϕ ×1/4096
Watchdog timer counter (WTCNT)	H'FFFE0002	H'5AAD	Timer counter is initialized to H'AD.
Frequency control register (FRQCR)	H'FFFE0010	H'0801	CKOEN = 1: Clock output is enabled STC[2:0] = B'000: ×1 (multiplication factor for PLL circuit 1) RNGS = 0: Low-frequency mode PFC[2:0] = B'001: ×1/2 (division ratio for the peripheral clock)

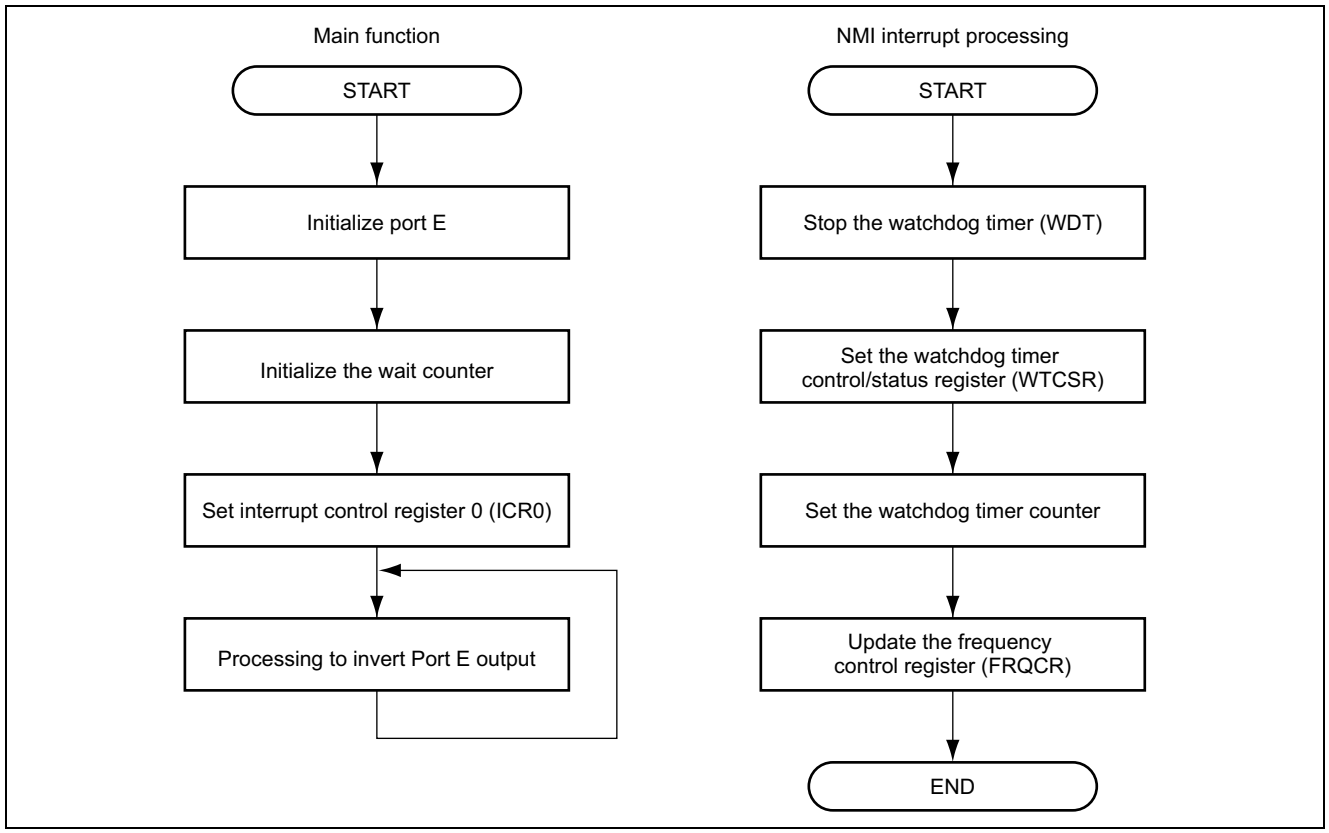


Figure 5 Flow of Processing by the Sample Program

3. Sample Program Listing

1. Sample Program Listing: main.c (1)

```
 1 /*""FILE COMMENT""*********************************************************************
 2 *
 3 *   System Name: SH7206 Sample Program
 4 *   File Name  : main.c
 5 *   Contents   : Changing the operating frequency
 6 *   Version    : 1.00.00
 7 *   Model      : M3A-HS60
 8 *   CPU        : SH7206
 9 *   Compiler   : SHC9.0.00
10 *
11 *   Note       : Sample program for changing the operating frequency
12 *
13 *                <Caution>
14 *                This sample program is for reference
15 *                and its operation is not guaranteed.
16 *                Customers should use this sample program for technical reference
17 *                in software development.
18 *
19 *   Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
20 *   and Renesas Solutions Corp. All Rights Reserved
21 *
22    history      :2004.10.28  ver.1.00.00
23 *""FILE COMMENT END""*********************************************************************/
24 #include <machine.h>
25 #include "iodefine.h"                    /* iodefine.h is automatically created by HEW    */
26
27
28 /* ==== Prototype declaration ==== */
29 void main(void);
30
```

2. Sample Program Listing: main.c (2)

```
/*""FUNC COMMENT""*****************************************************************************
* ID            :
* Module summary: Main function of the sample program (Changing the operating clock)
*-----------------------------------------------------------------------------------------------
* Include       :
*-----------------------------------------------------------------------------------------------
* Declaration   : void main(void)
*-----------------------------------------------------------------------------------------------
* Functional description: Processing to invert the output on a Port E pin (PE1)
*-----------------------------------------------------------------------------------------------
* Argument      : None
*-----------------------------------------------------------------------------------------------
* Return value  : None
*-----------------------------------------------------------------------------------------------
* Notes         :
*""FUNC COMMENT END""*************************************************************************/
void main(void)
{
   volatile unsigned int cnt;             /* For counting software wait                    */

   /* ==== Port initialization ==== */
   PORT.PECRL1.WORD = 0x0000;             /* Select PE1 as the pin function                */
   PORT.PEIORL.WORD = 0x0002;             /* Set PE1 as an output pin                      */
   PORT.PEDRL.WORD  = 0x0002;             /* Write the output value (= 1) to               */
                                          /*                            port E data register */
   /* ==== Interrupt control register 0 (ICR0) setting ==== */
    INTC.ICR0.BIT.NMIE = 0;               /* Select falling edge                           */

   /* ==== Port E output inverting processing ==== */
    while(1){
        for(cnt=0x100000u; cnt > 0u; cnt--){
                                          /* Software wait                                 */
        }
        PORT.PEDRL.BIT.PE1DR ^= 0x1u ;    /* Invert the Port E output (LED blinks)         */
    }
}

/* End of file */
```

3. Sample Program Listing: intprg.c (1)

```
 1  /*""FILE COMMENT""*********************************************************************
 2  *
 3  *   System Name: SH7206 Sample Program
 4  *   File Name  : intprg.c
 5  *   Version    : 1.00.00
 6  *   Contents   : Definition of interrupt processing function
 7  *   Model      : M3A-HS60
 8  *   CPU        : SH7206
 9  *   Compiler   : SHC9.0.00
10  *   OS         : none
11  *
12  *   Note       : This file was originally created by Renesas Project
13  *              : Generator (Ver.3.1) and modified for the application note.
14  *
15  *                <Caution>
16  *                This sample program is for reference
17  *                and its operation is not guaranteed.
18  *                Customers should use this sample program for
19  *                technical reference in software development.
20  *
21  *
22  *   This file is generated by Renesas Project Generator (Ver.3.1).
23  *
24  *   Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
25  *   AND Renesas Solutions Corp. All Rights Reserved
26  *
27  *   history     : 2004.10.14 ver.1.00.00
28  *""FILE COMMENT END""*****************************************************************/
29  #include <machine.h>
30  #include "vect.h"                       /* vect.h is automatically created by HEW        */
31  #include "iodefine.h"                   /* iodefine.h is automatically created by HEW    */
32  #pragma section IntPRG

    Lines 33 to 47 have been omitted.
```

4. Sample Program Listing: intprg.c (2)

```
48 // 11 NMI
49 /*""FUNC COMMENT""*****************************************************************************
50 * ID             :
51 * Module summary : NMI interrupt processing (Change the operating clock)
52 *-----------------------------------------------------------------------------------------------
53 * Include        : #include "iodefine.h"
54 *-----------------------------------------------------------------------------------------------
55 * Declaration    : void INT_CMI0(void)
56 *-----------------------------------------------------------------------------------------------
57 * Functional description: Changes the operating frequency
58 *                : by modifying the multiplication factor of the PLL.
59 *                : I:B:P = 200MHz:66MHz:33MHz -> I:B:P = 66MHz:66MHz:33MHz
60 *-----------------------------------------------------------------------------------------------
61 * Argument       : None
62 *-----------------------------------------------------------------------------------------------
63 * Return value   : None
64 *-----------------------------------------------------------------------------------------------
65 * Notes          : The entry address of NMI is defined in vecttbl.c, which is
66 *                : automatically generated  by HEW.
67 *                : Description of #pragma is written in vect.h, which is
68 *                : automatically generated by HEW.
69 *""FUNC COMMENT END""*************************************************************************/
70  void INT_NMI(void)
71  {
72      /* ==== Set watchdog timer control/status register (WTCSR) ==== */
73       WDT.WTCSR.WORD = 0xa51e;         /*
74                                           TME="0" should be set if WDT is used when canceling
75                                           standby mode or changing the operating frequency
76                                           Counter clock = P clock /4096
77                                           Write H'A5 to the upper byte of WTSCR.
78                                        */
79      /* ==== Set watchdog timer counter ==== */
80      WDT.WTCNT.WORD = 0x5aad;           /* Overflows after counting approx. 10 ms          */
81
82      /* ==== Change frequency control register (FRQCR) setting ==== */
83      CPG.FRQCR.WORD = 0x0801;          /*
84                                           PLL1(x1),PLL2(x4), I:B:P=4:4:1
85                                           Clockin = 16.67MHz, CKIO = 66.6MHz
86                                           I Clock = 66.6MHz, B Clock = 66.6MHz,
87                                           P Clock = 33.3MHz
88                                        */
89      /* CPU operation stops and resumes after WDT counter has overflowed  */
90  }

   Line 91 and subsequent lines have been omitted.
```

4. Reference Documents

- SH-2A SH2A-FPU Software Manual (Rev.3.00)
  (Download the latest edition from the website of Renesas Technology Corp.)
- SH7206 Group Hardware Manual (Rev. 1.00)
  (Download the latest edition from the website of Renesas Technology Corp.)

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		Description	
Rev.	Date	Page	Summary
1.00	Sep.05.05	—	First edition issued

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