SH7216 Group

Example of Initialization

REJ06B0899-0101
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Summary

This application note gives an example of configuration items to activate the SH7216 Microcomputers (MCUs).

Target Device

SH7216 MCU

Contents

1. Introduction

1.1 Specifications

Configure the clock pulse generator (CPG) after the reset is canceled.

1.2 Modules Used

- Clock pulse generator (CPG)

1.3 Applicable Conditions

MCU	SH7216
Operating Frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated Development Environment	Renesas Electronics High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu - fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

2. Applications

Configuration program for the minimum hardware setup is required to execute the main function created in C code. This application note describes the configuration example for the configuration program.

All of the SH7216 application notes assume to use the sample program described in this application note as the configuration program.

2.1 Sample Program

The configuration program consists of several source files such as the resetprg.c, describing the PowerON_Reset_PC function, and the hwsetup.c, describing the hardware setup function. Main source files are as follows.

- resetprg.c
- hwsetup.c
- cpg.c

"resetprg.c" is a source file created on the file automatically generated by the High-performance Embedded Workshop, and describes the PowerON_ResetPC function. The PowerON_ResetPC function initially executed after the reset is canceled. Its beginning address is set in the reset vector defined by the vecttbl.c.

"hwsetup.c" describes the HardwareSetup function called by the PowerON_Reset_PC function. The HardwareSetup function calls the io_set_cpg function to set the CPG. When using the external bus interface such as interfacing SDRAM, call the io_set_cpg function, and then add processing to set the Bus State Controller (BSC) to the HardwareSetup function as appropriate.

"cpg.c" describes the io_set_cpg function which is called from the HardwareSetup function. The io_set_cpg function sets the Frequency control register (FRQCR) in the program on the on-chip RAM (For more information, refer to the Renesas technical update TN-SH7-Axxxx/E). The sample program execute the _seccpy function to copy the program section to set the FRQCR (section name: PURAM) from on-chip ROM to on-chip RAM at the beginning of the io_set_cpg function, and sets the FRQCR by the io_set_cpg_frqcr function. After setting the FRQCR, set the MTU2S clock frequency control register (MCLKCR) and the AD clock frequency control register (ACLKCR) to clear the module standby function for internal peripheral modules.

Figure 1 to Figure 4 show flow charts of the configuration program in above source files used in this application.

Supplement: About the stack area

CPU can access pages 0 to 3 in the SH7216 on-chip RAM in one cycle both in reading and writing. This application allocates the stack area at the end of page 3 in the on-chip RAM (address: H'FFF8 C0000 to H'FFF8 FFFF) to support the SH7216 high-speed access performance.

The stack area is allocated as section S, which can be set in the High-performance Embedded Workshop. On the [Build] menu, open the [SuperH RISC engine Standard Toolchain] dialog box, and select [Link/Library] tab. Then, select "Section" from the "Category" drop-down list. When it is not required to support the SH7216 high-speed access performance, the stack area can be allocated to pages 4 to 7 in the on-chip RAM (For 768 KB on-chip ROM: allocate to pages 4 and 5). Reallocate the stack area to sections according to the system.

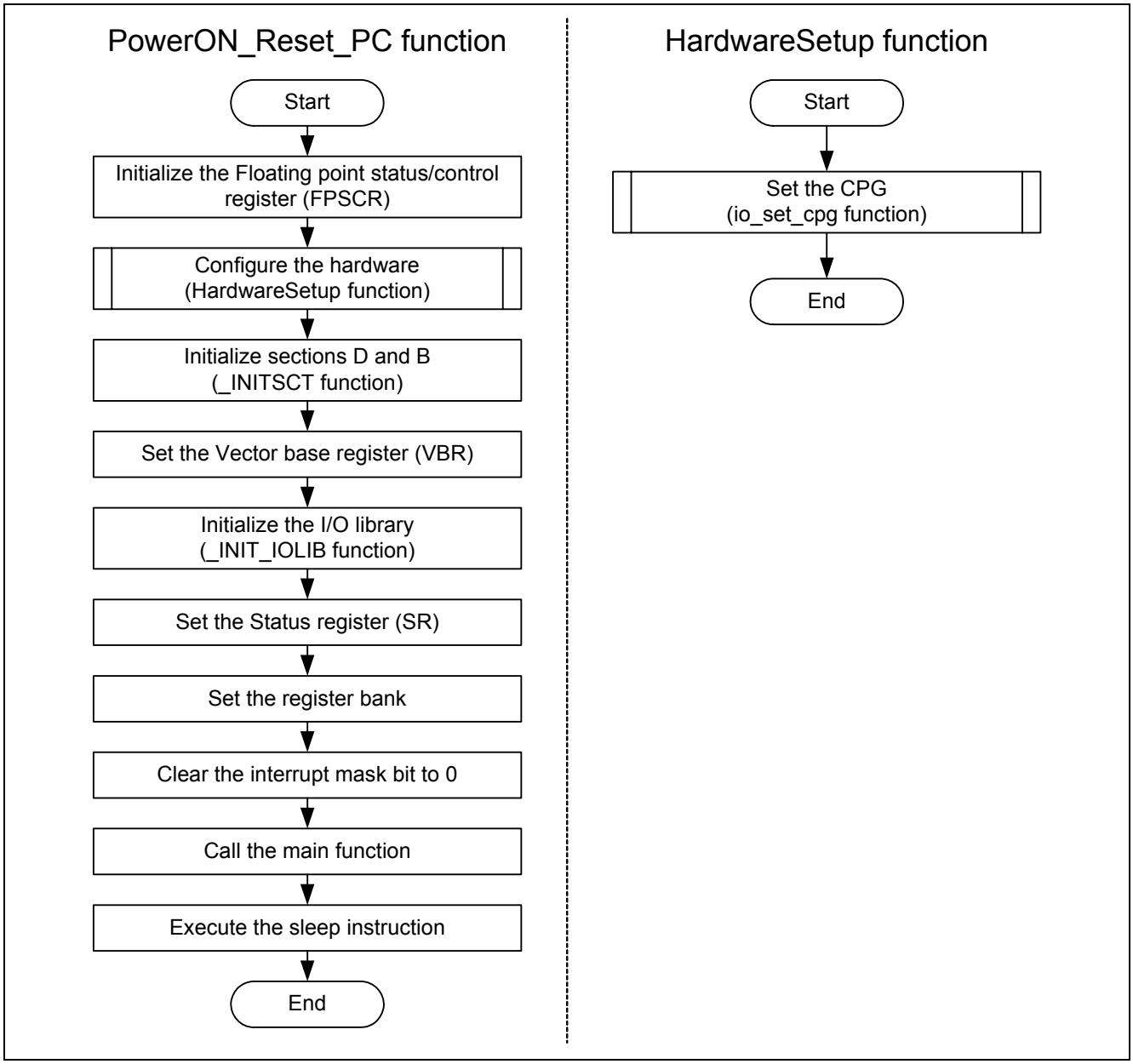


Figure 1 Flow Charts of Functions (PowerON_Reset_PC, and HardwareSetup)

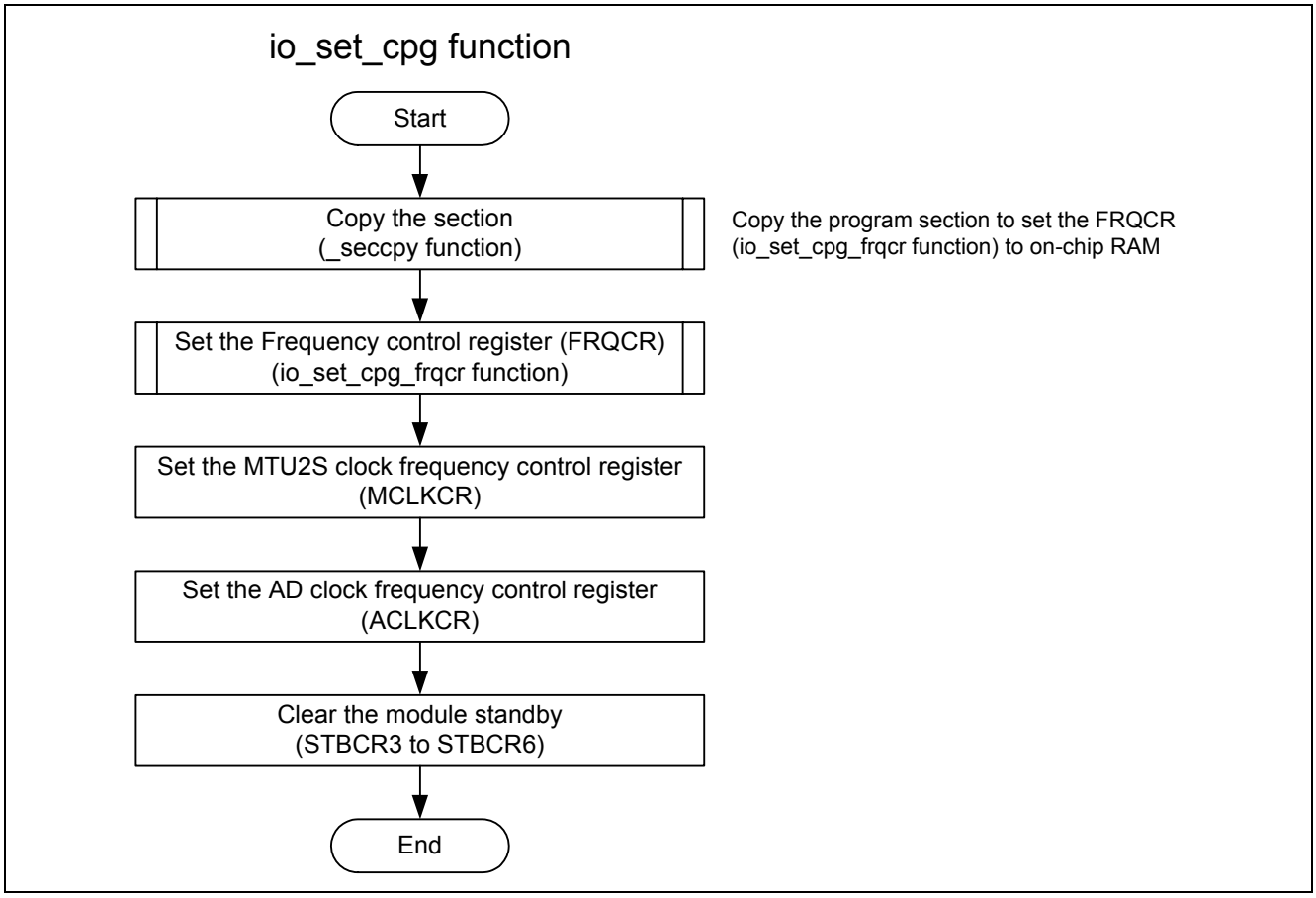


Figure 2 Flow Chart for Setting the CPG (io_set_cpg function)

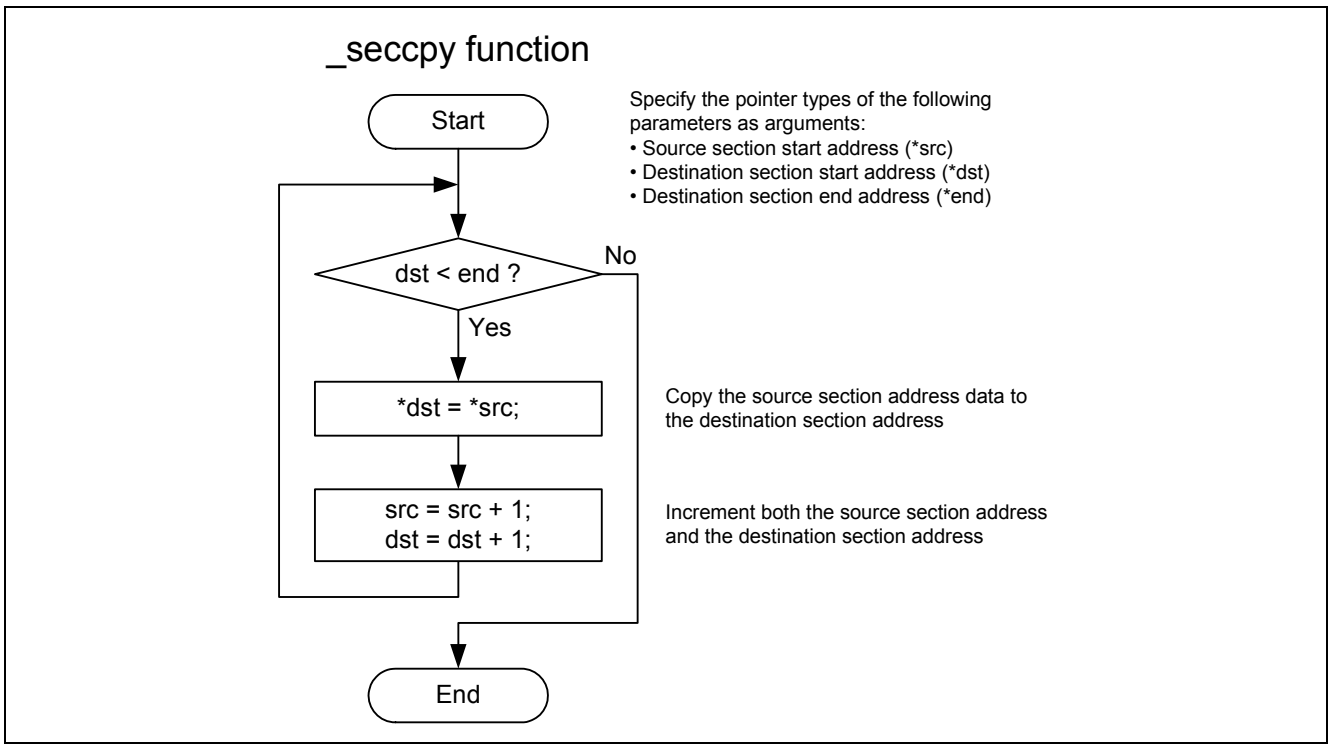


Figure 3 Flow Chart for Copying the Section (_seccpy function)

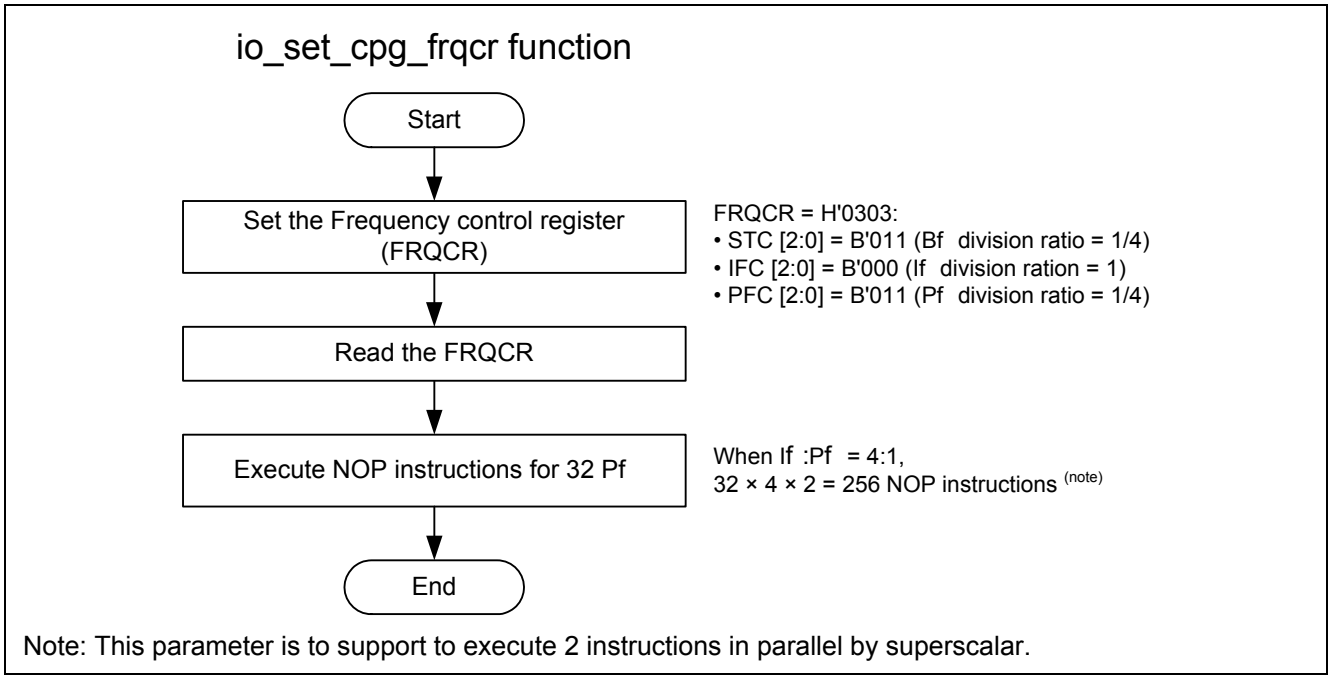


Figure 4 Flow Chart for Setting the FRQCR (io_set_cpg_frqcr function)

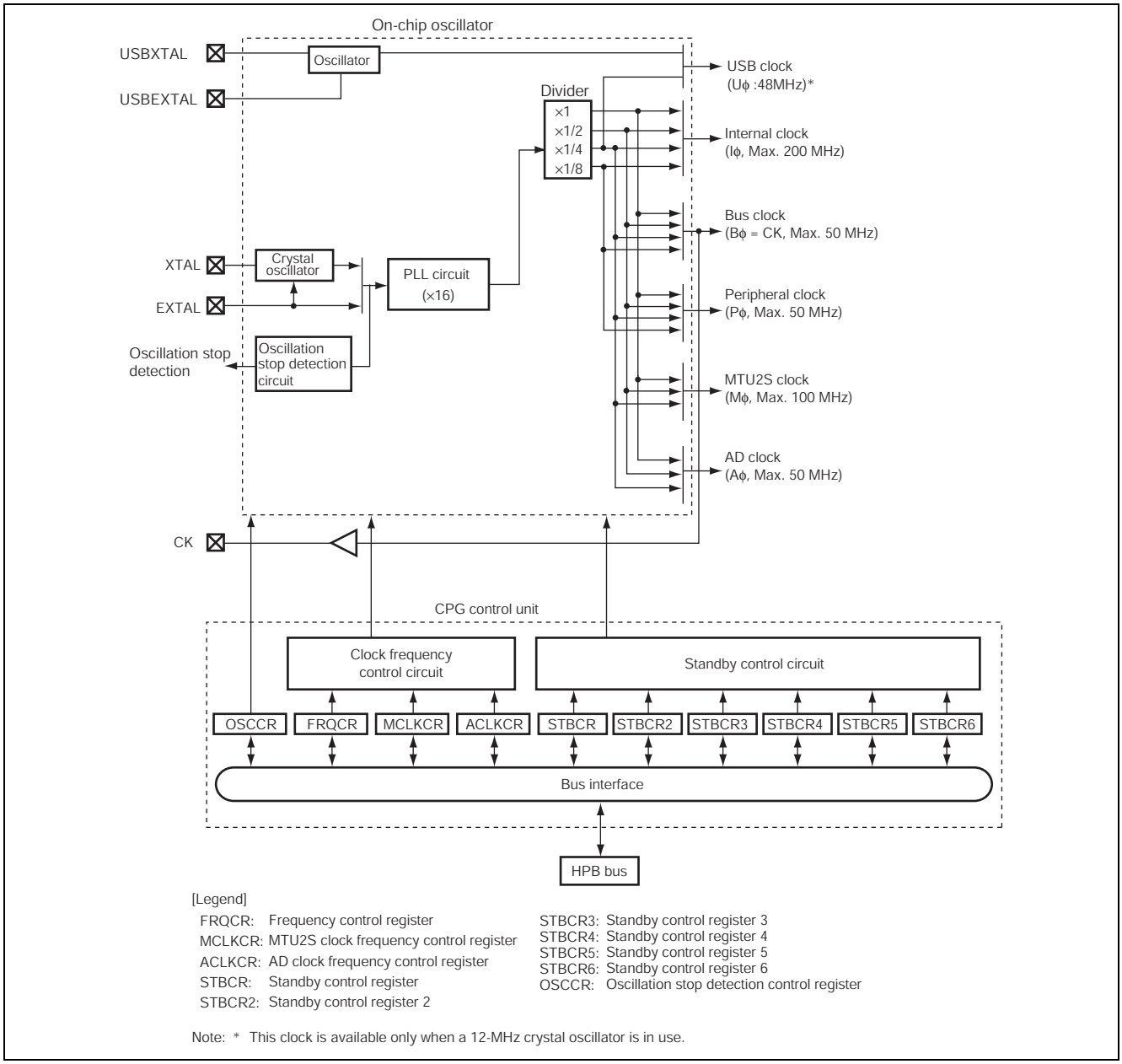
2.2 CPG Operation

CPG generates the internal clock (Iφ), bus clock (Bφ), peripheral clock (Pφ), MTU2S clock (Mφ), and AD clock (Aφ), as well as controlling the low power mode.

The following table gives an overview of the CPG. Figure 5 shows the CPG block diagram.

Table 1 CPG Overview

Item	Description	
Generate clock	• Internal clock (Iφ):	Used by the CPU
	• Bus clock (Bφ):	Used by the external bus interface
	• Peripheral clock (Pφ):	Used by the internal peripheral module
	• MTU2S clock (Mφ):	Used by the MTU2S
	• AD clock (Aφ):	Used by the ADC module
Change frequency	• Sets frequencies for clocks independently using the PLL (Phase Locked Loop) and divider circuits in the CPG. • Changes frequency by software using the frequency control registers (FRQCR, MCLKCR, and ACLKCR).	
Control the low power mode	Stops clock in sleep mode or software standby mode. Stops the module specified by module standby function.	



[Legend]

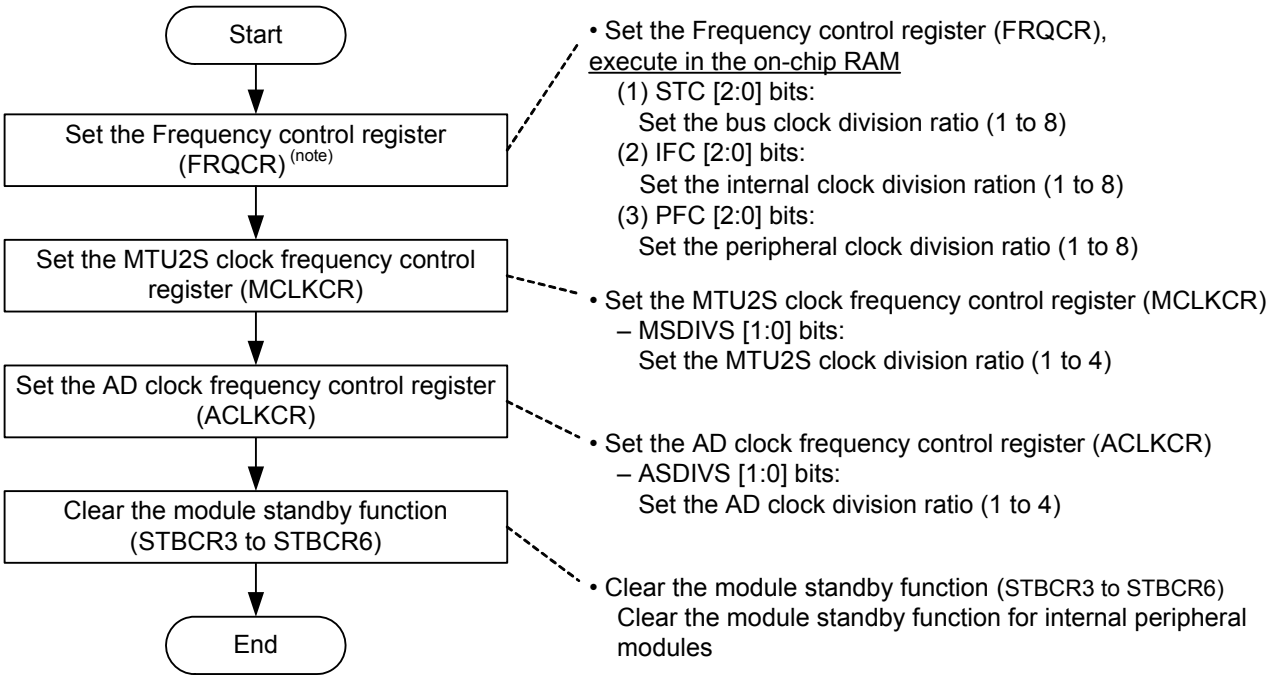
FRQCR: Frequency control register
MCLKCR: MTU2S clock frequency control register
ACLKCR: AD clock frequency control register
STBCR: Standby control register
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4
STBCR5: Standby control register 5
STBCR6: Standby control register 6
OSCCR: Oscillation stop detection control register

Note: * This clock is available only when a 12-MHz crystal oscillator is in use.

Figure 5 CPG Block Diagram

2.3 CPG Setting

The figure below shows the flow chart of setting CPG. Internal peripheral modules are in module standby mode after the reset is canceled. The sample program clears the module standby function for internal peripheral module after setting the Frequency control register (FRQCR), MTU2S clock frequency control register (MCLKCR), and AD clock frequency control register (ACLKCR). For details on these registers, refer to the SH7216 Group Hardware Manual.



Note: Make sure to set the FRQCR in the program located in the on-chip RAM. FRQCR can only be accessed in words. Read the FRQCR and verify if its value is the same as the set value, and then execute NOP instructions for 32 Pφ. This application reads the FRQCR immediately after setting the FRQCR, and executes NOP instructions for 32 Pφ (Refer to Figure 4 FRQCR flow chart).

Figure 6 Flow Chart of CPG Setting

2.4 Setting in the Sample Program

Table 2 lists the setting in the sample program. Table 3 and Table 4 list register settings for each module.

Table 2 Module Setting in the Sample Program

Module	Setting
Floating point status/control unit (FPU)	• Precision mode Executes floating-point instructions in single-precision • Round mode Round to zero
Clock pulse generator (CPG)	• Clock frequency (input clock is 12.5 MHz) — Internal clock: 200 MHz — Bus clock: 50 MHz — Peripheral clock: 50 MHz — MTU2S clock: 100 MHz — AD clock: 50 MHz • Modules cleared the module standby function MTU2S, MTU2, IIC3, ADC0, ADC1, CMT, E-DMAC, EtherC, SCIF3, SCI0, SCI1, SCI2, SCI4, RSPI, USB, RCAN-ET

Table 3 CPG Register Settings (1/2)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0303	• STC[2:0] = "B'011": Bus clock (Bφ) division ratio: 4 • IFC[2:0] = "B'000": Internal clock (Iφ) division ratio = 1 • PFC[2:0] = "B'011": Peripheral clock (Pφ) division ratio = 4
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	• MSDIVS[1:0] = "B'01": MTU2S clock (Mφ) division ratio = 2
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'43	• ASDIVS[1:0] = "B'11": AD clock (Aφ) division ratio = 4

Table 4 CPG Register Settings (2/2)

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFE 0408	H'12	• HIZ = "0": The pin state is held in software standby mode • MSTP36 = "0": MTU2S is operating • MSTP35 = "0": MTU2 is operating • MSTP33 = "0": IIC3 is operating • MSTP32 = "0": ADC0 is operating • MSTP30 = "0": Flash memory is operating
Standby control register 4 (STBCR4)	H'FFFE 040C	H'E2	• MSTP44 = "0": SCIF3 is operating • MSTP42 = "0": CMT is operating • MSTP40 = "0": E-DMAC and Ether-C are operating
Standby control register 5 (STBCR5)	H'FFFE 0418	H'12	• MSTP57 = "0": SCI0 is operating • MSTP56 = "0": SCI1 is operating • MSTP55 = "0": SCI2 is operating • MSTP53 = "0": SCI4 is operating • MSTP52 = "0": ADC1 is operating • MSTP50 = "0": RSPI is operating
Standby control register 6 (STBCR6)	H'FFFE 041C	H'8F	• USBSEL = "1": Selects the USB oscillator as the USB clock source • MSTP66 = "0": USB is operating • USBCLK = "0": USB oscillator is operating • MSTP64 = "0": RCAN-ET is operating

Supplement: About the ROM support function

This application copies the program section to set the FRQCR (io_set_cpg_frqcr function) from the on-chip ROM to on-chip RAM. The ROM support function must be set by the C compiler optimizing linkage editor to add such copy processing.

On the [Build] menu of the High-performance Embedded Workshop, open the [SuperH RISC engine Standard Toolchain] dialog box, and select [Link/Library] tab. Select "Output" from the "Category" drop-down list, and specify the "Show entries for" as "ROM to RAM mapped sections". Click "Add", specify the source section as the ROM section, and the destination section as the RAM section. Before setting the ROM support function, set where to allocate sections both in the source and destination in the "Category" drop-down list on the [Link/Library] tab. This application sets "PURAM" as the program section to set the FRQCR, and "RPURAM" as the destination RAM section.

Figure 7 shows an example of setting the ROM support function. For more information, refer to the SuperH C/C++ Compiler Package V.9.01 User's Manual.

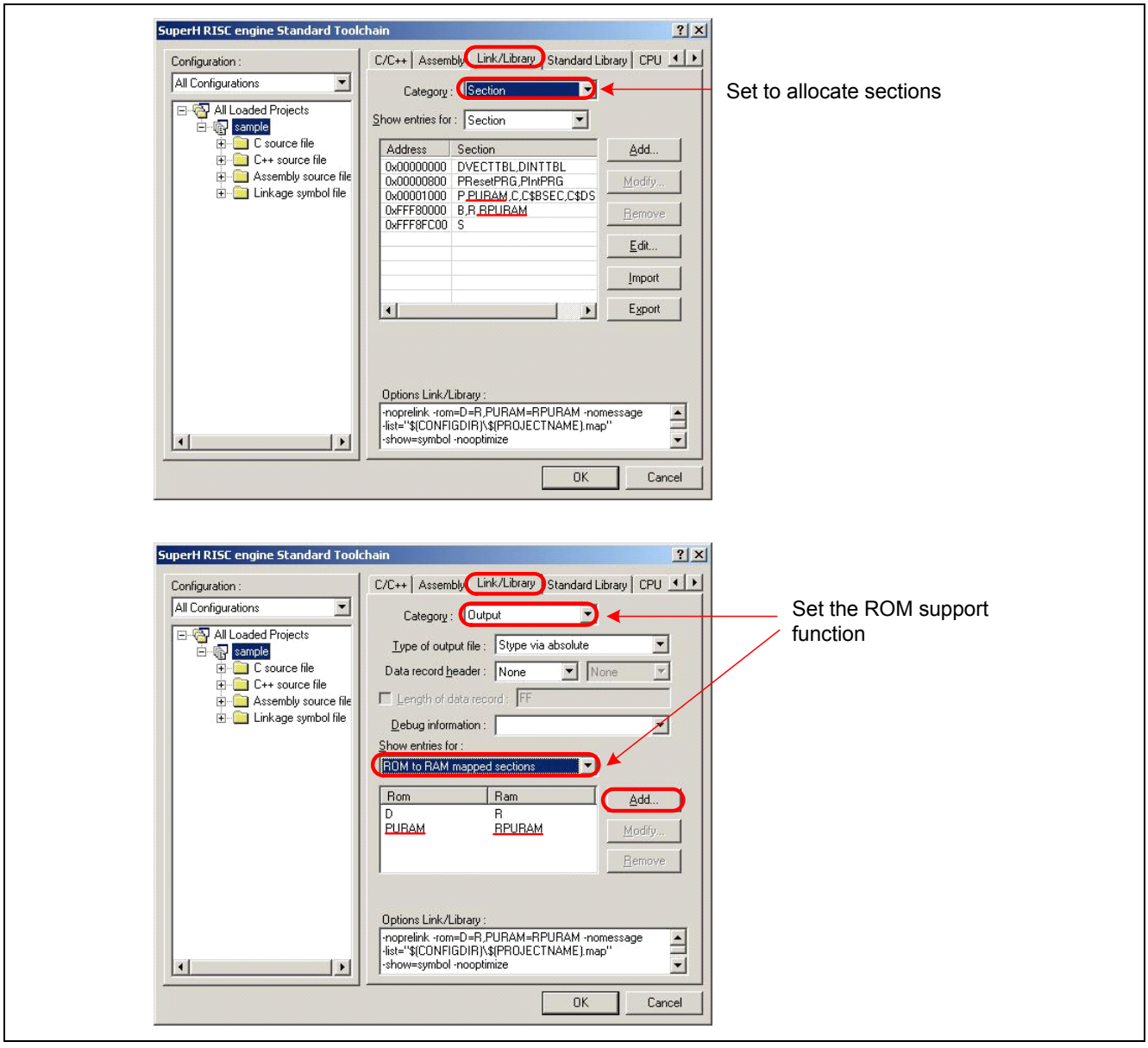


Figure 7 Example to Set the ROM Support Function

3. Sample Program Listing

3.1 Sample Program Listing "resetprg.c" (1/3)

```
1       /***********************************************************************
2       *   DISCLAIMER
3       *
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5       *   intended for use with Renesas products.  No other uses are authorized.
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16      *   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
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26      *   http://www.renesas.com/disclaimer
27      ***********************************************************************
28      *   (C) 2009(2010) Renesas Electronics Corporation. All rights reserved.
29      *""FILE COMMENT""************ Technical reference data *************************
30      *   System Name : SH7216 Sample Program
31      *   File Name   : resetprg.c
32      *   Abstract    : SH7216 Initial Setting
33      *   Version     : 1.04.00
34      *   Device      : SH7216
35      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36      *               : C/C++ compiler package for the SuperH RISC engine family
37      *               :                             (Ver.9.03 Release00).
38      *   OS          : None
39      *   H/W Platform: R0K572167 (CPU board)
40      *   Description :
41      ***********************************************************************
42      *   History     : Jul.29,2009 Ver.1.00.00
43      *               : Dec.28,2009 Ver.1.01.00  Comment correction
44      *               : Jan.28,2010 Ver.1.02.00  - Comment correction (Tool-Chain Ver.)
45      *               :                          - Era name update (2009 -> 2010)
46      *               : Apr.06,2010 Ver.1.03.00  Changing the corporate name and
47      *               :                           the copyright format
48      *               : Apr.23,2010 Ver.1.04.00  Comment correction
49      *""FILE COMMENT END""*************************************************************/
```

3.2 Sample Program Listing "resetprg.c" (2/3)

```
50    #include <machine.h>
51    #include <_h_c_lib.h>
52    #include "stacksct.h"
53    #include "iodefine.h"
54
55    /* ==== Macro definition ==== */
56    #define FPSCR_Init 0x00040001
57    #define SR_Init    0x000000F0
58    #define INT_OFFSET 0x10
59
60    /* ==== Prototype declaration ==== */
61    void PowerON_Reset_PC(void);
62    void Manual_Reset_PC(void);
63
64    /* ==== External reference declaration ==== */
65    /* ---- Function prototype ---- */
66    extern void main(void);
67    extern void HardwareSetup(void);
68    /* ---- Global variable ---- */
69    extern unsigned int INT_Vectors;
70
71    /* ==== Section name changed to ResetPRG ==== */
72    #pragma section ResetPRG
73
74    /* ==== Entry function specified ==== */
75    #pragma entry PowerON_Reset_PC
76
77    /*""FUNC COMMENT""*****************************************************************
78     * ID           :
79     * Outline      : CPU initialization
80     *-----------------------------------------------------------------------------
81     * Include      : <machine.h>, <_h_c_lib.h>, and "iodefine.h"
82     *-----------------------------------------------------------------------------
83     * Declaration  : void PowerON_Reset_PC(void);
84     *-----------------------------------------------------------------------------
85     * Description  : Executes the CPU initialization processing to register
86     *              : the power-on reset vector to the exception vector table.
87     *-----------------------------------------------------------------------------
88     * Argument     : void
89     *-----------------------------------------------------------------------------
90     * Return Value : void
91     *-----------------------------------------------------------------------------
92     * Note         : This function is executed first after power-on reset.
93     *""FUNC COMMENT END""*************************************************************/
94    void PowerON_Reset_PC(void)
95    {
96      /* ==== Floating Point Status/Control Register setting ==== */
97      set_fpscr(FPSCR_Init);
98
99      /* ==== Hardware initialization ==== */
100     HardwareSetup();            /* HardwareSetup function */
```

3.3 Sample Program Listing "resetprg.c" (3/3)

```
101
102     /* ==== Sections initialization ==== */
103     _INITSCT();
104
105     /* ==== Vector Base Register setting ==== */
106     set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));
107
108     /* ==== IO library initialization ==== */
109     _INIT_IOLIB();
110
111     /* ==== Status Register setting ==== */
112     set_cr(SR_Init);
113     nop();
114
115     /* ==== Bunk Number Register setting ==== */
116     INTC.IBNR.BIT.BE = 1;           /* Use of register banks enabled for all */
117                                 /*  interrupts except NMI and user break */
118
119     /* ==== Interrupt mask bits clear ==== */
120     set_imask(0);
121
122     /* ==== Main function call ==== */
123     main();
124
125     /* ==== Sleep instruction execution ==== */
126     sleep();
127   }
128
129   //#pragma entry Manual_Reset_PC       /* Remove the comment when you use Manual Reset */
130   /*""FUNC COMMENT""*****************************************************************
131    * ID           :
132    * Outline      : Manual reset processing
133    *-----------------------------------------------------------------------------
134    * Include      :
135    *-----------------------------------------------------------------------------
136    * Declaration  : void Manual_Reset_PC(void);
137    *-----------------------------------------------------------------------------
138    * Description  : Registers the manual reset vector to the exception vector table.
139    *-----------------------------------------------------------------------------
140    * Argument     : void
141    *-----------------------------------------------------------------------------
142    * Return Value : void
143    *-----------------------------------------------------------------------------
144    * Note         : This sample does not describe the processing content at all.
145    *              : Add the program in this function as needed.
146    *""FUNC COMMENT END""*************************************************************/
147   void Manual_Reset_PC(void)
148   {
149     /* NOP */
150   }
151
152   /* END of File */
```

3.4 Sample Program Listing "hwsetup.c" (1/2)

```
1    /***********************************************************************
2    *   DISCLAIMER
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27   ***********************************************************************
28   *   (C) 2009(2010) Renesas Electronics Corporation. All rights reserved.
29   *""FILE COMMENT""************ Technical reference data *************************
30   *   System Name : SH7216 Sample Program
31   *   File Name   : hwsetup.c
32   *   Abstract    : Hardware Function Initial Setting
33   *   Version     : 1.03.00
34   *   Device      : SH7216
35   *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36   *               : C/C++ compiler package for the SuperH RISC engine family
37   *               :                               (Ver.9.03 Release00).
38   *   OS          : None
39   *   H/W Platform: R0K572167 (CPU board)
40   *   Description :
41   ***********************************************************************
42   *   History     : Jul.28,2009 Ver.1.00.00
43   *               : Dec.28,2009 Ver.1.01.00  Comment correction
44   *               : Jan.28,2010 Ver.1.02.00  - Comment correction (Tool-Chain Ver.)
45   *               :                          - Era name update (2009 -> 2010)
46   *               : Apr.06,2010 Ver.1.03.00  Changing the corporate name and
47   *               :                           the copyright format
48   *""FILE COMMENT END""*********************************************************/
49   #include "iodefine.h"
50
```

3.5 Sample Program Listing "hwsetup.c" (2/2)

```
51    /* ==== Prototype declaration ==== */
52    void HardwareSetup(void);
53
54    /* ==== External reference ==== */
55    /* ---- Function prototype ---- */
56    extern void io_set_cpg(void);
57    extern void io_init_sdram(void);
58
59    /*""FUNC COMMENT""*****************************************************************
60     * ID           :
61     * Outline      : Hardware initialization
62     *-----------------------------------------------------------------------------
63     * Include      :
64     *-----------------------------------------------------------------------------
65     * Declaration  : void HardwareSetup(void);
66     *-----------------------------------------------------------------------------
67     * Description  : Initializes the hardware function.
68     *-----------------------------------------------------------------------------
69     * Argument     : void
70     *-----------------------------------------------------------------------------
71     * Return Value : void
72     *-----------------------------------------------------------------------------
73     * Note         : None
74     *""FUNC COMMENT END""*************************************************************/
75    void HardwareSetup(void)
76    {
77      /* ==== CPG setting ==== */
78      io_set_cpg();
79
80    #if 0      /* Enable this line when you use external SDRAM */
81      /* ==== SDRAM area setting ==== */
82      io_init_sdram();
83    #endif
84    }
85
86    /* End of File */
```

3.6 Sample Program Listing "cpg.c" (1/5)

```
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*
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*   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
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*
*   TO THE MAXIMUM EXTENT PERMITTED NOT PROHIBITED BY LAW, NEITHER RENESAS
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*   http://www.renesas.com/disclaimer
***********************************************************************
*   (C) 2009(2010) Renesas Electronics Corporation. All rights reserved.
*""FILE COMMENT""*********** Technical reference data *************************
*   System Name : SH7216 Sample Program
*   File Name   : cpg.c
*   Abstract    : CPG Setting Processing
*   Version     : 1.04.00
*   Device      : SH7216
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
*               : C/C++ compiler package for the SuperH RISC engine family
*               :                               (Ver.9.03 Release00).
*   OS          : None
*   H/W Platform: R0K572167 (CPU board)
*   Description :
***********************************************************************
*   History     : Jun.29,2009 Ver.1.00.00
*               : Dec.28,2009 Ver.1.01.00  Comment correction
*               : Apr.02,2010 Ver.1.02.00  - Correcting the MSTP34 bit to
*               :                             a reserve bit in STBCR3
*               :                          - Comment correction (Tool-Chain Ver.)
*               :                          - Era name update (2009 -> 2010)
*               : Apr.06,2010 Ver.1.03.00  Changing the corporate name and
*               :                           the copyright format
*               : Apr.23,2010 Ver.1.04.00  - Dividing FRQCR setting into
*               :                             subroutine "io_set_cpg_frqcr"
*               :                             which is allocated to on-chip RAM
*               :                          - Adding processing of section copy
*               :                             function "_seccpy"
*""FILE COMMENT END""*****************************************************/
```

3.7 Sample Program Listing "cpg.c" (2/5)

```
56    #include <machine.h>
57    #include "iodefine.h"
58
59    /* ==== Prototype declaration ==== */
60    void io_set_cpg(void);
61    void io_set_cpg_frqcr(void);
62    static void _seccpy(unsigned long *src, unsigned long *dst, unsigned long *end);
63
64    /*""FUNC COMMENT""*****************************************************************
65     * ID           :
66     * Outline      : CPG setting
67     *-----------------------------------------------------------------------------
68     * Include      : "iodefine.h"
69     *-----------------------------------------------------------------------------
70     * Declaration  : void io_set_cpg(void);
71     *-----------------------------------------------------------------------------
72     * Description  : Initializes the clock pulse generator (CPG) as follows:
73     *              :   I-clock = 200MHz, B-clock = 50MHz, P-clock = 50MHz,
74     *              :   M-clock = 100MHz, and A-clock = 50MHz.
75     *              : And then supplies clock to all peripheral modules except USB.
76     *-----------------------------------------------------------------------------
77     * Argument     : void
78     *-----------------------------------------------------------------------------
79     * Return Value : void
80     *-----------------------------------------------------------------------------
81     * Note         : This function is an example of CPG setting at the input clock
82     *              : of 12.5MHz.
83     *""FUNC COMMENT END""*************************************************************/
84    void io_set_cpg(void)
85    {
86      /* ==== CPG setting ==== */
87      /* ---- Program section initialization for FRQCR setting ---- */
88      _seccpy((unsigned long *)__sectop("PURAM"), (unsigned long *)__sectop("RPURAM"),
89           (unsigned long *)__secend("RPURAM"));
90           /* Program section copying from "PURAM" to on-chip RAM */
91      /* ---- FRQCR setting (Running on-chip RAM) ---- */
92      io_set_cpg_frqcr();             /* Clock-in = 12.5MHz */
93                                  /* - I-clock = 200MHz */
94                                  /* - B-clock = 50MHz */
95                                  /* - P-clock = 50MHz */
96      /* ---- MCLKCR setting ---- */
97      CPG.MCLKCR.BYTE = 0x41;         /* M-clock = 100MHz */
98      /* ---- ACLKCR setting ---- */
99      CPG.ACLKCR.BYTE = 0x43;         /* A-clock = 50MHz */
100
101
```

3.8 Sample Program Listing "cpg.c" (3/5)

```
102      /* ==== Module standby clear ==== */
103      /* ---- STBCR3 setting ---- */
104      STB.CR3.BYTE = 0x12;        /* HIZ, MTU2S, MTU2, Reserve(1), */
105                                  /* IIC3, ADC0, Reserve(1), FLASH */
106      /* ---- STBCR4 setting ---- */
107      STB.CR4.BYTE = 0xe2;        /* Reserve(1), Reserve(1), Reserve(1), SCIF3, */
108                                  /* Reserve(0), CMT, Reserve(1), EtherC        */
109      /* ---- STBCR5 setting ---- */
110      STB.CR5.BYTE = 0x12;        /* SCI0, SCI1, SCI2, Reserve(1), */
111                                  /* SCI4, ADC1, Reserve(1), RSPI  */
112      /* ---- STBCR6 setting ---- */
113      STB.CR6.BYTE = 0x8f;        /* USB: Using USBXTAL/USBEXTAL for USBCLK. */
114                                  /* RCAN-ET */
115    }
116
117    /* ==== Section name changed to URAM ==== */
118    #pragma section URAM
119    /*""FUNC COMMENT""*****************************************************************
120     * ID           :
121     * Outline      : FRQCR register setting
122     *-----------------------------------------------------------------------------
123     * Include      : <machine.h> and "iodefine.h"
124     *-----------------------------------------------------------------------------
125     * Declaration  : void io_set_cpg_frqcr(void);
126     *-----------------------------------------------------------------------------
127     * Description  : Initializes the clock pulse generator (CPG) as follows:
128     *              :   I-clock = 200MHz, B-clock = 50MHz, P-clock = 50MHz.
129     *-----------------------------------------------------------------------------
130     * Argument     : void
131     *-----------------------------------------------------------------------------
132     * Return Value : void
133     *-----------------------------------------------------------------------------
134     * Note         : - This function needs to be run on internal RAM.
135     *              : - This function is also an example of CPG setting at the
136     *              :   input clock of 12.5MHz.
137     *""FUNC COMMENT END""*************************************************************/
138    void io_set_cpg_frqcr(void)
139    {
140      volatile unsigned short dummy;
141
```

3.9 Sample Program Listing "cpg.c" (4/5)

```
142     /* ==== FRQCR setting ==== */
143     CPG.FRQCR.WORD = 0x0303;    /* Clock-in = 12.5MHz */
144                                 /* - I-clock = 200MHz */
145                                 /* - B-clock = 50MHz */
146                                 /* - P-clock = 50MHz */
147     dummy = CPG.FRQCR.WORD;         /* FRQCR readout */
148     /* ---- 256 NOPs for 32 x P-clock (I:P = 4:1) ---- */
149     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
150     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
151     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
152     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
153     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
154     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
155     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
156     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
157     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
158     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
159     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
160     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
161     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
162     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
163     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
164     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
165     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
166     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
167     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
168     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
169     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
170     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
171     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
172     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
173     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
174     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
175     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
176     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
177     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
178     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
179     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
180     nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
181   }
182   #pragma section    /* End of "URAM" section */
183
```

3.10 Sample Program Listing "cpg.c" (5/5)

```
184    /*""FUNC COMMENT""*****************************************************************
185     * ID           :
186     * Outline      : Section copy function
187     *-------------------------------------------------------------------------------
188     * Include      :
189     *-------------------------------------------------------------------------------
190     * Declaration  : static void _seccpy(unsigned long *src, unsigned long *dst,
191     *              :                     unsigned long *end);
192     *-------------------------------------------------------------------------------
193     * Description  : Copies a source section to specified target.
194     *-------------------------------------------------------------------------------
195     * Argument     : unsigned long *src ; Initial address of source section
196     *              : unsigned long *dst ; Initial address of target section
197     *              : unsigned long *end ; Final address of target section
198     *-------------------------------------------------------------------------------
199     * Return Value : void
200     *-------------------------------------------------------------------------------
201     * Note         : None
202     *""FUNC COMMENT END""*************************************************************/
203    static void _seccpy(unsigned long *src, unsigned long *dst, unsigned long *end)
204    {
205      while(dst < end){
206        *dst++ = *src++;
207      }
208    }
209
210    /* End of File */
```

3.11 Sample Program Listing "vecttbl.c" (1/2)

```
1    /***********************************************************************
2    *   DISCLAIMER
3    *
4    *   This software is supplied by Renesas Electronics Corp. and is only
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6    *
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25   *   conditions found by accessing the following link:
26   *   http://www.renesas.com/disclaimer
27   ***********************************************************************
28   *   (C) 2009(2010) Renesas Electronics Corporation. All rights reserved.
29   *""FILE COMMENT""************ Technical reference data *************************
30   *   System Name : SH7216 Sample Program
31   *   File Name   : vecttbl.c
32   *   Abstract    : Initialization for Vector Table
33   *   Version     : 1.04.00
34   *   Device      : SH7216
35   *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
36   *               : C/C++ compiler package for the SuperH RISC engine family
37   *               :                               (Ver.9.03 Release00).
38   *   OS          : None
39   *   H/W Platform: R0K572167 (CPU board)
40   *   Description :
41   ***********************************************************************
42   *   History     : Jun.18,2009 Ver.1.00.00
43   *               : Dec.17,2009 Ver.1.01.00  Spelling correction of the inline
44   *               :                           comment: "Vecter" -> "Vector"
45   *               : Dec.28,2009 Ver.1.02.00  Comment correction
46   *               : Jan.28,2010 Ver.1.03.00  - Comment correction (Tool-Chain Ver.)
47   *               :                          - Era name update (2009 -> 2010)
48   *               : Apr.06,2010 Ver.1.04.00  Changing the corporate name and
49   *               :                           the copyright format
50   *""FILE COMMENT END""*****************************************************/
51   #include "vect.h"
52
```

3.12 Sample Program Listing "vecttbl.c" (2/2)

```
53      #pragma section VECTTBL
54      void *RESET_Vectors[] = {
55      // <<VECTOR DATA START (POWER ON RESET)>>
56      // 0 Power On Reset PC
57          (void *)PowerON_Reset_PC,
58      // <<VECTOR DATA END (POWER ON RESET)>>
59      // 1 Power On Reset SP
60          __secend("S"),
61      // <<VECTOR DATA START (MANUAL RESET)>>
62      // 2 Manual Reset PC
63          (void *)Manual_Reset_PC,
64      // <<VECTOR DATA END (MANUAL RESET)>>
65      // 3 Manual Reset SP
66          __secend("S")
67      };
68
69      #pragma section INTTBL
70      void *INT_Vectors[] = {
71      // 4 Illegal code
72          (void *)INT_Illegal_code,

…       …

573     // 255 SCIF SCIF3 TXI3
574         (void *)INT_SCIF_SCIF3_TXI3,
575     // xx Reserved
576         (void *)Dummy
577     };
578
579     /* End of File */
```

4. References

- Software Manual
  SH-2A, SH2A-FPU Software Manual Rev. 3.00
  The latest version can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7216 Group Hardware Manual Rev. 1.01
  The latest version can be downloaded from the Renesas Electronics website.

- Technical Update
  Addition to and correction of errors in the SH7280 Group Hardware Manual and SH7216 Group Hardware Manual (TN-SH7-A727A/E)
  Correction of errors in the SH7216 Group Hardware Manual (TN-SH7-A754A/E)
  Correction of errors in the SH7216 Group Hardware Manual (TN-SH7-A761A/E)
  Amendment to Product Code Lineup in the SH7216 Group Hardware Manual (TN-SH7-A762A/E)
  Limitation on Changes to the Frequency Control Register and Correction of Error in the Hardware Manual (TN-SH7-A769A/E)
  Correction of errors in the Hardware Manual (TN-SH7-A771A/E)
  The latest version can be downloaded from the Renesas Electronics website.

- Development Tool Manual
  SuperH C/C++ Compiler Package V.9.01 User's Manual Rev.1.01
  The latest version can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jun.30.09	–	First edition issued
1.01	Jun.03.10	3	2.1 explanation added and modified
		3, 12	Supplements added
		4 to 6	Flow charts added and modified
		9	Note in Figure 6 modified
		13 to 25	Sample program listing updated
		26	Technical updates added

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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