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April 1\textsuperscript{st}, 2010
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SH7137 Group
Example of Initialization

Summary
This application note gives an example of configuration items to activate the SH7137 Microcomputers (MCUs).

Target Device
SH7137 MCU

Contents

1. Introduction................................................................................................................... 2
2. Applications................................................................................................................ 3
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4. References............................................................................................................... 19
1. Introduction

1.1 Specifications
Configure the clock pulse generator (CPG) after the reset is canceled.

1.2 Modules Used
- Clock pulse generator (CPG)

1.3 Applicable Conditions

<table>
<thead>
<tr>
<th>MCU</th>
<th>SH7137</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>Internal clock: 80 MHz</td>
</tr>
<tr>
<td></td>
<td>Bus clock: 40 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral clock: 40 MHz</td>
</tr>
<tr>
<td>Integrated Development</td>
<td>Renesas Technology Corp.</td>
</tr>
<tr>
<td>Environment</td>
<td>High-performance Embedded Workshop Ver.4.03.00</td>
</tr>
<tr>
<td>C compiler</td>
<td>Renesas Technology SuperH RISC engine Family</td>
</tr>
<tr>
<td></td>
<td>C/C++ compiler package Ver.9.01 Release 01</td>
</tr>
<tr>
<td>Compiler options</td>
<td>Default setting in the High-performance Embedded Workshop</td>
</tr>
<tr>
<td></td>
<td>(-cpu=sh2 -debug -gbr=auto -global_volatile=0 -opt_range=all</td>
</tr>
<tr>
<td></td>
<td>-infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)</td>
</tr>
</tbody>
</table>
2. Applications

Configuration program for the minimum hardware setup is required to execute the main function created in C code. This application note describes the configuration example for the configuration program.

All of the SH7137 application notes assume to use the sample program described in this application note as the configuration program.

2.1 Sample Program

The configuration program consists of several source files such as the resetprg.c, describing the PowerON_Reset_PC function, and the hwsetup.c, describing the hardware setup function. Main source files are as follows.

- resetprg.c
- hwsetup.c
- cpg.c

"resetprg.c" is a source file created on the file automatically generated by the High-performance Embedded Workshop, and describes the PowerON_Reset_PC function. The PowerON_ResetPC function initially executed after the reset is canceled. Its beginning address is set in the reset vector defined by the vecttbl.c.

"hwsetup.c" describes the HardwareSetup function called by the PowerON_Reset_PC function. The HardwareSetup function calls the io_set_cpg function to set the CPG.

"cpg.c" describes the io_set_cpg function which is called from the HardwareSetup function. The io_set_cpg function sets the frequency control registers (FRQCR, MCLKCR, and ACLKCR) to clear the module standby function for internal peripheral modules.

Figure 1 shows flow charts of the PowerON_Reset_PC function, the HardwareSetup function, and the io_set_cpg function.
Example of Initialization

PowerON_Reset_PC function
- Start
- Configure the hardware (HardwareSetup function)
- Initialize sections B and R (_INITSCT function)
- Set the Vector base register (VBR)
- Set the Status register (SR)
- Permit interrupts
- Call the main function
- Execute the sleep instruction
- End

HardwareSetup function
- Start
- Set the CPG (io_set_cpg function)
- End

io_set_cpg function
- Start
- Set the Frequency control register (FRQCR)
- Clear the module standby function (STBCR2 to STBCR5)
- End

Figure 1 Flow Charts of Functions (PowerON_Reset_PC, HardwareSetup, io_set_cpg)
2.2 CPG Operation

CPG generates the internal clock (I\(\phi\)), bus clock (B\(\phi\)), peripheral clock (P\(\phi\)), clocks for MTU2S and MTU2 modules (MI\(\phi\), MP\(\phi\)). It also controls the clock in low power mode.

The following table gives an overview of the CPG. Figure 2 shows the CPG block diagram.

**Table 1 CPG Overview**

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generate clock</td>
<td>• Internal clock (I(\phi)): Used by the CPU</td>
</tr>
<tr>
<td></td>
<td>• Bus clock (B(\phi)): Used by the external bus interface</td>
</tr>
<tr>
<td></td>
<td>• Peripheral clock (P(\phi)): Used by the internal peripheral module</td>
</tr>
<tr>
<td></td>
<td>• MTU2S clock (MI(\phi)): Used by the MTU2S module</td>
</tr>
<tr>
<td></td>
<td>• MTU2 clock (MP(\phi)): Used by the MTU2 module</td>
</tr>
<tr>
<td>Change frequency</td>
<td>• Sets frequencies for internal clock, bus clock, peripheral clock, MTU2S</td>
</tr>
<tr>
<td></td>
<td>clock, and MTU2 clock independently using the divider circuits in the</td>
</tr>
<tr>
<td></td>
<td>CPG.</td>
</tr>
<tr>
<td></td>
<td>• Changes frequency by software using the Frequency control registers (FRQCR).</td>
</tr>
<tr>
<td>Control the low power mode</td>
<td>Stops clock in sleep mode or software standby mode. Stops the module</td>
</tr>
<tr>
<td></td>
<td>specified by module standby function.</td>
</tr>
</tbody>
</table>
Figure 2 CPG Block Diagram
2.3 CPG Setting

The figure below shows the flow chart of setting CPG. Internal peripheral modules are in module standby mode after the reset is canceled. The sample program clears the module standby function for internal peripheral module after setting the Frequency control register (FRQCR). For details on these registers, refer to the SH7137 Group Hardware Manual.

![Flow Chart of CPG Setting](image)

- **Figure 3 Flow Chart of CPG Setting**
2.4 Setting in the Sample Program

Table 2 lists the setting in the sample program. Table 3 and Table 4 list register settings for each module.

### Table 2 Module Setting in the Sample Program

<table>
<thead>
<tr>
<th>Module</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pulse generator (CPG)</td>
<td>• Clock frequency (input clock is 10 MHz)</td>
</tr>
<tr>
<td></td>
<td>Internal clock: 80 MHz</td>
</tr>
<tr>
<td></td>
<td>Bus clock: 40 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral clock: 40 MHz</td>
</tr>
<tr>
<td></td>
<td>MTU2S clock: 80 MHz</td>
</tr>
<tr>
<td></td>
<td>MTU2 clock: 40 MHz</td>
</tr>
<tr>
<td></td>
<td>• Modules cleared the module standby function</td>
</tr>
<tr>
<td></td>
<td>DTC, I²C2, SCI_0, SCI_1, SCI_2, SSU, RCAN-ET_0, MTU2S,</td>
</tr>
<tr>
<td></td>
<td>MTU2, CMT, A/D_0, A/D_1, AUD, UBC</td>
</tr>
</tbody>
</table>

### Table 3 CPG Register Settings (1/2)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency control register (FRQCR)</td>
<td>H'FFFF E800</td>
<td>H'0241</td>
<td>• IFC[2:0] = &quot;B'000&quot;:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Internal clock (Iφ) division ratio = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BFC[2:0] = &quot;B'001&quot;:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bus clock (Bφ) division ratio = 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PFC[2:0] = &quot;B'001&quot;:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Peripheral (Pφ) clock division ratio = 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• MIFC[2:0] = &quot;B'000&quot;:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MTU2S clock (MIφ) division ratio = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• MPFC[2:0] = &quot;B'001&quot;:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MTU2 clock (MPφ) division ratio = 2</td>
</tr>
</tbody>
</table>
### Table 4 CPG Register Settings (2/2)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby control register 2</td>
<td>H'FFFF E804</td>
<td>H'28</td>
<td>- MSTP7 = &quot;0&quot;: RAM is operating</td>
</tr>
<tr>
<td>(STBCR2)</td>
<td></td>
<td></td>
<td>- MSTP6 = &quot;0&quot;: ROM is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP4 = &quot;0&quot;: DTC is operating</td>
</tr>
<tr>
<td>Standby control register 3</td>
<td>H'FFFF E806</td>
<td>H'42</td>
<td>- MSTP15 = &quot;0&quot;: i²C2 is operating</td>
</tr>
<tr>
<td>(STBCR3)</td>
<td></td>
<td></td>
<td>- MSTP13 = &quot;0&quot;: SCI_2 is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP12 = &quot;0&quot;: SCI_1 is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP11 = &quot;0&quot;: SCI_0 is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP10 = &quot;0&quot;: SSU is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP8 = &quot;0&quot;: RCAN-ET_0 is operating</td>
</tr>
<tr>
<td>Standby control register 4</td>
<td>H'FFFF E808</td>
<td>H'07</td>
<td>- MSTP23 = &quot;0&quot;: MTU2S is operating</td>
</tr>
<tr>
<td>(STBCR4)</td>
<td></td>
<td></td>
<td>- MSTP22 = &quot;0&quot;: MTU2 is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP21 = &quot;0&quot;: CMT is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP20 = &quot;0&quot;: A/D_1 is operating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- MSTP19 = &quot;0&quot;: A/D_0 is operating</td>
</tr>
<tr>
<td>Standby control register 5</td>
<td>H'FFFF E80A</td>
<td>H'00</td>
<td>- MSTP25 = &quot;0&quot;: AUD is operating</td>
</tr>
<tr>
<td>(STBCR5)</td>
<td></td>
<td></td>
<td>- MSTP24 = &quot;0&quot;: UBC is operating</td>
</tr>
</tbody>
</table>
3. Sample Program Listing

3.1 Sample Program Listing "resetprg.c" (1/3)

```c
#include <machine.h>
#include <_h_c_lib.h>
#include "stacksct.h"
#include "iodefine.h"

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* FILE COMMENT"*********** Technical reference data ***********************
* System Name : SH7137 Sample Program
* File Name    : resetprg.c
* Abstract     : SH7137 Initial Setting
* Version      : 1.00.00
* Device       : SH7137
* Tool-Chain   : High-performance Embedded Workshop (Ver.4.03.00).
*              : C/C++ compiler package for the SuperH RISC engine family
*              : (Ver.9.01 Release01).
* OS           : None
* H/W Platform: M3A-HS37 (CPU board)
* Description :
* //**********************************************************************
* History      : Jun.18,2009 Ver.1.00.00
* "FILE COMMENT END"***********************************************/
#include <machine.h>
#include <_h_c_lib.h>
#include "stacksct.h"
#include "iodefine.h"
```
3.2 Sample Program Listing "resetprg.c" (2/3)

```c
/* ==== Macro definition ==== */
#define SR_Init 0x000000F0
#define INT_OFFSET 0x10

/* ==== Prototype declaration ==== */
void PowerON_Reset_PC(void);
void Manual_Reset_PC(void);

/* ==== External reference declaration ==== */
/* ---- Function prototype ---- */
extern void HardwareSetup(void);
extern void main(void);
/* ---- Global variable ---- */
extern unsigned int INT_Vectors;

/* ==== Section name changed to ResetPRG ==== */
#pragma section ResetPRG

/* ==== Entry function specified ==== */
#pragma entry PowerON_Reset_PC

/*"FUNC COMMENT"******************************************************************************
* ID             :
* Outline       : CPU initialization
*-------------------------------------------------------------------------------
* Include       : <machine.h> and <_h_c_lib.h>
*-------------------------------------------------------------------------------
* Declaration  : void PowerON_Reset_PC(void);
*-------------------------------------------------------------------------------
* Description  : Executes the CPU initialization processing to register
*                 : the power-on reset vector to the exception vector table.
*-------------------------------------------------------------------------------
* Argument      : void
*-------------------------------------------------------------------------------
* Return Value : void
*-------------------------------------------------------------------------------
* Note          : This function is executed first after power-on reset.
*""FUNC COMMENT END"**************************************************************************/

void PowerON_Reset_PC(void)
{
    /* ==== Hardware initialization ==== */
    HardwareSetup(); /* HardwareSetup function */

    /* ==== B and R sections initialization ==== */
    _INITSCT();
```
3.3 Sample Program Listing "resetprg.c" (3/3)

```c
/* ==== Vector Base Register setting ==== */
set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));

/* ==== Status Register initialization ==== */
set_cr(SR_Init);
nop();

/* ==== Interrupt enabling ==== */
set_imask(0); /* Interrupt mask bits clear */

/* ==== Main function call ==== */
main();

/* ==== Sleep instruction execution ==== */
sleep();

} /* END of File */

#pragma entry Manual_Reset_PC    /* Remove the comment when you use Manual Reset */
/*"FUNC COMMENT"************************************************************
* ID             :
* Outline       : Manual reset processing
*------------------------------------------------------------------------
* Include       :
*------------------------------------------------------------------------
* Declaration  : void Manual_Reset_PC(void);
*------------------------------------------------------------------------
* Description  : Registers the manual reset vector to the exception vector table.
*------------------------------------------------------------------------
* Argument      : void
*------------------------------------------------------------------------
* Return Value : void
*------------------------------------------------------------------------
* Note           : This sample does not describe the processing content at all.
*                 : Add the program in this function as needed.
*"FUNC COMMENT END"**********************************************************/
void Manual_Reset_PC(void)
{
    /* NOP */
}

/* END of File */
```
### 3.4 Sample Program Listing "hwsetup.c" (1/2)

```c
#include "iodefine.h"

/* === Prototype declaration === */

void HardwareSetup(void);
```

3.5 Sample Program Listing "hwsetup.c" (2/2)

```c
/* ==== External reference ==== */
/* ---- Function prototype ---- */
extern void io_set_cpg(void);

;/*"FUNC COMMENT"********************************************************************
* ID             :
* Outline       : Hardware initialization
*------------------------------------------------------------------------------
* Include       :
*------------------------------------------------------------------------------
* Declaration  : void HardwareSetup(void);
*------------------------------------------------------------------------------
* Description  : Initializes the hardware function.
*------------------------------------------------------------------------------
* Argument      : void
*------------------------------------------------------------------------------
* Return Value : void
*------------------------------------------------------------------------------
* Note           : None
;"FUNC COMMENT END"********************************************************************/

void HardwareSetup(void)
{
    /* ---- CPG setting ---- */
    io_set_cpg();

    /* End of File */
```
3.6 Sample Program Listing "cpg.c" (1/2)

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* System Name : SH7137 Sample Program
* File Name    : cpg.c
* Abstract     : CPG Setting Processing
* Version      : 1.00.00
* Device       : SH7137
* Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
*             : C/C++ compiler package for the SuperH RISC engine family
*             : (Ver.9.01 Release01).
* OS            : None
* H/W Platform: M3A-HS37 (CPU board)
* Description :
******************************************************************************
* History      : Jun.18,2009 Ver.1.00.00
******************************************************************************
* FILE COMMENT END******************************************************************************
#include "iodefine.h"

/* ==== Prototype declaration ==== */
void io_set_cpg(void);
3.7 Sample Program Listing "cpg.c" (2/2)

```c
/*"FUNC COMMENT"*********************************************************************/
* ID             : 
* Outline       : CPG setting 
*------------------------------------------------------------------------------
* Include       : "iodefine.h" 
*------------------------------------------------------------------------------
* Declaration  : void io_set_cpg(void);
*------------------------------------------------------------------------------
* Description  : Initializes the clock pulse generator (CPG) as follows:
*                 :  I-clock = 80MHz, B-clock = 40MHz, P-clock = 40MHz, 
*                 :  MI-clock = 80MHz, and MP-clock = 40MHz.
*                 : And then supplies clock to all the peripheral modules.
*------------------------------------------------------------------------------
* Argument      : void
*------------------------------------------------------------------------------
* Return Value : void
*------------------------------------------------------------------------------
* Note           : This function is an example of CPG setting at the input clock 
*                 : of 10MHz.
*"FUNC COMMENT END"******************************************************************/

void io_set_cpg(void)
{
    /* ==== CPG setting ==== */
    CFG.FRQCR.WORD = 0x0241;        /* Clock-in = 10MHz */
       /* I-clock = 80MHz */
       /* B-clock = 40MHz */
       /* P-clock = 40MHz */
       /* MI-clock = 80MHz */
       /* MP-clock = 40MHz */
    /* ==== Module Stanby Clear ==== */
    STB.CR2.BYTE = 0x28;            /* RAM, ROM, Reserve(1), DTC, Reserve(0), */
       /* Reserve(0), Reserve(0), Reserve(0) */
    STB.CR3.BYTE = 0x42;            /* IIC2, Reserve(1), SCI_2, SCI_1, SCI_0, */
       /* SSU, Reserve(1), RCAN */
    STB.CR4.BYTE = 0x07;            /* MTU2S, MTU2, CNT, A/D_1, A/D_0, */
       /* Reserve(1), Reserve(1), Reserve(1) */
    STB.CR5.BYTE = 0x00;            /* Reserve(0), Reserve(0), Reserve(0), */
       /* Reserve(0), Reserve(0), Reserve(0), */
       /* AUD, UBC */
}
/* End of File */
```
### 3.8 Sample Program Listing "vecttbl.c" (1/2)

```c
#include "vect.h"
#pragma section VECTTBL

void *RESET_Vectors[] = {
// <<VECTOR DATA START (POWER ON RESET)>>
// 0 Power On Reset PC
(void *)PowerON_Reset_PC,
```

```c
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/* ***FILE COMMENT"*********** Technical reference data ***********"*/
/* System Name : SH7137 Sample Program */
/* File Name : vecttbl.c */
/* Abstract : Initialization for Vector Table */
/* Version : 1.00.00 */
/* Device : SH7137 */
/* Tool-Chain : High-performance Embedded Workshop (Ver.4.03.00). */
/* : C/C++ compiler package for the SuperH RISC engine family */
/* : (Ver.9.01 Release01). */
/* OS : None */
/* H/W Platform: M3A-HS37 (CPU board) */
/* Description : */
/* ************************************************************************* */
/* History : Jun.18,2009 Ver.1.00.00 */
/* ***FILE COMMENT END"*/
#include "vect.h"
```

```c
#pragma section VECTTB
void *RESET_Vectors[] = {
// <<VECTOR DATA START (POWER ON RESET)>>
// 0 Power On Reset PC
(void *)PowerON_Reset_PC,
```
3.9  Sample Program Listing "vecttbl.c" (2/2)

```c
51     // <<VECTOR DATA END (POWER ON RESET)>>
52     // 1 Power On Reset SP
53     __secend("S"),
54     // <<VECTOR DATA START (MANUAL RESET)>>
55     // 2 Manual Reset PC
56     (void *)Manual_Reset_PC,
57     // <<VECTOR DATA END (MANUAL RESET)>>
58     // 3 Manual Reset SP
59     __secend("S")
60 }
61
62 #pragma section INTTBL
63 void *INT_Vectors[] = {
64     // 4 Illegal code
65     (void *)INT_Illegal_code,
66
67     // 255 Reserved
68     (void *)Dummy
69 }
70
70    /* End of File */
```
4. References

- Software Manual
  SH-1/SH2/SH-DSP Software Manual Rev. 7.00
  (Download the latest version from the Renesas website.)

- Hardware Manual
  SH7137 Group Hardware Manual Rev. 2.00
  (Download the latest version from the Renesas website.)
Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
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Revision History

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<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>1.00</td>
<td>Jun. 30, 2009</td>
<td>First edition issued</td>
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