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SH7211 Group

Example of Initialization

Introduction

This application note describes an example of initialization of the SH7211 CPU.

Target Device

SH7211

Contents

1. Preface

1.1 Specifications

The clock pulse generator (CPG), bus state controller (BSC), and pin function controller (PFC) are initialized after release from the reset state.

1.2 Modules Used

- Clock pulse generator (CPG)
- Bus state controller (BSC)
- Pin function controller (PFC)

1.3 Applicable Conditions

- MCU: SH7211
- Operating frequency:
  - Internal clock: 160 MHz
  - Bus clock: 40 MHz
  - Peripheral clock: 40 MHz
  - MTU2S clock: 80 MHz
  - AD clock: 40 MHz
- C compiler: SuperH RISC Engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Technology
- Compiler options: Default settings of the High-performance Embedded Workshop
  -cpu=sh2 -debug -gbr=auto -chgincpath -global_volatile=0
  -opt_range=all -infinite_loop=0 -struct_alloc=1 -nologo

2. Description of the Sample Application

Use of the program for initial settings described in this application note is a precondition for all of the other SH7211 application notes.

2.1 Description of the Sample Program

The initialization program consists of the following two source files:

- resetprg.c
- hwsetup.c

Code for the PowerON_Reset_PC function, which is executed first after release from the reset state, is written in resetprg.c.

Code for the HardwareSetup function, which is called from the PoweON_Reset_PC function, is written in hwsetup.c. Code in the HardwareSetup function includes the individual function calls for the CPG and BSC settings.

Figure 1 shows flows of processing by the PowerON_Reset_PC and HardwareSetup functions.

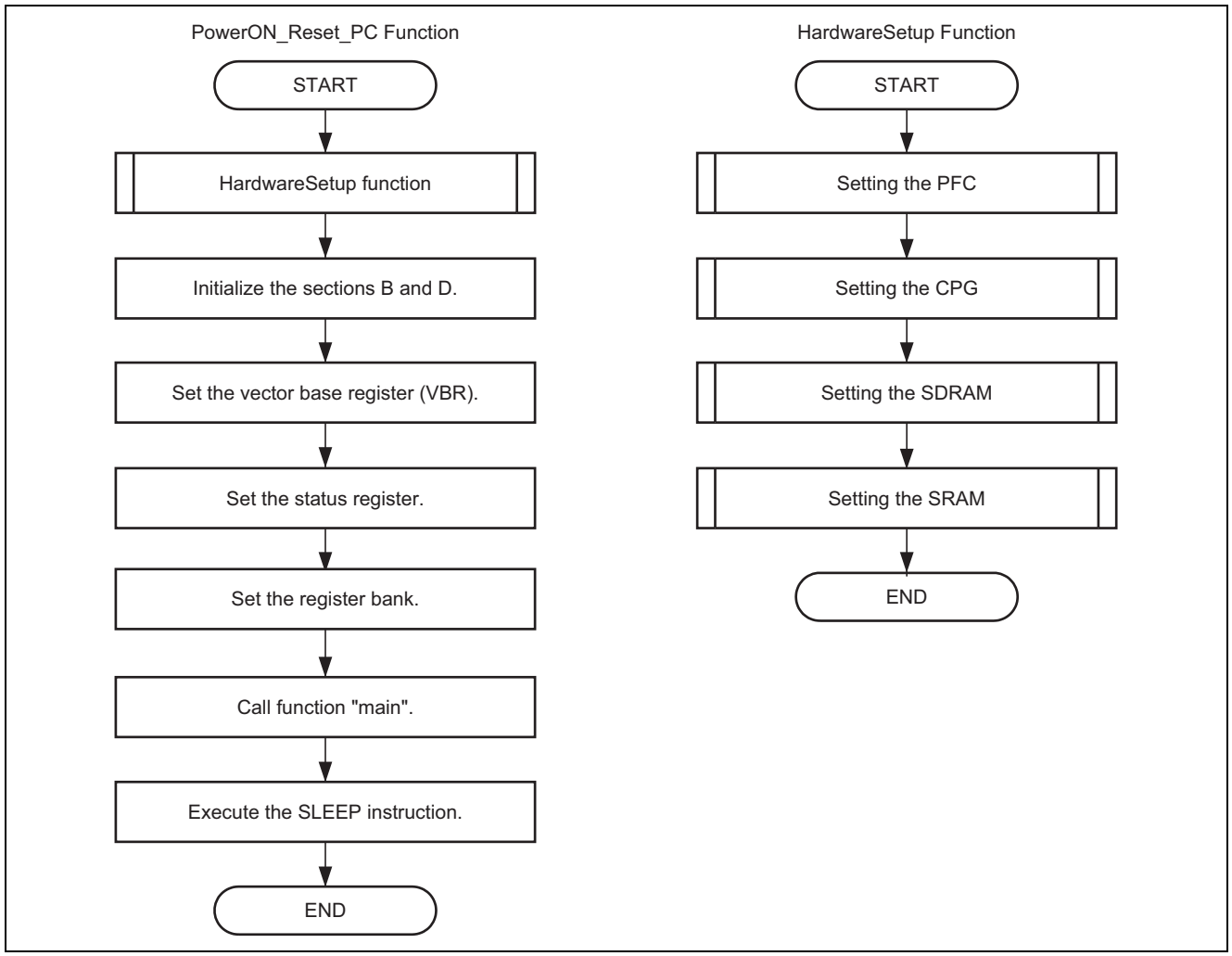

Figure 1 Flows of Processing by the PowerON_Reset_PC and HardwareSetup Functions

2.2 Description of Settings in the Sample Program

Table 1 is a list of the settings in the sample program.

Table 1 Settings in the Sample Program

Module	Description	
CPG	Input clock	: 10 MHz
	Internal clock	: 160 MHz
	Bus clock	: 40 MHz
	Peripheral clock	: 40 MHz
	MTU2S clock	: 80 MHz
	AD clock	: 40 MHz
INTC	Use of register banks is enabled for all interrupts except NMI and user break. (Settings of the bank control register (IBCR) are ignored.)	
BSC	CS3 space: SDRAM	
	Data bus width	16 bits
	Row address	12 bits
	Column address	9 bits
	CAS latency	2 cycles
	CS4 space: SRAM	
	Data bus width	16 bits
PFC	The address bus, data bus, and bus control pin functions for use in the CS3 and CS4 spaces are selected for multiplexed pins.	

2.3 Notes on Using the Sample Program

In this sample program, the bus state controller is initialized in HardwareSetup function. Only access sections B and D in external memory after initialization of the bus state controller.

3. Listing of Sample Program

1. Sample program listing: "resetprg.c" (1)

```
1       /*""FILE COMMENT""*****************************************************************
2       *
3       *       System Name : SH7211 Sample Program
4       *       File Name   : resetprg.c
5       *       Version     : 1.01.00
6       *       Contents    : SH7211 Initial Setting
7       *       Model       : M3A-HS11
8       *       CPU         : SH7211
9       *       Compiler    : SHC9.1.1.0
10      *       OS          : none
11      *
12      *       Note        :
13      *       <Caution>
14      *       This sample program is for reference
15      *       and its operation is not guaranteed.
16      *       Customers should use this sample program
17      *       for technical reference in software development.
18      *
19      *
20      *
21      *
22      *
23      *
24      *
25      *       Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
26      *       AND Renesas Solutions Corp. All Rights Reserved
27      *
28      *       History   : 2006.02.23 ver.1.00.00
29      *                 : 2008.04.07 ver.1.01.00
30      *""FILE COMMENT END""*************************************************************/
31      #include           <machine.h>
32      #include           <_h_c_lib.h>
33      #include           "stacksct.h"
34      #include           "iodefine.h"
35
36      #define SR_Init    0x000000F0
37      #define INT_OFFSET 0x10
38
39      extern unsigned int INT_Vectors;
40      void PowerON_Reset_PC(void);
41      void Manual_Reset_PC(void);
42      extern void main(void);
43      extern void HardwareSetup(void);
44
45      //extern void srand(unsigned int);    // Remove the comment when you use rand()
46      //extern char *_s1ptr;                // Remove the comment when you use strtok()
47
48      /*==== Section name changed to ResetPRG  ====*/
49      #pragma section ResetPRG
50
51      /*==== Entry function specified ====*/
52      #pragma entry PowerON_Reset_PC
53
```

2. Sample program listing: "resetprg.c" (2)

```
54      /*""FUNC COMMENT""*****************************************************************
55      * ID             :
56      * Module outline : CPU initialization function
57      *-----------------------------------------------------------------------------
58      * Include        : #include "iodefine.h"
59      *-----------------------------------------------------------------------------
60      * Declaration    : void PowerON_Reset_PC(void)
61      *-----------------------------------------------------------------------------
62      * Function       : This is the CPU initialization processing routine at the
63      *                : location registered in the power-on reset exception vector in
64      *                : the vector table.
65      *                : This function is executed immediately after a power-on reset.
66      *                :
67      *                :
68      *                :
69      *-----------------------------------------------------------------------------
70      * Argument       : None
71      *-----------------------------------------------------------------------------
72      * Return value   : None
73      *-----------------------------------------------------------------------------
74      * Note           : Processing that has been commented out should be restored as
75      *                : required.
76      *""FUNC COMMENT END""*************************************************************/
77      void PowerON_Reset_PC(void)
78      {
79
80          /*==== HardwareSetup function ====*/
81          HardwareSetup();              // Use Hardware Setup
82
83          /*==== Initializing sectionB,D ====*/
84          _INITSCT();
85
86          /*==== VBR setting ====*/
87          set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));
88
89      //  errno=0;                      // Remove the comment when you use errno
90      //  srand(1);                     // Remove the comment when you use rand()
91      //  _s1ptr=NULL;                  // Remove the comment when you use strtok()
92
93          /*==== Status register setting ====*/
94          set_cr(SR_Init);
95          nop();
96
97          /* ==== Bunk number register setting ==== */
98          INTC.IBNR.BIT.BE = 0x01;      /* Use the register bank for all interrupts */
99
100         /*==== main function call ====*/
101         main();
102
103         /*==== sleep instruction execute ====*/
104         sleep();
105     }
106
```

3. Sample program listing: "resetprg.c" (3)

```
107     //#pragma entry Manual_Reset_PC       // Remove the comment when you use Manual Reset
108     /*""FUNC COMMENT""*************************************************************
109     * ID             :
110     * Module outline : Manual reset processing
111     *-----------------------------------------------------------------------------
112     * Include        :
113     *-----------------------------------------------------------------------------
114     * Declaration    : void Manual_Reset_PC(void)
115     *-----------------------------------------------------------------------------
116     * Function       : This function is at the location registered in the manual
117     *                : reset exception vector in the vector table.
118     *                : No processing is defined in this reference program.
119     *                : Processing should be added as required.
120     *                :
121     *                :
122     *                :
123     *                :
124     *-----------------------------------------------------------------------------
125     * Argument       : None
126     *-----------------------------------------------------------------------------
127     * Return value   : None
128     *-----------------------------------------------------------------------------
129     * Note           : None
130     *""FUNC COMMENT END""*********************************************************/
131     void Manual_Reset_PC(void)
132     {
133                 /* NOP */
134     }
135     /* END of File */
```

4. Sample program listing: " hwsetup.c " (1)

```
1       /*""FILE COMMENT""*****************************************************************
2       *
3       *       System name : SH7211 Sample Program
4       *       File name   : hwsetup.c
5       *       Version     : 1.00.00
6       *       Contents    : Hardware initialization function
7       *       Model       : M3A-HS11
8       *       CPU         : SH7211
9       *       Compiler    : SHC9.1.1.0
10      *       OS          : None
11      *
12      *       Note        : <Caution>
13      *                     This sample program is for reference
14      *                     and its operation is not guaranteed.
15      *                     Customers should use this sample program
16      *                     for technical information in software
17      *                     development.
18      *
19      *
20      *
21      *
22      *
23      *
24      *       Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
25      *       AND Renesas Solutions Corp. All Rights Reserved
26      *
27      *       History   : 2008.04.07 ver.1.00.00
28      *""FILE COMMENT END""*************************************************************/
29      #include "iodefine.h"
30
31      /* ==== Prototype declaration ==== */
32      void  HardwareSetup(void);
33      //static void init_puram_section(void);
34      void  I_O_Init(void);
35
36      /* ==== Prototype declaration for external reference ==== */
37      extern void io_set_cpg(void);
38      //extern void io_init_sdram(void);
39
40
41
42
43      /*""FUNC COMMENT""*****************************************************************
44      * ID             :
45      * Module outline : Hardware initialization function
46      *---------------------------------------------------------------------------------
47      * Include        : #include "iodefine.h"
48      *---------------------------------------------------------------------------------
49      * Declaration    : void  HardwareSetup(void)
50      *---------------------------------------------------------------------------------
51      * Function       : Initializing the CPG and BSC
52      *---------------------------------------------------------------------------------
53      * Argument       : None
54      *---------------------------------------------------------------------------------
55      * Return value   : None
56      *---------------------------------------------------------------------------------
57      * Function       :
58      *---------------------------------------------------------------------------------
59      * Note           :
60      *""FUNC COMMENT END""*************************************************************/
```

5. Sample program listing: " hwsetup.c " (2)

```
61      void  HardwareSetup(void)
62      {
63          /*==== I/O setting ====*/
64          I_O_Init();
65
66          /*==== CPG setting ====*/
67          io_set_cpg();
68
69          /*==== SDRAM area setting ====*/
70          io_init_sdram();
71
72          /*==== SRAM area setting ====*/
73          io_init_sram();
74
75      }
76
77      void  I_O_Init(void){
78
79          /* ==== PFC settings ==== */
80
81          PB.DR.BIT.B10 =1u;         /* PB10 LED OFF */
82          PB.DR.BIT.B11 =1u;         /* PB11 LED OFF */
83          PB.DR.BIT.B12 =1u;         /* PB12 LED OFF */
84          PB.DR.BIT.B13 =1u;         /* PB13 LED OFF */
85          PB.DR.BIT.B20 =1u;         /* PB20 LED OFF */
86          PB.DR.BIT.B21 =1u;         /* PB21 LED OFF */
87
88          PFC.PACRH3.WORD = 0x0000;
89          PFC.PACRH2.WORD = 0x0000;
90          PFC.PACRH1.WORD = 0x0000;
91          PFC.PACRL4.WORD = 0x0000;
92          PFC.PACRL3.WORD = 0x0000;
93          PFC.PACRL2.WORD = 0x0000;
94          PFC.PACRL1.WORD = 0x0000;
95
96          PFC.PAIORH.WORD = 0x03FF;
97          PFC.PAIORL.WORD = 0xFFFF;
98
99          PFC.PBCRH4.WORD = 0x0000;
100         PFC.PBCRH3.WORD = 0x0000;
101         PFC.PBCRH2.WORD = 0x0000;
102         PFC.PBCRH1.WORD = 0x0000;
103         PFC.PBCRL4.WORD = 0x0000;
104         PFC.PBCRL3.WORD = 0x0000;
105         PFC.PBCRL2.WORD = 0x0000;
106         PFC.PBCRL1.WORD = 0x0000;
107
108         PFC.PBIORH.WORD = 0x0037;
109         PFC.PBIORL.WORD = 0x7FCF;
110
111         PFC.PDCRL4.WORD = 0x0000;
112         PFC.PDCRL3.WORD = 0x0000;
113         PFC.PDCRL2.WORD = 0x0000;
114         PFC.PDCRL1.WORD = 0x0000;
115
116         PFC.PDIOR.WORD = 0xFFFF;
117
118         PFC.PFCRL1.BIT.PF1MD = 0x0;
119         PFC.PFCRL1.BIT.PF0MD = 0x0;
120     }
121
122     /* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manuals
  SH7211 Group Hardware Manual (REJ09B0344)
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