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SH7206 Group

Example of BSC SDRAM Interface Setting (32-Bit Bus)

Introduction

This document describes the synchronous DRAM (SDRAM) interface of the bus state controller (BSC) and provides a practical example of SDRAM connection.

Target Device

SH7206

Contents

1. Overview

1.1 Specifications

- Two pieces of 128-Mbit (2 Mwords x 16 bits x 4 banks) SDRAM are used and are connected to the SH7206 with a data bus width of 32 bits.
- The SDRAM interface function of SH7206 is used to initialize SDRAM.

1.2 Function Used

Bus state controller (BSC)

1.3 Applied Conditions

- MCU: SH7206 (R5S72060)
- Operating frequency: Internal clock at 200 MHz
  Bus clock at 66.67 MHz
  Peripheral clock at 33.33 MHz
- C compiler: Manufactured by Renesas Technology Corp.
  Version 9.00 C/C++ compiler package for the SuperH RISC engine Family
- Compile option: Default settings of High-performance Embedded Workshop (-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Note

Operation of the sample program in this application note has been confirmed with the setting conditions given in the application note on *Example of SH7206 Initial Configuration*. Please refer to that document when setting up this sample task.

2. Description of Application Examples

2.1 Functions Used: Overview of Operation

SDRAM units that are connectable to this LSI are products that have 11, 12, 13 bits of row address, 8, 9, or 10 bits of column address, 4 or fewer banks, and in which the A10 pin is used to set pre-charge mode in read and write command cycles. Burst read/single write (burst length 1) and burst read/burst write (burst length 1) are supported as SDRAM operating modes.
Table 1 shows the specifications of the SDRAM unit used in this sample task.

Table 1 Specifications of SDRAM Used in This Application Task

Item	SDRAM Specification
Configuration	4 banks x 2,097,152 words x 16 bits
Capacity	128 Mbits x 2
CAS latency	2/3 (programmable)
Refresh cycle	4096 refresh cycles per 64 ms
Burst length	1/2/4/8 full pages (programmable)
Row address	A11 to A0
Column address	A8 to A0
Pre-charge	Auto pre-charge/all bank pre-charge controlled via A10

Figure 1 shows the memory map. SDRAM can be connected to the CS2 and CS3 spaces of SH7206. In this sample task, SDRAM is connected to the CS3 space.

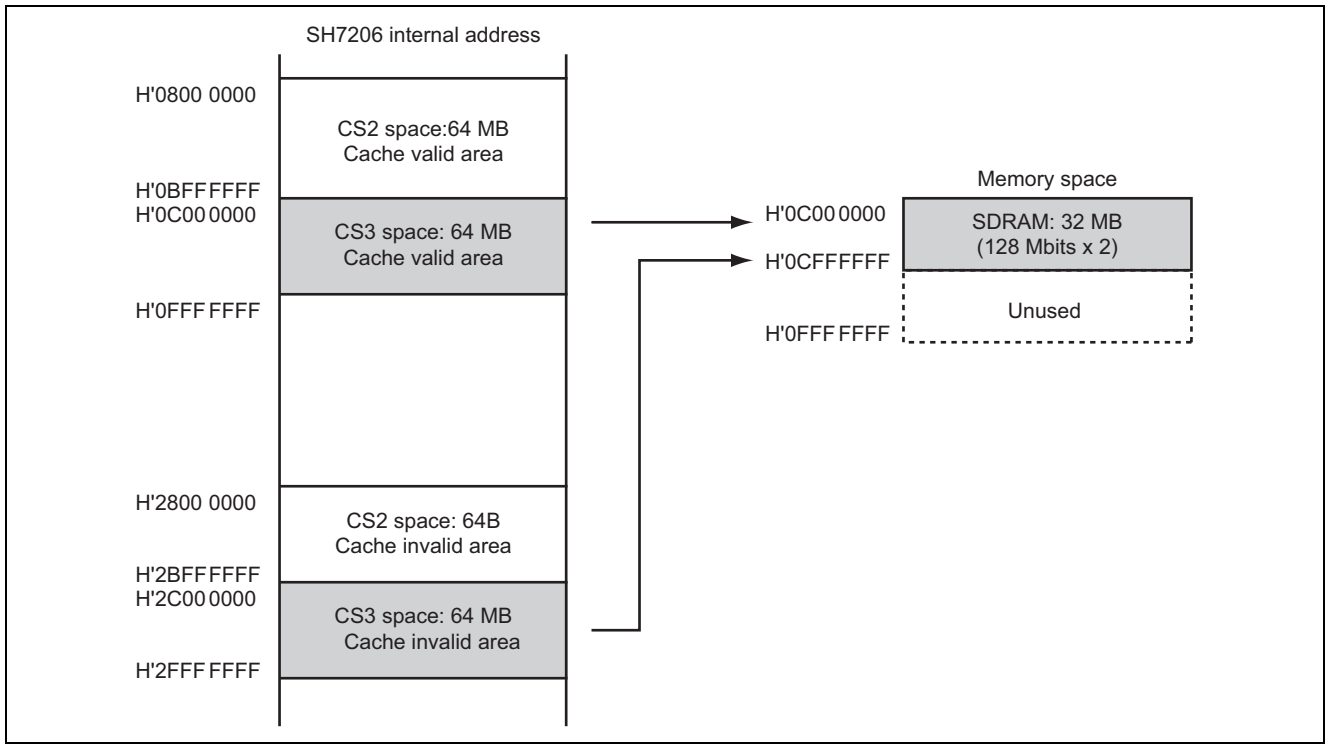

Figure 1 Memory Map

Figure 2 shows an example of an SDRAM connection circuit.

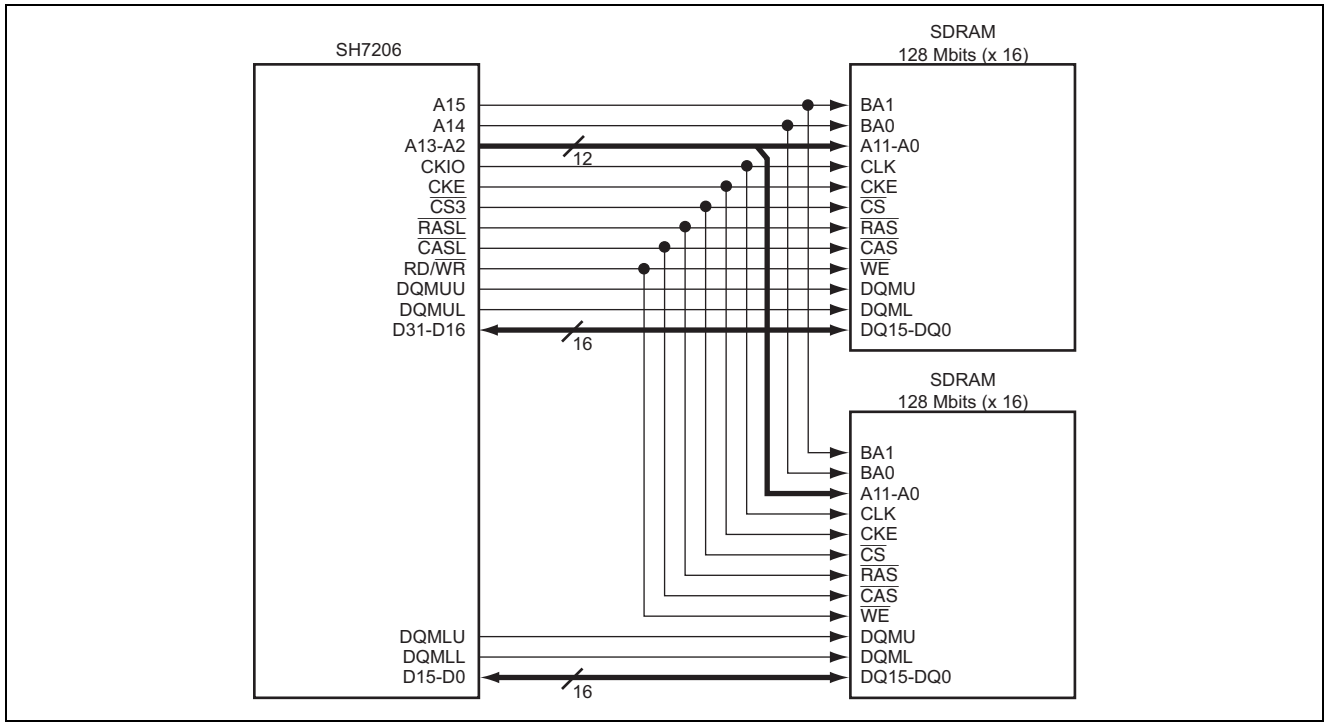

Figure 2 Example of SDRAM Connection Circuit (128-Mbit product x 2 and 32-bit bus)

Table 2 shows address-multiplexed output pins.

Table 2 Address Multiplexed Output

SH7206 Pin	Row Address	Column Address	SDRAM Pin	Function
A15	A24*2	A24*2	A13 (BA1)	Specifies the bank
A14	A23*2	A23*2	A12 (BA0)	Specifies the bank
A13	A22	A13	A11	Address
A12	A21	L/H*1	A10/AP	Specifies address/pre-charge
A11	A20	A11	A9	Address
A10	A19	A10	A8	Address
A9	A18	A9	A7	Address
A8	A17	A8	A6	Address
A7	A16	A7	A5	Address
A6	A15	A6	A4	Address
A5	A14	A5	A3	Address
A4	A13	A4	A2	Address
A3	A12	A3	A1	Address
A2	A11	A2	A0	Address

Notes: *1. The L/H bit is used in specifying commands for the SDRAM; and it is fixed low or high according to the access mode.
*2. Bank address specification

2.2 Procedure for Setting up the Functions

2.2.1 Example of the initialization Procedure for SDRAM

Figure 3 describes an example of initialization procedure to place SDRAM in the CS3 space.

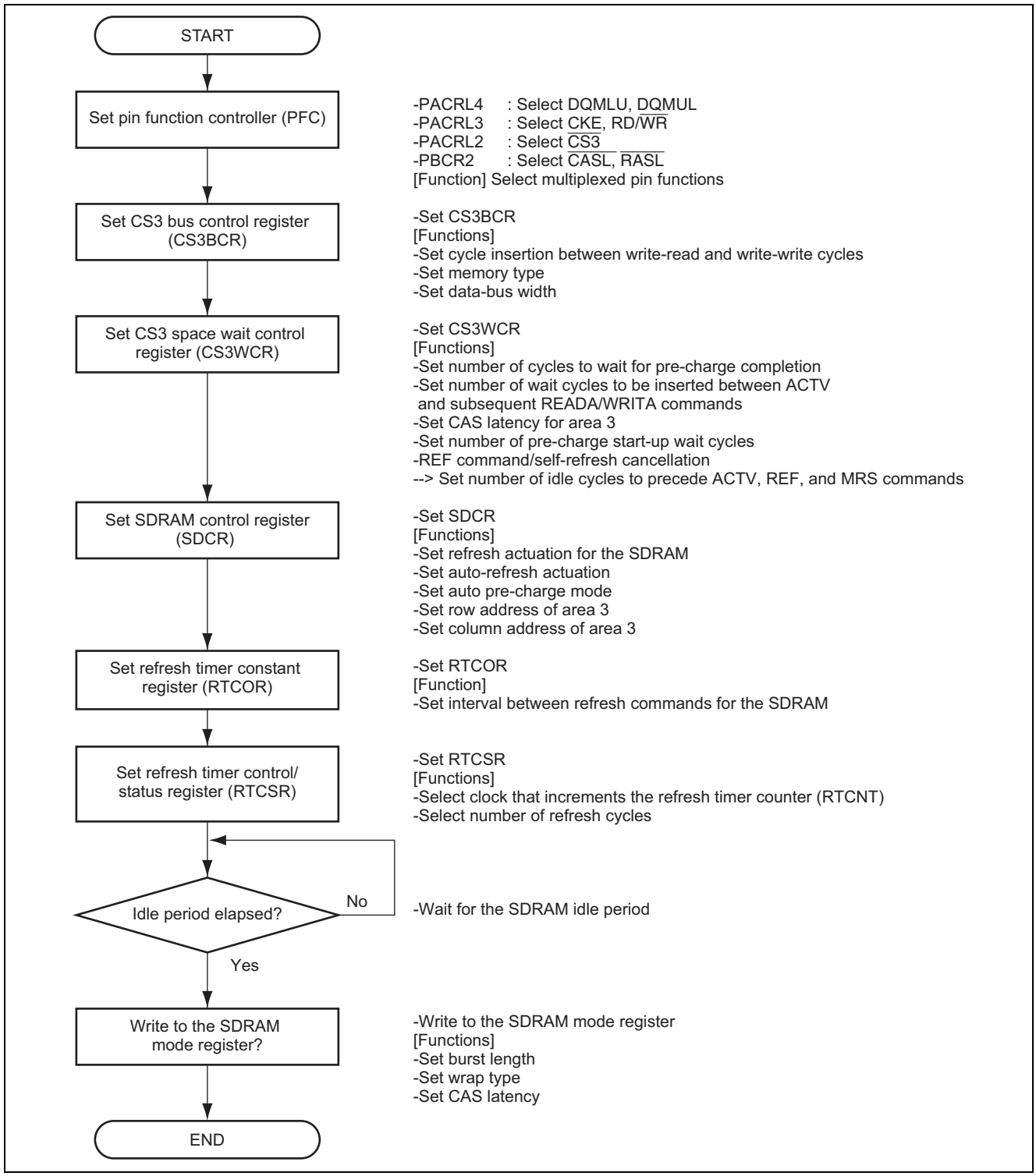

Figure 3 Example of the Procedure for Initial Settings to Place SDRAM in the CS3 Space

2.2.2 Example of Switching Procedure for AC Characteristics

To connect SDRAM to the SH7206 and use the SDRAM in clock mode 2, the AC characteristics must be switched. To use the AC characteristics switching function, set the AC characteristics switching register (ACSWR) and AC characteristics switching key register (ACKEYR).

Figure 4 gives an example of the procedure for setting the AC characteristics switching register (ACSWR). These settings must be executed from the internal RAM.

When the SH7206 is used in clock mode 7, leave the initial state as it is and do not make any particular initial settings.

Also, please refer to the SH7206 application note giving an example of initialization, which covers the switching of AC characteristics.

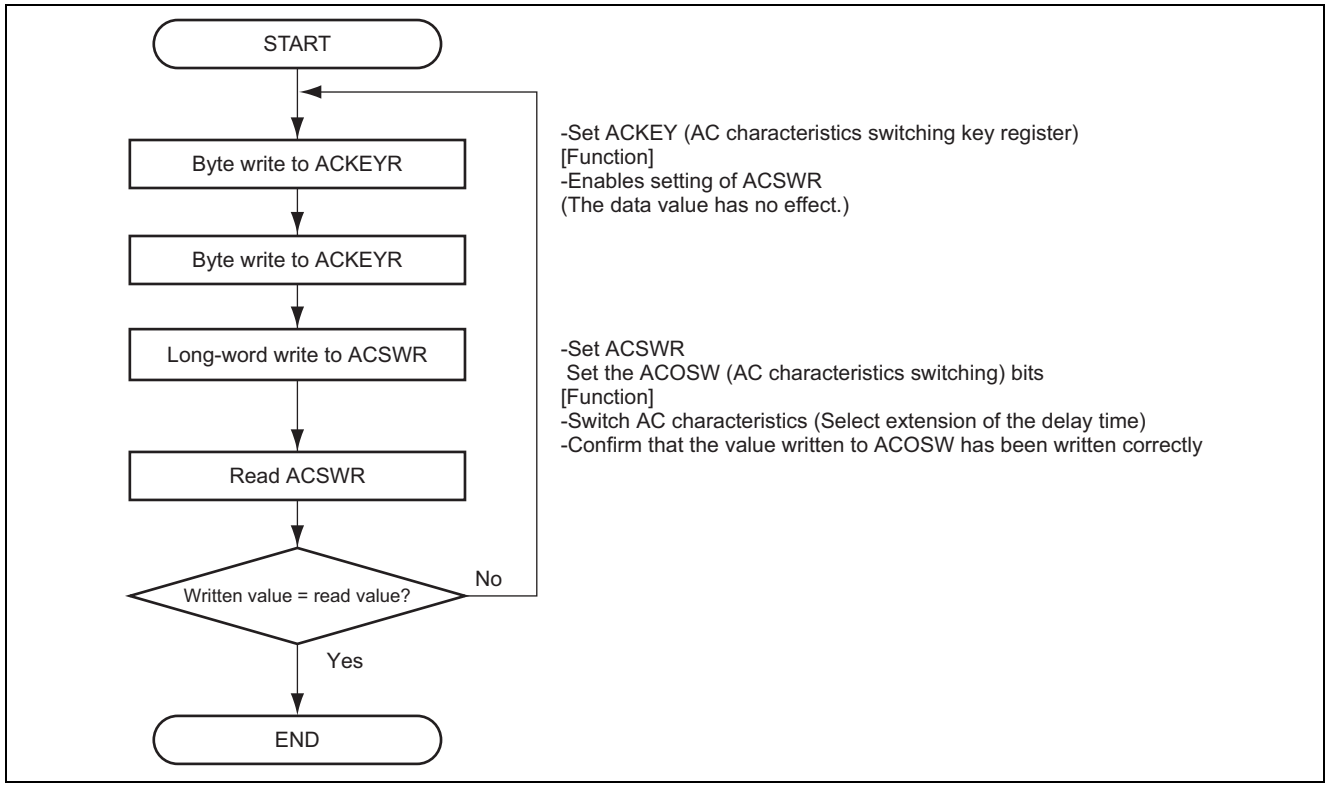

Figure 4 Example Procedure for Making Settings with the AC-Characteristics Switching Function

2.2.3 Power-On Sequence

To perform SDRAM initialization, the bus state controller registers must first be set, followed by a write to the SDRAM mode register.

Once power has been supplied, SDRAM needs a constant idle period. An idle period of at least 200 µs is set up by the software in this sample task. The required idle period differs with the SDRAM specification. Please refer to the manual for the SDRAM you are using. To write to the SDRAM mode register, a mode-register setting (MRS) command is issued. This takes the form of a special combination of the $\overline{CS3}$, $\overline{RASL}$, $\overline{CASL}$, and RD/$\overline{WR}$ signals. The address provides the data for input the SDRAM. Table 3 shows the address to be accessed in writing to the SDRAM mode register when the SDRAM is allocated to the CS3 space.

Table 3 Addresses to be Accessed as Values Written to the SDRAM Mode Register (CS3 Space)

Data Bus Width	CAS Latency	Burst Read/Single Write (Burst Length 1)		Burst Read/Burst Write (Burst Length 1)	
		Access Address	External Address Pin	Access Address	External Address Pin
16 bits	2	H'FFFC 5440	H'0000 0440	H'FFFC 5040	H'0000 0040
	3	H'FFFC 5460	H'0000 0460	H'FFFC 5060	H'0000 0060
32 bits	2	H'FFFC 5880	H'0000 0880	H'FFFC 5080	H'0000 0080
	3	H'FFFC 58C0	H'0000 08C0	H'FFFC 50C0	H'0000 00C0

In this sample task, the following settings are made in the SDRAM mode register.

- Burst length: burst read/single write (burst length 1)
- Wrap type: sequential
- CAS latency: 2 cycles

As shown in table 3, these settings are written to the SDRAM mode register by writing a word of any value to H'FFFC 5880 (the data is ignored.). In detail, the following commands are issued sequentially to the SDRAM.

— All bank pre-charge command (PALL)
  Idle cycles as specified by the WTRP1[1:0] bits in CS3WCR are inserted between the PALL and the first REF (shown below as idle period Tpw).
— Auto-refresh command (REF, eight times)
  Idle cycles as specified by the WTRC[1:0] bits in CS3WCR are inserted after the REF command is issued (shown below as idle period Trc).
— Mode-register setting command (MRS)

Figure 5 shows an example of timing in writing to the SDRAM mode register.

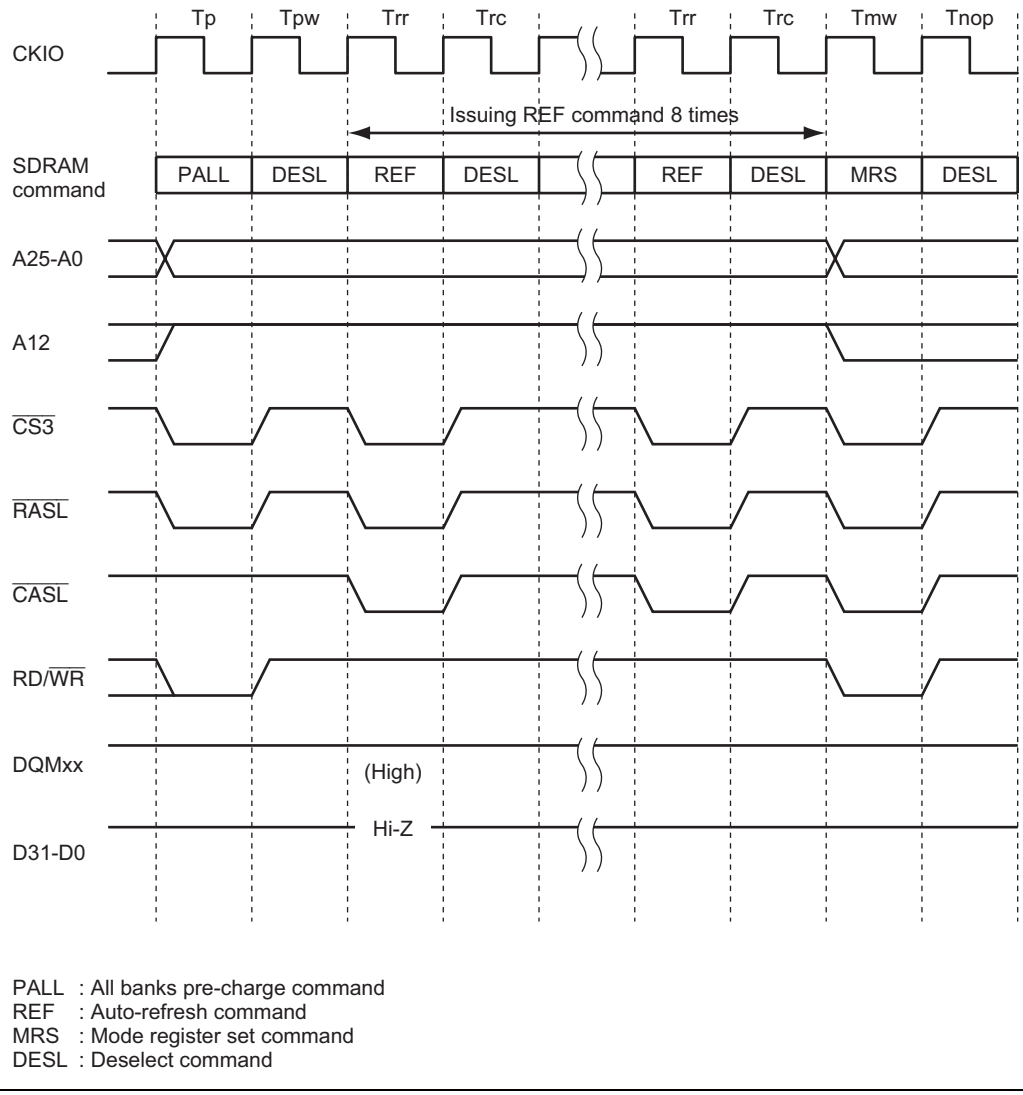

Figure 5 Example of Timing in Writing to the SDRAM Mode Register

2.3 Operation of the Sample Program

SDRAM read and write operations for sample program are described as follows:

1. Read operation

   Figure 6 shows an example of SDRAM single-read timing in operation with the bus clock running at 66.67 MHz. The operations below are performed on successive cycles of the SH7206.

   — Tr: Issuance of ACTV (activating row and bank) command

   — Trw1, Trw2: Wait cycles between the ACTV command and READA/WRITA commands
   The number of wait cycles set by the WTRCD[1:0] bits in CS3WCR is inserted here.

   — Tcl: Issuance of READA command

   — Tcw: Wait cycles between the Tc1 and Td1 cycles
   The number of wait cycles should be equivalent to the CAS latency of the SDRAM. The number of wait cycles set by the A3CL[1:0] bits in CS3WCR (CAS latency of Area 3) is inserted here.

   — Td1: Reading of data to be read

   — Tde: Idle cycle necessary for transferring the read data within this LSI
   One cycle must be allowed without fail for both burst-read and single-read operations.

   — Tap1, Tap2: Cycles of waiting for completion of auto pre-charge
   The number of wait cycles set by the WTRP[1:0] bits in CS3WCR is inserted here.

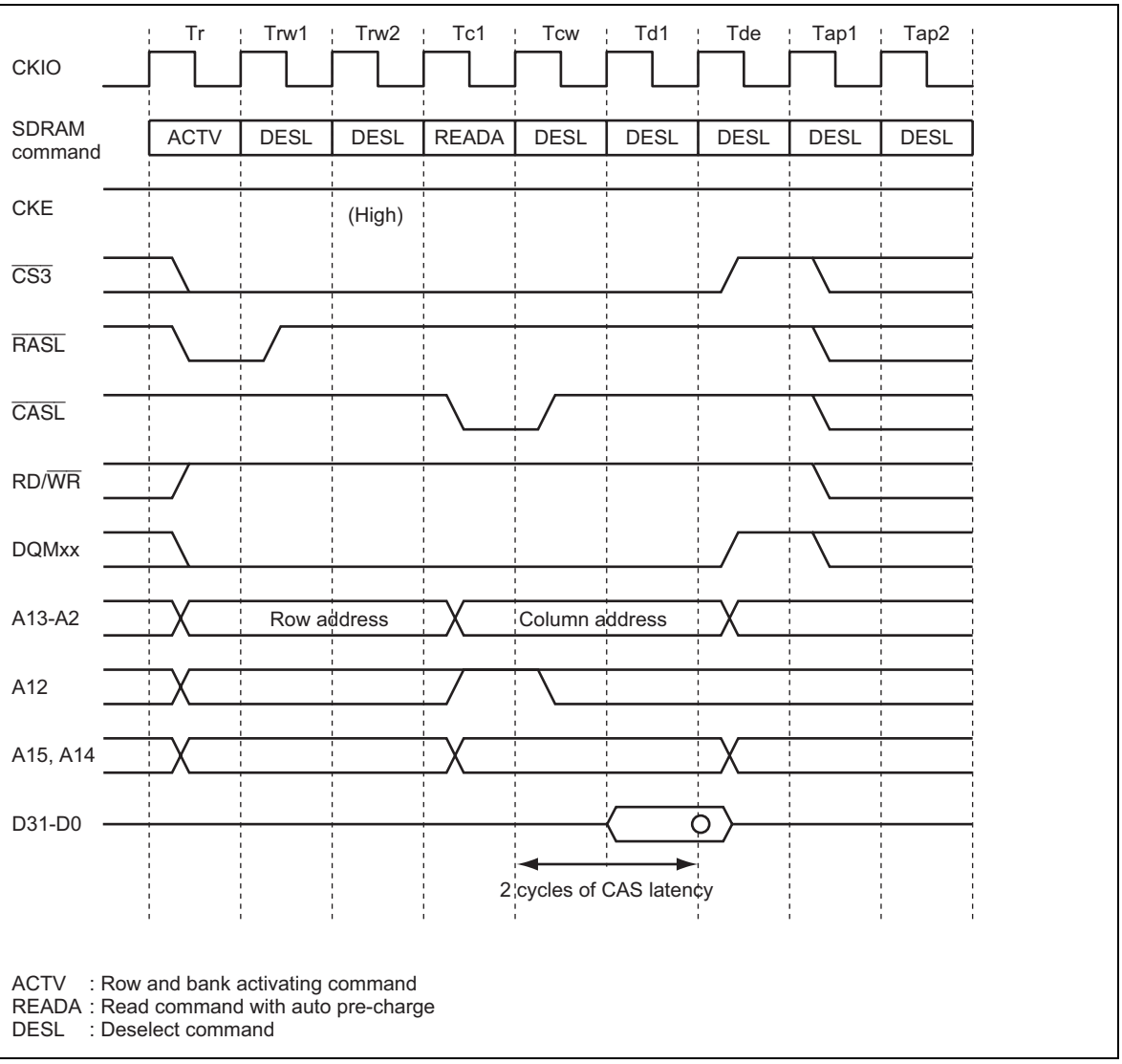

Figure 6 Example of SDRAM Single-Read Timing (with the Bus-Clock Operating at 66.67 MHz)

2. Write operation

Figure 7 shows an example of SDRAM single-write timing in operation with the bus clock running at 66.67 MHz. The operations below are performed on successive cycles of the SH7206.

— Tr: Issuance of the ACTV (activating row and bank) command
— Trw1, Trw2: Wait cycles between the ACTV command and READA/WRITA commands
The number of wait cycles set by the WTRCD[1:0] bits in CS3WCR is inserted here.
— Tcl: Issuance of WRITA command
— Trwl1, Trwl2: Cycles of waiting for the start-up of auto pre-charge
The number of wait cycles set by the TRWL[1:0] bits in CS3WCR is inserted here.
— Tap1, Tap2: Cycles of waiting for completion of auto pre-charge
The number of wait cycles set by the WTRP[1:0] bits in CS3WCR is inserted here.

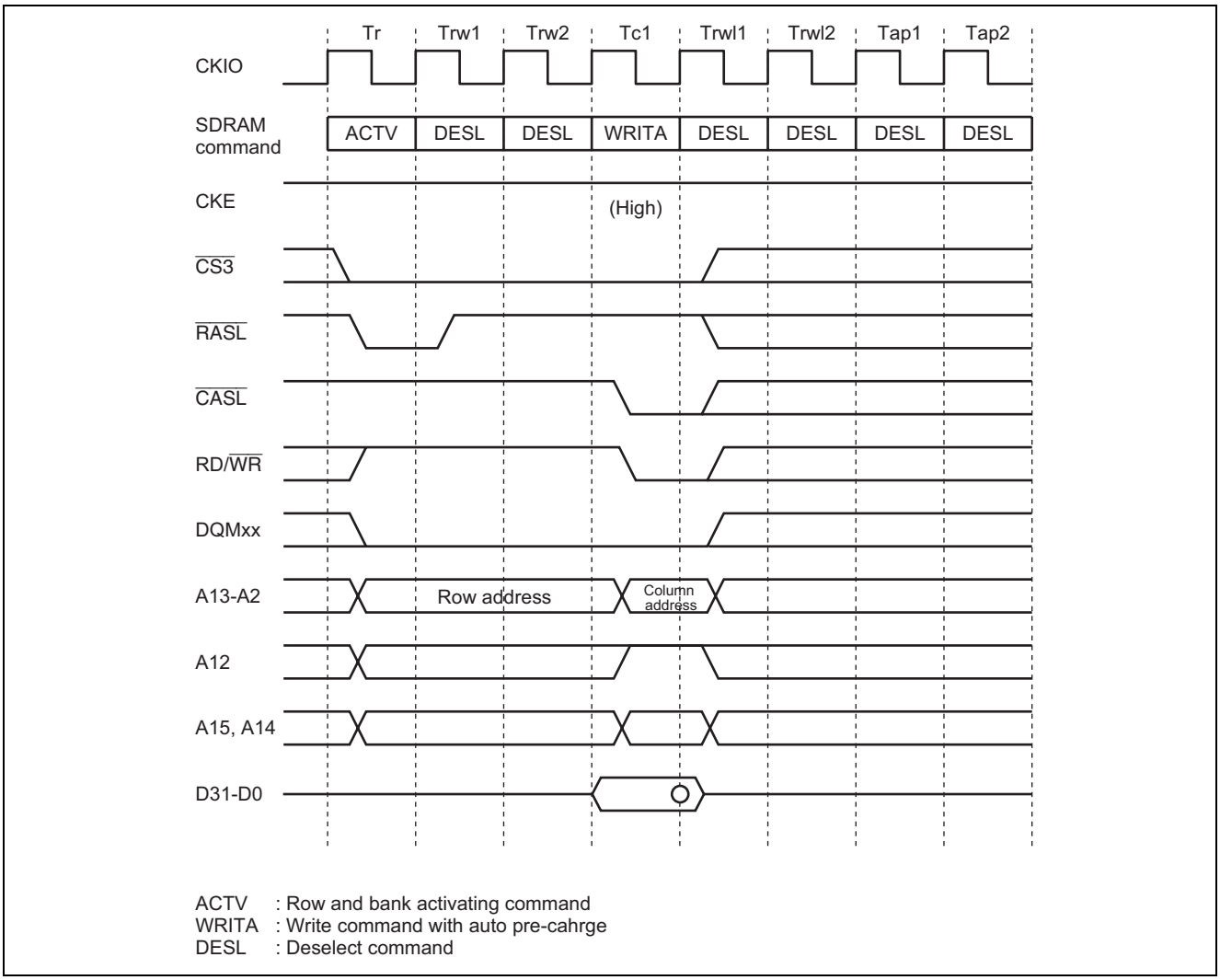

Figure 7 Example of SDRAM Single-Write Timing (with the Bus-Clock Operating at 66.67 MHz)

2.4 Example of Bus State Controller Setting

An example of bus state controller settings for bus-clock operation at 66.67 MHz is given in table 4. Please refer to the section on the bus state controller in the SH7206 Group hardware manual for details on the individual registers.

Table 4 Example of Bus State Controller Settings

Name of Register	Address	Setting Value	Function
CS3 space bus control register (CS3BCR)	H'FFFC 0010	H'1000 4600	-IWW[2:0] = B'001 Idle period between writing and reading and between writing and writing: 1 cycle -TYPE[2:0] = B'100: SDRAM -BSZ[1:0] = B'10: 32-bit data bus width
CS3 space wait control register (CS3WCR)	H'FFFC 0034	H'0000 4892	-WTRP[1:0] = B'10 Number of cycles to wait for pre-charge completion: 2 -WTRCD[1:0] = B'10 ACTV command → Number of wait cycles between READA/WRITA commands: 2 -A3CL[1:0] = B'01 CAS latency of Area 3: 2 cycles -TRWL[1:0] = B'10 Number of cycles to wait for pre-charge start-up: 2 -WTRC[1:0] = B'10 REF command/self-refresh cancellation → Number of idle cycles among ACTV/REF/MRS commands: 5
SDRAM control register (SDCR)	H'FFFC 004C	H'0000 0809	-RFSH = 1: Refresh -RMODE = 0: Auto-refresh -BACTV = 0: Auto pre-charge mode -A3ROW[1:0] = B'01 Row address of Area 3: 12 bits -A3COL[1:0] = B'01 Column address of Area 3: 9 bits

Name of Register	Address	Setting Value	Function
Refresh timer control register/status register (RTCSR)	H'FFFC 0050	H'A55A 0010*	-1 cycle = 1/(Bϕ (66 MHz)/16) ≈ 240 ns -Interval between SDRAM-refresh requests: 4096 cycles/64 ms = 15.625 µs/time -Setting value of RTCOR = 15.625 µs ÷ 240 ns ≈ 65 = H'41
Refresh timer constant register (RTCOR)	H'FFFC 0058	H'A55A 0041*	-1 cycle = 1/(Bϕ (66 MHz)/16) ≈ 240 ns -Interval between SDRAM-refresh requests: 4096 cycles/64 ms = 15.625 µs/time -Setting value of RTCOR = 15.625 µs ÷ 240 ns ≈ 65 = H'41
AC characteristics switching register (ACSWR)	H'FFFC 180C	H'0000 0009	-AC0SW[3:0] = B'1001 Switches the AC characteristics to extend the delay time.
AC characteristics switching key register (ACKEYR)	H'FFFC 1BFC	H'0000 0000	-Write operation for AC characteristics switching (written value is ignored.)

Note: * When writing, set the upper 16 bits of write data to H'A55A and cancel the write protection.

3. Sample Program

- Sample Program: Listing of “bscsdram.c” (1)

```
1   /*""FILE COMMENT""*****************************************************************
2   *
3   *       System Name : SH7206 Sample Program
4   *       File Name   : bscsdram.c
5   *       Version     : 1.00.00
6   *       Contents    : SH7206 initial setting
7   *       Model       : M3A-HS60
8   *       CPU         : SH7206
9   *       Compiler    : SHC9.0.00
10  *       OS          : None
11  *
12  *       Note        :
13  *                     <Caution>
14  *                     This entire sample program is for reference only and
15  *                     its operation is not guaranteed.
16  *                     Please use this sample as a technical reference
17  *                     in software development.
18  *
19  *       Copyright (C) 2004 Renesas Technology Corp. All Rights Reserved
20  *       AND Renesas Solutions Corp. All Rights Reserved
21  *
22  *       History   : 2004.10.14 ver.1.00.00
23  *""FILE COMMENT END""*************************************************************/
24  #include "iodefine.h"
25
26  /* ==== Macro definition ==== */
27
28  /* Access address for writing to the SDRAM mode register */
29  #define  SDRAM_MODE      (*(volatile unsigned short *)(0xfffc5880))
30
31  /* ==== Prototype declaration ==== */
32  void io_init_sdram(void);
33
34  /*""FUNC COMMENT""*****************************************************************
35  * ID                  :
36  * Overview of module : SDRAM 32-bit bus width connection setting
37  *-------------------------------------------------------------------------------
38  * Include             : #include "iodefine.h"
39  *-------------------------------------------------------------------------------
40  * Declaration         : void io_init_sdram(void)
41  *-------------------------------------------------------------------------------
```

- Sample Program: Listing of “bscsdram.c” (2)

```
42  * Function          : Sets pin function controller (PFC) and bus state
43  *                   : controller (BSC) to enable SDRAM in the CS3 space
44  *                   :
45  *-----------------------------------------------------------------------
46  * Argument          : None
47  *-----------------------------------------------------------------------
48  * Return value      : None
49  *-----------------------------------------------------------------------
50  * Caution           : PFC settings are applied to the individual bits to avoid
51  *                   : changes to PFC settings made in other processing.
52  *""FUNC COMMENT END""***************************************************/
53  void io_init_sdram(void)
54  {
55       volatile int j = 40000;         /* 200-µs wait count @ 200 MHz */
56
57    /* ==== PFC setting ==== */
58       PORT.PACRH2.BIT.PA23MD = 0x1;   /* Output DQMUU  */
59       PORT.PACRH2.BIT.PA22MD = 0x1;   /* Output DQMUL  */
60       PORT.PACRL4.BIT.PA13MD = 0x1;   /* Output DQMLU  */
61       PORT.PACRL4.BIT.PA12MD = 0x1;   /* Output DQMLL  */
62       PORT.PACRL3.BIT.PA9MD = 0x5;    /* Output CKE    */
63       PORT.PACRL3.BIT.PA8MD = 0x5;    /* Output RD/WR# */
64       PORT.PACRL2.BIT.PA7MD = 0x2;    /* Output CS3    */
65       PORT.PBCR2.BIT.PB5MD = 0x4;     /* Output CASL   */
66       PORT.PBCR2.BIT.PB4MD = 0x4;     /* Output RASL   */
67
68       PORT.PDCRH4.WORD = 0x1111;      /* Input/output D31-D28 */
69       PORT.PDCRH3.WORD = 0x1111;      /* Input/output D27-D24 */
70       PORT.PDCRH2.WORD = 0x1111;      /* Input/output D23-D20 */
71       PORT.PDCRH1.WORD = 0x1111;      /* Input/output D19-D16 */
72
73       /* ==== CS3 space bus control register (CS3BCR) setting ==== */
74       BSC.CS3BCR.LONG = 0x10004600ul; /*
75                               * Between write & read/between write & write cycles
76                               * Idle specification : inserts 1 idle cycle
77                               * Memory type        : SDRAM
78                               * Data-bus spec.     : 32-bit width
79                                     */
80       /* ==== CS3 space wait control register (CS3WCR) setting ==== */
81       BSC.UN2_BSC.SDRAM.REG_CS3WCR.LONG = 0x00004892ul;
82                                        /*
83                                      * Number of pre-charge cycles: 2
84                                      * Number of wait cycles from ACT command to
85                                      * read commands             :2
86                                      * CAS latency for Area 3    :2
87                                      * Pre-charge start-up cycles:2
88                                      * Idle cycles from REF command to ACT/REF/
89                                      * MRS commands              :5
90                                      */
```

- Sample Program: Listing of “main.c” (3)

```
91          /* ==== SDRAM control register (SDCR) setting ==== */
92          BSC.SDCR.LONG = 0x00000809ul;   /*
93                                          * Refresh control 1        : Refresh
94                                          * Refresh control 2        : Auto-refresh
95                                          * Bank active mode         : Auto pre-
96                                          *                           charge mode
97                                          * Area 3 row address bits  : 12
98                                          * Area 3 column address bit: 9
99                                             */
100         /* ==== Refresh timer constant register (RTCOR) setting ==== */
101         BSC.RTCOR.LONG = 0xa55a0041ul;  /*
102                                         * 15.625 µs/240 ns = 64(0x41) cycles/time
103                                         */
104         /* ==== Refresh timer control/status register (RTCSR) setting ==== */
105         BSC.RTCSR.LONG = 0xa55a0010ul;  /*
106                                         * Start initialization sequence
107                                         * -clock select: Bϕ16: 1 cycle = 240 ns
108                                         * -times consecutively refreshed: 1
109                                         */
110         /* ==== Idle period passed? ==== */
111         while(j-- > 0){
112            /* Wait */
113         }
114
115         /* ==== Write to SDRAM mode register ==== */
116         SDRAM_MODE = 0;                    /*
117                                         * Write data is arbitrary.
118                                         * SDRAM mode register setting in CS3 space
119                                         * Burst read (burst length 1)/single write
120                                         */
121     }
122     /* End of File */
```

4. Documents for Reference

- Software manual
  SH-2A SH2A-FPU Software Manual Rev.3.00
  If you don't already have it, please download the latest version from the homepage of Renesas Technology Corp.

- Hardware manual
  SH7206 Group Hardware Manual Rev.1.00
  If you don't already have it, please download the latest version from the homepage of Renesas Technology Corp.

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1.00	Sep.05.05	—	First edition issued

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