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SH7263/SH7203 Groups

Example of BSC SDRAM Interface Connection (16-Bit Data Bus)

Introduction

This application note describes the synchronous DRAM (SDRAM) interface of the bus state controller (BSC) and provides a practical example of connection with a data-bus width of 16 bits.

Target Devices

SH7263/SH7203

Contents

1. Preface

1.1 Specification

- A 64-, 128-, 256-, or 512-Mbit SDRAM (4 banks and 16-bit data bus) is connected to the SH7263 or SH7203 with a 16-bit data-bus width.

1.2 Module Used

- Bus state controller (BSC)

1.3 Applicable Conditions

- Microcontroller: SH7263/SH7203 (R5S72630/R5S72030) Groups
- SDRAM:

64-Mbit product	EDS6416AJTA (4 banks × 1 Mwords × 16 bits) from Elpida Memory, Inc.
128-Mbit product	EDS1216AGTA (4 banks × 2 Mwords × 16 bits) from Elpida Memory, Inc.
256-Mbit product	EDS2516ADTA (4 banks × 4 Mwords × 16 bits) from Elpida Memory, Inc.
512-Mbit product	K4S511632D (4 banks × 8 Mwords × 16 bits) from Samsung Japan Corporation

- Operating frequencies:

Internal clock	200 MHz
Bus clock	66.67 MHz

1.4 Related Application Notes

The operation of the reference program for this document was confirmed with the setting conditions described in the *SH7263/SH7203 Group Hardware Manual*. Please refer to the hardware manual with this application note.

2. Description of Sample Application

2.1 Operational Overview of Module Used

The bus state controller (BSC) of the SH7263/SH7203 supports an SDRAM interface that is directly connectable to SDRAM units that have 11, 12, or 13 bits of row address, 8, 9, or 10 bits of column address, 4 or fewer banks, and in which the A10 pin is used to set pre-charge mode in read and write command cycles. Burst reading/single writing (burst length 1) and burst reading/burst writing (burst length 1) are supported as SDRAM operating modes.

Table 1 provides the specifications of SDRAM for the SH7263/SH7203 and table 2 gives a list of capacities of 16-bit data bus products corresponding to the combinations of row- and column-address bits that are suitable for the SDRAM specifications of the SH7263/SH7203.

Table 1 Specifications of SDRAM for the SH7263/SH7203

Item	Description
Configuration	2 or 4 banks
Capacity	16, 64, 128, 256, or 512 Mbits
Data-bus width	16 or 32 bits
CAS latency	2 or 3 (programmable)
Refresh cycles	4096 or 8192 refresh cycles (max.) per 64 ms
Burst length	1, 2, 4, or 8 full pages (programmable)
Pre-charge	Auto pre-charge/all bank pre-charge controlled via A10

Table 2 Capacity by Address Configuration of SDRAM for the SH7263/SH7203 (16-Bit Data Bus)

		Column address		
		8 bits	9 bits	10 bits
Row address	11 bits	16-Mbit SDRAM	—	—
	12 bits	64-Mbit SDRAM	128-Mbit SDRAM	256-Mbit SDRAM*
	13 bits	—	256-Mbit SDRAM*	512-Mbit SDRAM

Note *: For 256-Mbits SDRAM products, 9-bit and 10-bit column addresses are usable.

Figure 1 shows a memory map.

SDRAM can be connected to the CS2 and CS3 spaces of the SH7263/SH7203. In cases where the SDRAM is only connected in one area, make the SDRAM-connection settings for area 3.

In this sample program, the SDRAM is connected in the CS3 space.

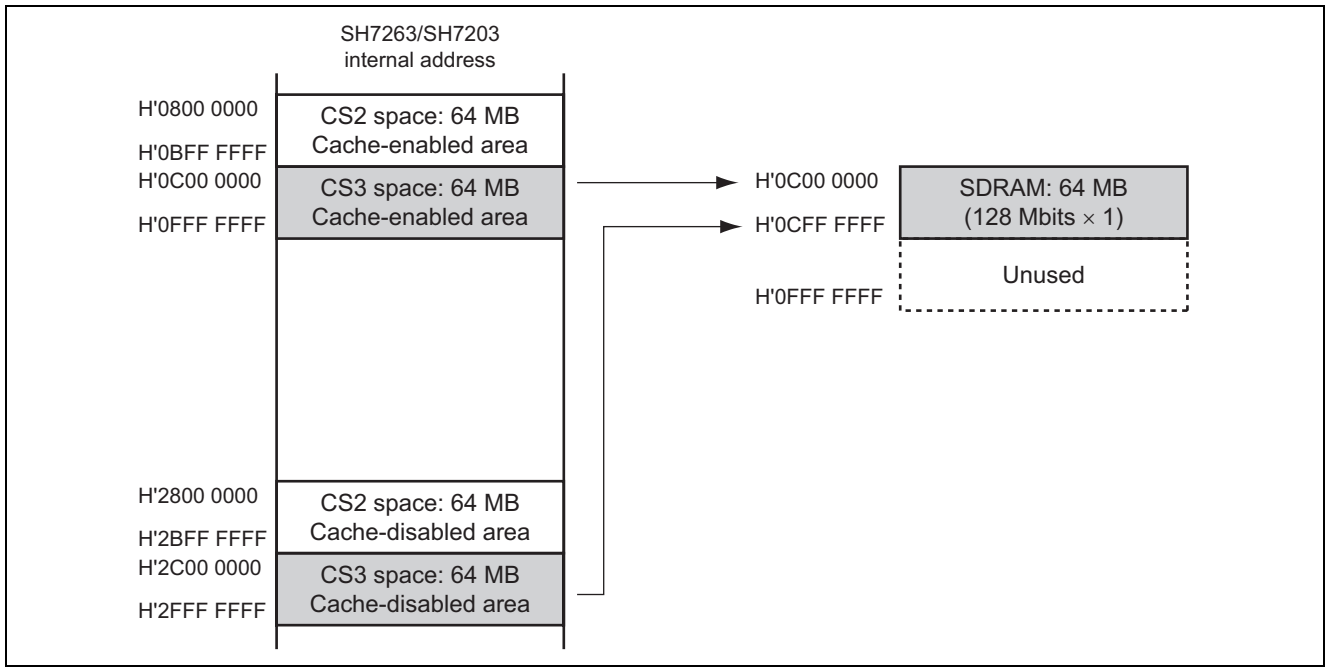


Figure 1 Memory Map (128-Mbit SDRAM × 1)

2.2 Description of Connection Example

This section describes how to connect SDRAM with capacities from 64- to 512-Mbits. In detail, connection methods are divided into groups according to the row-address specification of the SDRAM to be connected. For a 16-bit data bus, two types of product: ① those with 12 bits of row address (A0 to A11) and ② those with 13 bits of row address (A0 to A12) are connectable. The SH7263/SH7203 has $\overline{\text{RASL}}$/$\overline{\text{CASL}}$ and $\overline{\text{RASU}}$/$\overline{\text{CASU}}$ pins, enabling the separate control of two SDRAM units. The example of connection is with a single SDRAM unit.

Note: Relation between address space and levels on the $\overline{\text{RASL}}$/$\overline{\text{CASL}}$ and $\overline{\text{RASU}}$/$\overline{\text{CASU}}$ pins
The L/H bit of internal address A25 for the SH7263/SH7203 is used to switch the $\overline{\text{RASL}}$/$\overline{\text{CASL}}$ and $\overline{\text{RASU}}$/$\overline{\text{CASU}}$ pins. A single 512-Mbit SDRAM unit can be connected to an address range of up to 512 Mbits (64 Mbytes) in either the CS2 or the CS3 space. Figure 2 shows memory mapping in the CS3 space when SDRAM units with capacities from 64 to 512 Mbits are in use.

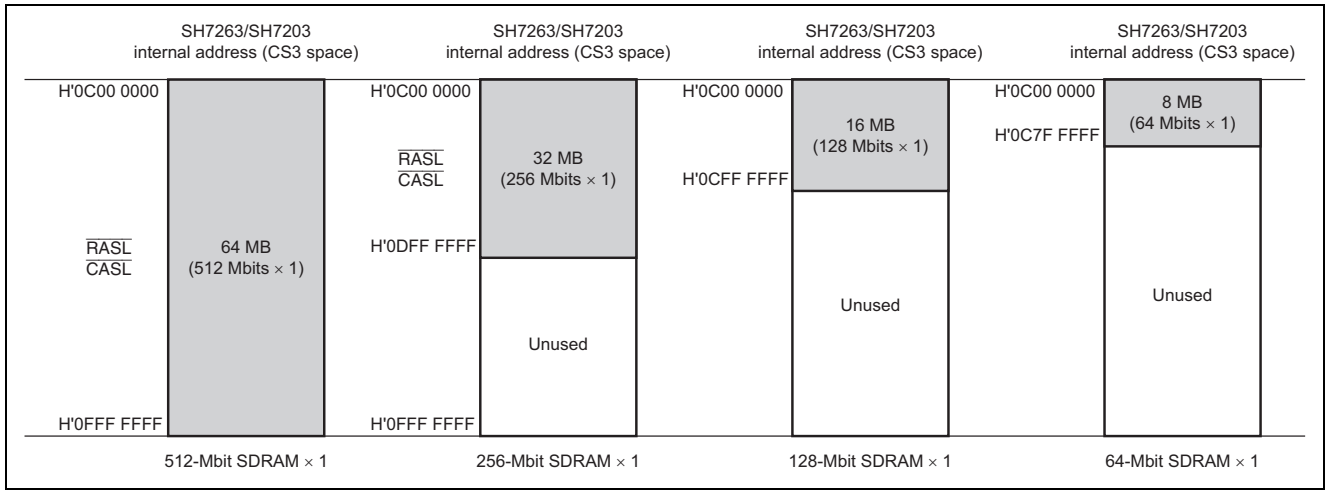


Figure 2 Memory Mapping (CS3 Space)

Note: Handling of control signal pins with external pull-up or pull-down resistors
Since the initial pin-function settings for individual control pins CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQMU, and DQML are for operation as I/O pins, the pin-function controller (PFC) must be used to switch the pin functions. Furthermore, since the initial settings for I/O pins of the MCU is for input operation, the states of the pins are undefined. To prevent undefined states on pins and stabilize memory operation, we recommend that levels on the above control pins be pulled up or down by external resistors.
The general criterion for whether the control pins should be pulled up or down is stability of operation. We thus recommend that the $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQMU, and DQML pins be pulled up (set to the high level) by external resistors.
The CKE pin is pulled down (set to the low level) by an external resistor for a reason other than that stated above. This is on the assumption that the self-refresh state is to provide continual protection of data in the SDRAM even after signals from the MCU have stopped.

2.2.1 Connection of SDRAM with 12 Bits of Row Address (A0 to A11)

The SDRAM units with 64 Mbits (product of with 8-bit column address), 128 Mbits (product with 9-bit column address), and 256 Mbits (product with 10-bit column address) listed in Table 2 are available are products with 12 bits of row address. Figure 3 shows an example of the connections for a single SDRAM unit, and table 3 gives a list of how address-output pins are multiplexed in the case of a 128-bit SDRAM (product with 9-bit column address). For the multiplexing of address-output pins in the case of other SDRAM units, refer to the *SH7263/SH7203 Group Hardware Manual*.

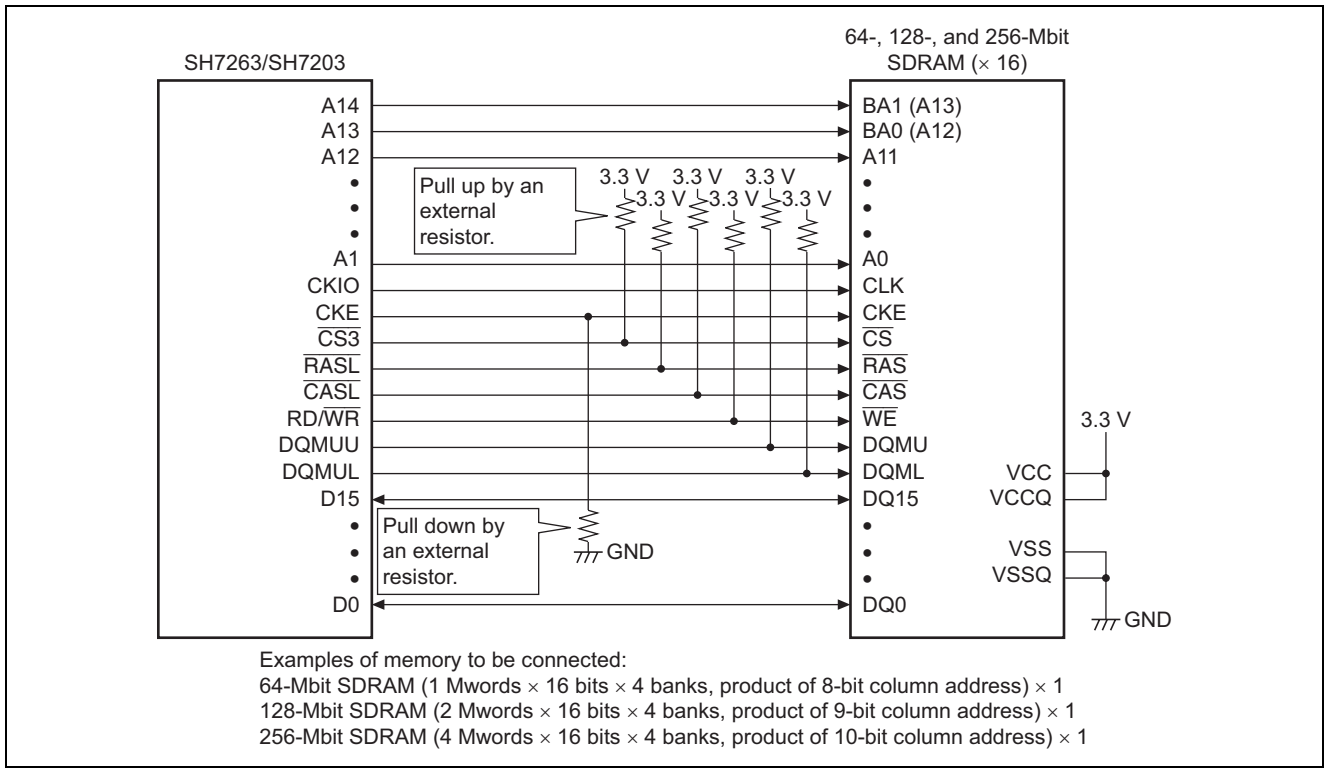


Figure 3 Example of Circuitry for SDRAM Connection (64-/128-/256-Mbit SDRAM × 1, 16-Bit Bus)

Table 3 Connections between SH7263/SH7203 Pin Functions and 128-Mbit SDRAM (Product with 9-Bit Column Address)

SH7263/SH7203 Pin	Row Address*3	Column Address*3	SDRAM Pin	Function
A14	A23*2	A23*2	A13 (BA1)	Specifies bank
A13	A22*2	A22*2	A12 (BA0)	Specifies bank
A12	A21	A12	A11	Address
A11	A20	L/H*1	A10/AP	Specifies address/pre-charge
A10	A19	A10	A9	Address
A9	A18	A9	A8	Address
A8	A17	A8	A7	Address
A7	A16	A7	A6	Address
A6	A15	A6	A5	Address
A5	A14	A5	A4	Address
A4	A13	A4	A3	Address
A3	A12	A3	A2	Address
A2	A11	A2	A1	Address
A1	A10	A1	A0	Address

Notes: 1. The L/H bit is used in command specification; it is fixed at L or H according to the access mode.
2. Bank address specification
3. The given bits are those output on the address pins during cycles of row-address/column-address output.

2.2.2 Connection of SDRAM with 13 Bits of Row Address (A0 to A12)

The SDRAM units with 256 Mbits (product with 9-bit column address) and 512 Mbits (product with 10-bit column address) listed in table 2 are available as products with 13 bits of row address. Figure 4 shows an example of the connections for a single SDRAM unit. The A25 pin is used to specify the bank address for the 512-Mbit SDRAM, so only assertion of the $\overline{\text{RASL}}$/$\overline{\text{CASL}}$ pins is required (assertion of the $\overline{\text{RASU}}$/$\overline{\text{CASU}}$ pins is not required). Table 4 gives a list of how address-output pins are multiplexed in the case of a 512-Mbit SDRAM (product with 10-bit column address). For the multiplexing of address-output pins for a 256-Mbit SDRAM unit (product with a 9-bit column address), refer to the *SH7263/SH7203 Group Hardware Manual*.

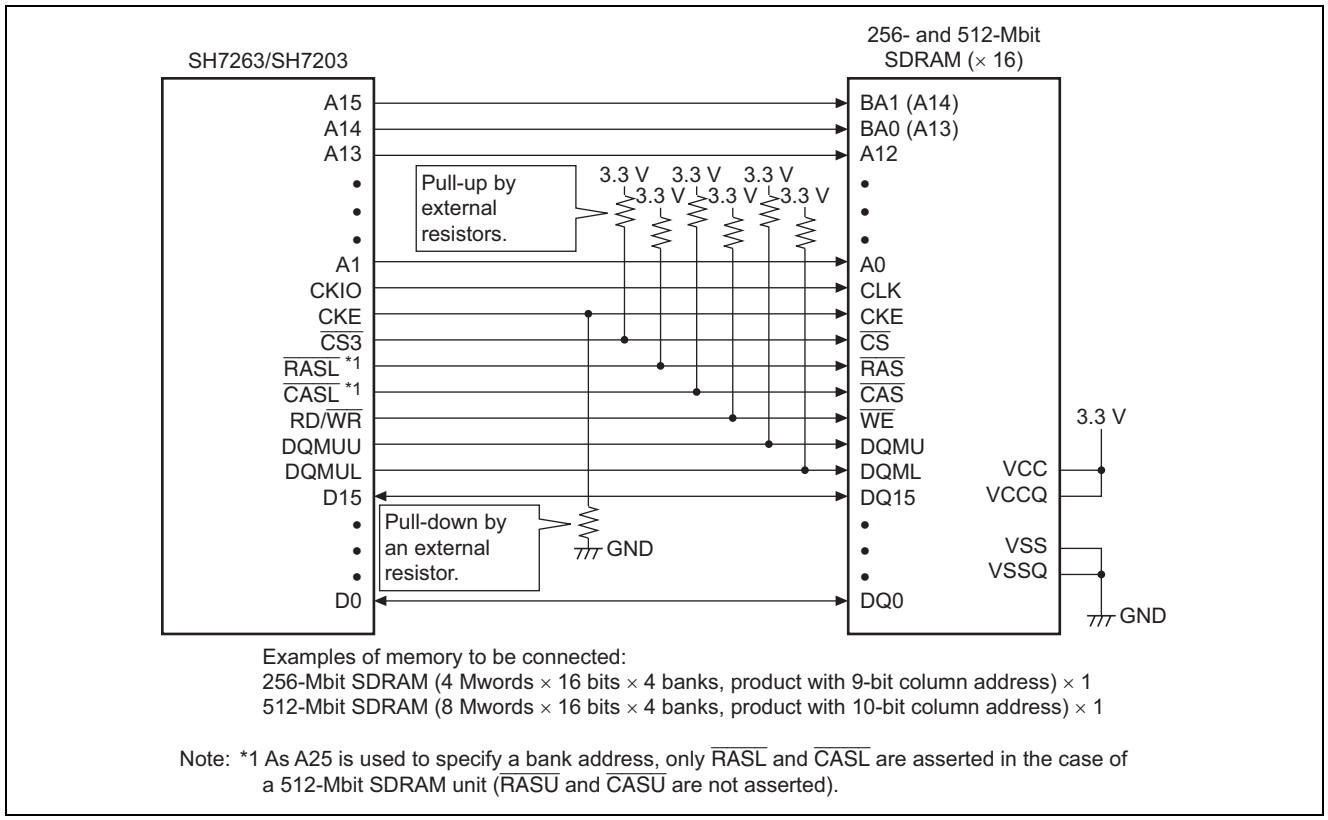


Figure 4 Example of Circuitry for SDRAM Connection (256-/512-Mbit SDRAM × 1, 16-Bit Bus)

Table 4 Connection between SH7263/SH7203 Pin Functions and 512-Mbit SDRAM (Product with 10-Bit Column Address)

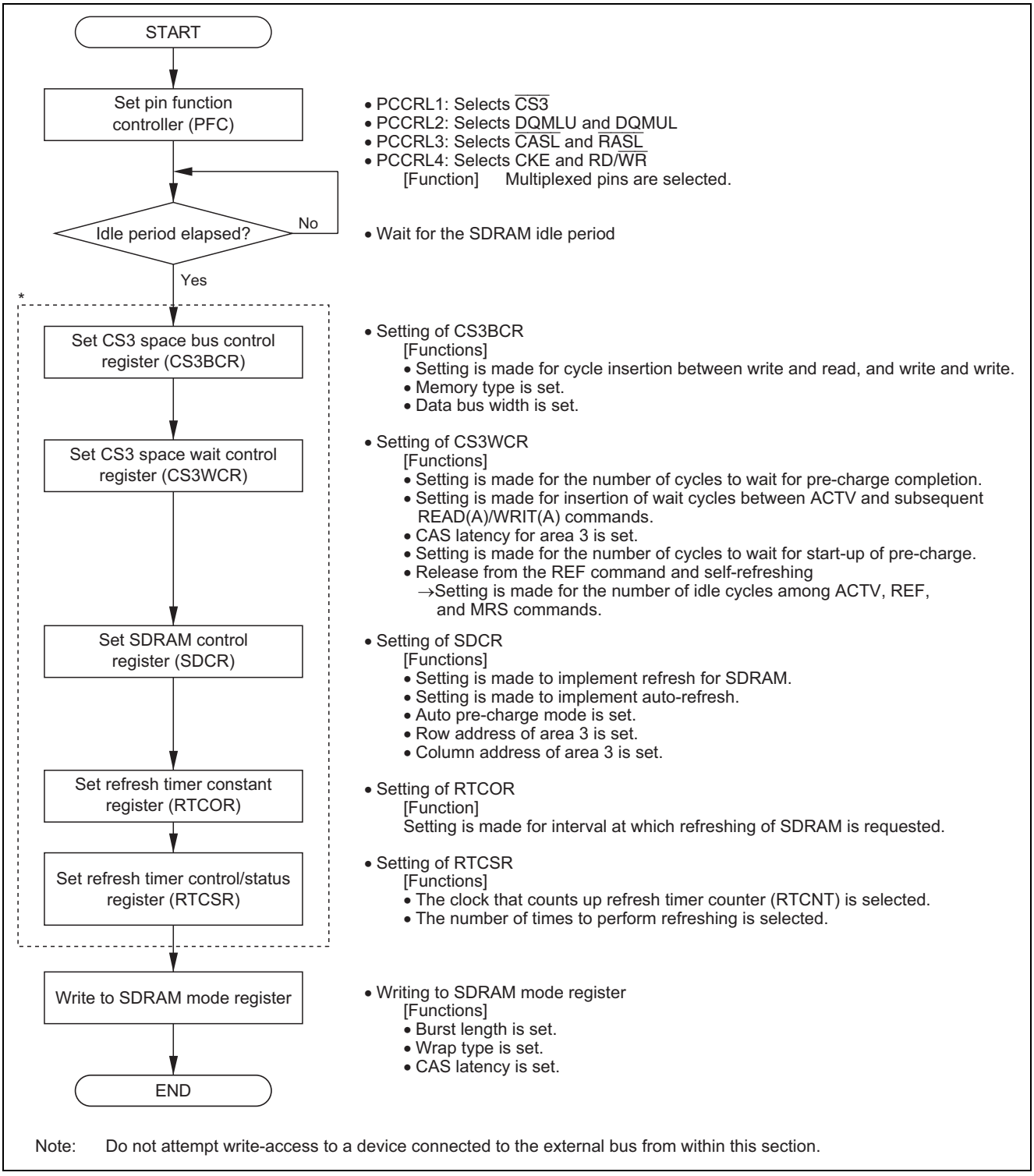
SH7263/SH7203 Pin	Row Address*4	Column Address*4	SDRAM Pin	Function
A15	A25*2*3	A25*2*3	A14 (BA1)	Specifies bank
A14	A24*2	A24*2	A13 (BA0)	Specifies bank
A13	A23	A13	A12	Address
A12	A22	A12	A11	Address
A11	A21	L/H*1	A10/AP	Specifies address/pre-charge
A10	A20	A10	A9	Address
A9	A19	A9	A8	Address
A8	A18	A8	A7	Address
A7	A17	A7	A6	Address
A6	A16	A6	A5	Address
A5	A15	A5	A4	Address
A4	A14	A4	A3	Address
A3	A13	A3	A2	Address
A2	A12	A2	A1	Address
A1	A11	A1	A0	Address

Notes: 1. The L/H bit is used in command specification; it is fixed at L or H according to the access mode.
2. Bank address specification
3. The A25 pin is used to specify the bank address, so only the $\overline{\text{RASL}}$/$\overline{\text{CASL}}$ pins are asserted for a 512-Mbit SDRAM (the $\overline{\text{RASU}}$/$\overline{\text{CASU}}$ pins are not).
4. The given bits are those output on the address pins during cycles of row-address/column-address output.

2.3 Procedure for Setting Module Used

2.3.1 Example of the Initialization Procedure for SDRAM

Figure 5 gives an example of the initialization procedure to place SDRAM in the CS3 space.



Note: Do not attempt write-access to a device connected to the external bus from within this section.

Figure 5 Example of Procedure for Initial Settings to Place SDRAM in the CS3 Space

2.3.2 Power-On Sequence

To perform SDRAM initialization, registers of the bus state controller must first be set, followed by a write to the SDRAM mode register.

Once power has been supplied, SDRAM needs a constant idle period. An idle period of at least 200 µs is set up by the software in this sample program. The required period differs with the SDRAM specification. Please refer to the manual for the SDRAM you are using.

To write to the SDRAM mode register, a mode-register setting (MRS) command is issued in combination with $\overline{CS3}$, $\overline{RASL}$, $\overline{CASL}$, and RD/$\overline{WR}$ pins. The address provides the data for input to SDRAM. Table 5 shows the addresses to be accessed in writing to the SDRAM mode register when SDRAM is allocated to the CS3 space.

Table 5 Addresses to be Accessed as Values Written to the SDRAM Mode Register (CS3 Space)

Data Bus Width	CAS Latency	Burst Read/Single Write (Burst Length 1)		Burst Read/Burst Write (Burst Length 1)	
		Access Address	External Address Pin	Access Address	External Address Pin
16 bits	2	H'FFFC 5440	H'0000 0440	H'FFFC 5040	H'0000 0040
	3	H'FFFC 5460	H'0000 0460	H'FFFC 5060	H'0000 0060
32 bits	2	H'FFFC 5880	H'0000 0880	H'FFFC 5080	H'0000 0080
	3	H'FFFC 58C0	H'0000 08C0	H'FFFC 50C0	H'0000 00C0

In this sample program, the following settings are made in the SDRAM mode register.

- Burst length: burst read/single write (burst length 1)
- Wrap type: sequential
- CAS latency: 2 cycles

As shown in table 5, these settings are written to the SDRAM mode register by writing a word of any value to H'FFFC 5440 (the data are ignored). In detail, the following commands are issued sequentially to the SDRAM.

1. All bank pre-charge command (PALL)
   Idle cycles (Tpw) as specified by the WTRP[1:0] bits in CS3WCR are inserted between the PALL and the first REF.
2. Auto-refresh command (REF; eight times)
   Idle cycles (Trc) as specified by the WTRC[1:0] bits in CS3WCR are inserted after the REF command is issued.
3. Mode-register setting command (MRS)

Figure 6 shows an example of timing in writing to the SDRAM mode register.

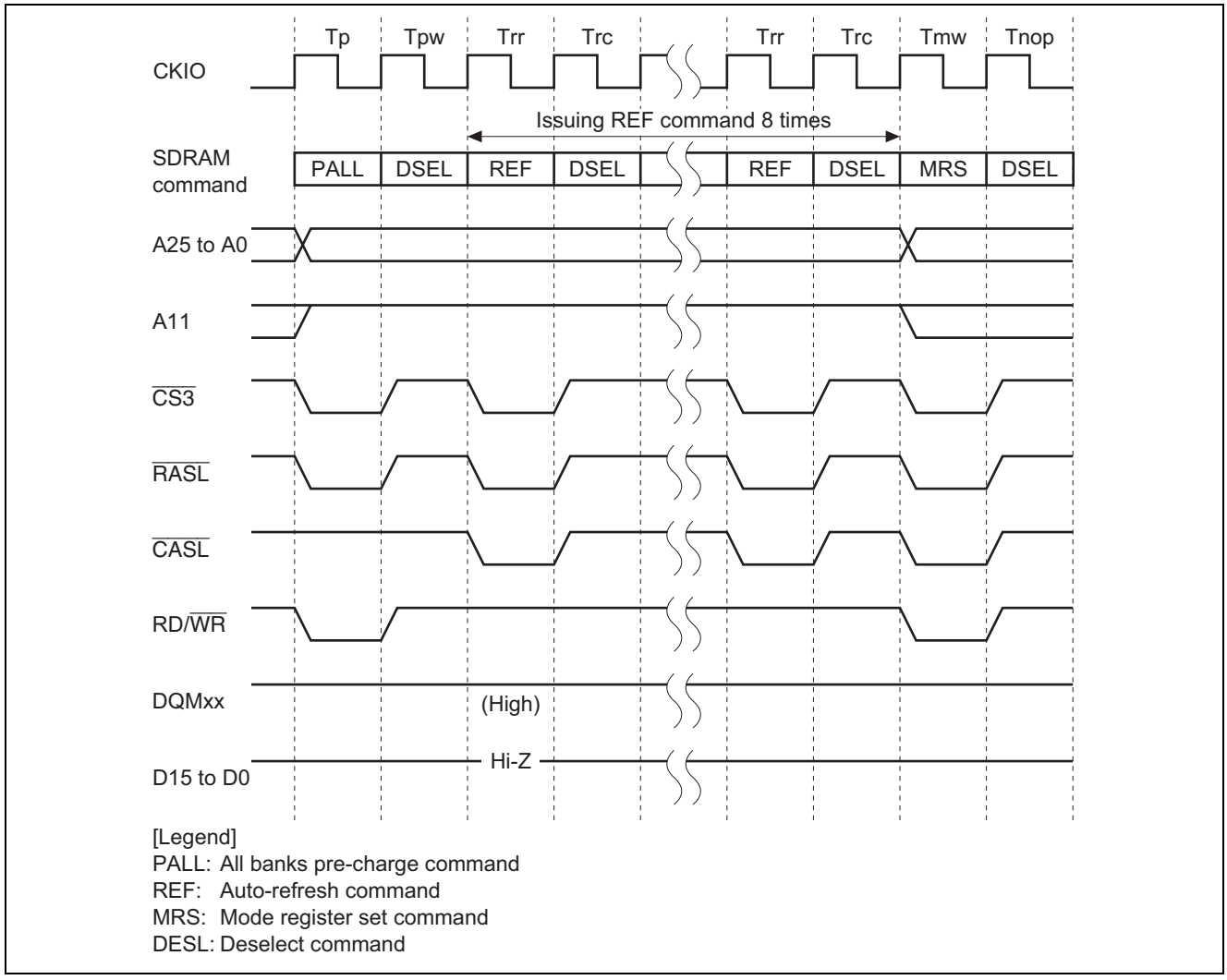


Figure 6 Example of Timing in Writing to the SDRAM Mode Register

2.4 Example of Bus State Controller Settings

Table 6 gives an example of bus state controller settings for bus-clock operation of the SH7263/SH7203 at 66.67 MHz. For details on individual registers, please refer to the section on the bus state controller in the *SH7263/SH7203 Group Hardware Manual*.

Table 6 Example of Bus State Controller Settings

Name of Register	Address	Setting	Function
CS3 space bus control register (CS3BCR)	H'FFFC 0010	H'1000 4400	• IWW[2:0] = B'001 Idle period between writing and reading and between writing and writing: 1 cycle • TYPE[2:0] = B'100: SDRAM • BSZ[1:0] = B'10: 16-bit data bus width
CS3 space wait control register (CS3WCR)	H'FFFC 0034	H'0000 4892	• WTRP[1:0] = B'10 Number of cycles to wait for pre-charge completion: 2 • WTRCD[1:0] = B'10 ACTV command → Number of wait cycles between READ (A)/WRITE (A) commands: 2 • A3CL[1:0] = B'01 CAS latency of area 3: 2 cycles • TRWL[1:0] = B'10 Number of cycles to wait for pre-charge start-up: 2 • WTRC[1:0] = B'10 REF command/self-refresh cancellation → Number of idle cycles among ACTV/REF/MRS commands: 5
SDRAM control register (SDCR)	H'FFFC 004C	H'0000 0809	• RFSH = 1: Refresh • RMODE = 0: Auto-refresh • BACTV = 0: Auto pre-charge mode • A3ROW[1:0] = B'01 Row address of area 3: 12 bits • A3COL[1:0] = B'01 Column address of area 3: 9 bits
Refresh timer control/status register (RTCSR)	H'FFFC 0050	H'A55A 0010*	• CKS[2:0] = B'010 Select Bϕ/16 as the clock • RRC[2:0] = B'000 Selects one as the number of consecutive refresh cycles
Refresh timer constant register (RTCOR)	H'FFFC 0058	H'A55A 0041*	• 1 cycle = 1/(Bϕ (66 MHz)/16) ≈ 240 ns • Interval between SDRAM-refresh requests: 4,096 cycles/64 ms = 15.625 µs/time • Setting value of RTCOR = 15.625 µs ÷ 240 ns ≈ 65 = H'41

Note*: When writing, set the higher-order 16 bits of write data to H'A55A so that the write protection is canceled.

2.5 Settings of SDRAM Timing in Sample Program

To connect SDRAM, the number of wait cycles corresponding to the access speed (CAS latency) and other AC characteristics of the SDRAM in use must be set. The interval for refreshing must also be set. This section describes the main points regarding the settings in the sample program for the cycles of waiting and refreshing.

In this sample program, the bus clock for the SH7263/SH7203 is set to 66.67 MHz (tcyc = 15 ns).

For AC characteristics of the SH7263/SH7203 and SDRAM, refer to the datasheets for the individual devices. The SDRAM starts operating on a rising edge of CKIO.

2.5.1 Cycles of Waiting for Access

1. Set cycle of waiting (Trw) between the Tr and Tc cycles.
2. Set cycle of waiting (Tcw) between the Tc and Td cycles.
3. Set cycle of waiting (Tap) between the Tde and Tr cycles.
4. Cycle of waiting (Trwl) until auto pre-charge is placed in the active state are set.
   With this setting, it is confirmed that bus timings of the SH7263/SH7203 and SDRAM are satisfied. (In this sample program, the following settings are made; Trw = 2, Tcw = 1, Tap = 1, and Trwl = 2.)
   Furthermore, Tr, Tc, Td, and Tde used in the following formulae are tcyc.

- tRC of the SDRAM (for read cycles)
  tRC (min) ≤ (tcyc × Trw) + (Tc) + (tcyc × (CL – 1)) + (Td) + (Tde) + (tcyc × Tap) + (Tr)..... (figure 7)

Note: Tr = Tc = Td = Tde = tcyc

- tRC of the SDRAM (for write cycles)
  tRC (min) ≤ (tcyc × Trw) + (Tc) + (tcyc × Trwl) + (tcyc × Tap) + (Tr) ..... (figure 11)

- tRAS of the SDRAM (column activation time)
  tRAS (min) ≤ (tcyc × Trw) + (Tc) + Td (tcyc × BL) ..... (figure 7)

- tRCD of the SDRAM (delay time from row to column)
  tRCD (min) ≤ (tcyc × Trw) + (Tc) ..... (figure 7)

- tRP of the SDRAM (column pre-charge time/for read cycles)
  tRP (min) ≤ (tcyc × (CL – 2)) + (Td) + (Tde) + (tcyc × Tap) + (Tr) ..... (figure 7)

- tRP of the SDRAM (column pre-charge time/for write cycles)
  tRP (min) ≤ (tcyc × Tap) + (Tr) ..... (figure 7)

- tDPL of the SDRAM (write recovery time)
  tDPL (min) ≤ (tcyc × Trwl)..... (figure 11)

- tDAL of the SDRAM (delay time from end of data input to Act)
  tDAL (min) ≤ (tcyc × Trwl) + (tcyc × Tap) + (Tr)..... (figure 11)

- tRRD of the SDRAM (delay time from Act to Act)
  tRRD (min) ≤ (tcyc × Tap) + (Trr) ..... (figure 13)

Note: Tpw = Tap

2.5.2 Refresh Cycle

1. Set the interval (tREF) for refreshing of the SDRAM.
2. Set cycle of waiting (Trc) between auto-refresh cycles.
   Confirm that these settings satisfy the bus-timing requirements of the SH7263/SH7203 and SDRAM.

- tREF of the SDRAM (refresh intervals)

  $tREF\ (max) \geq tcyc \times CKS \times RTCOR \times Ref\_Cyc$

Note: Ref_Cyc in the formula above is the number of refresh cycles. In the sample program, this number is 4,096. tcyc × CKS indicates clock cycles of the refresh counter. The value obtained by multiplying the number of clock cycles for the refresh counter and RTCOR is the interval between refreshing.

Reference

When Tcyc = 15 ns, CKS = 16, RTCOR = 64, and Ref_Cyc = 4,096,

- Period corresponding to number of clock cycles for the refresh counter: tcyc × CKS = 240 (ns)
- Interval between refreshing: tcyc × CKS × RTCOR = 15.36 (µs)
- Intervals corresponding to refreshing 4,096 times: tcyc × CKS × RTCOR × Ref_Cyc = 62.91 (ms)

- tRC of the SDRAM (for the refresh cycle)

  $tRC\ (min) \leq (tcyc \times Trc) + (Tr)$ ..... (figure 13)

Note: Tr = Trc = tcyc

Figure 7 shows the timing for single reading of the SDRAM (CL = 2).

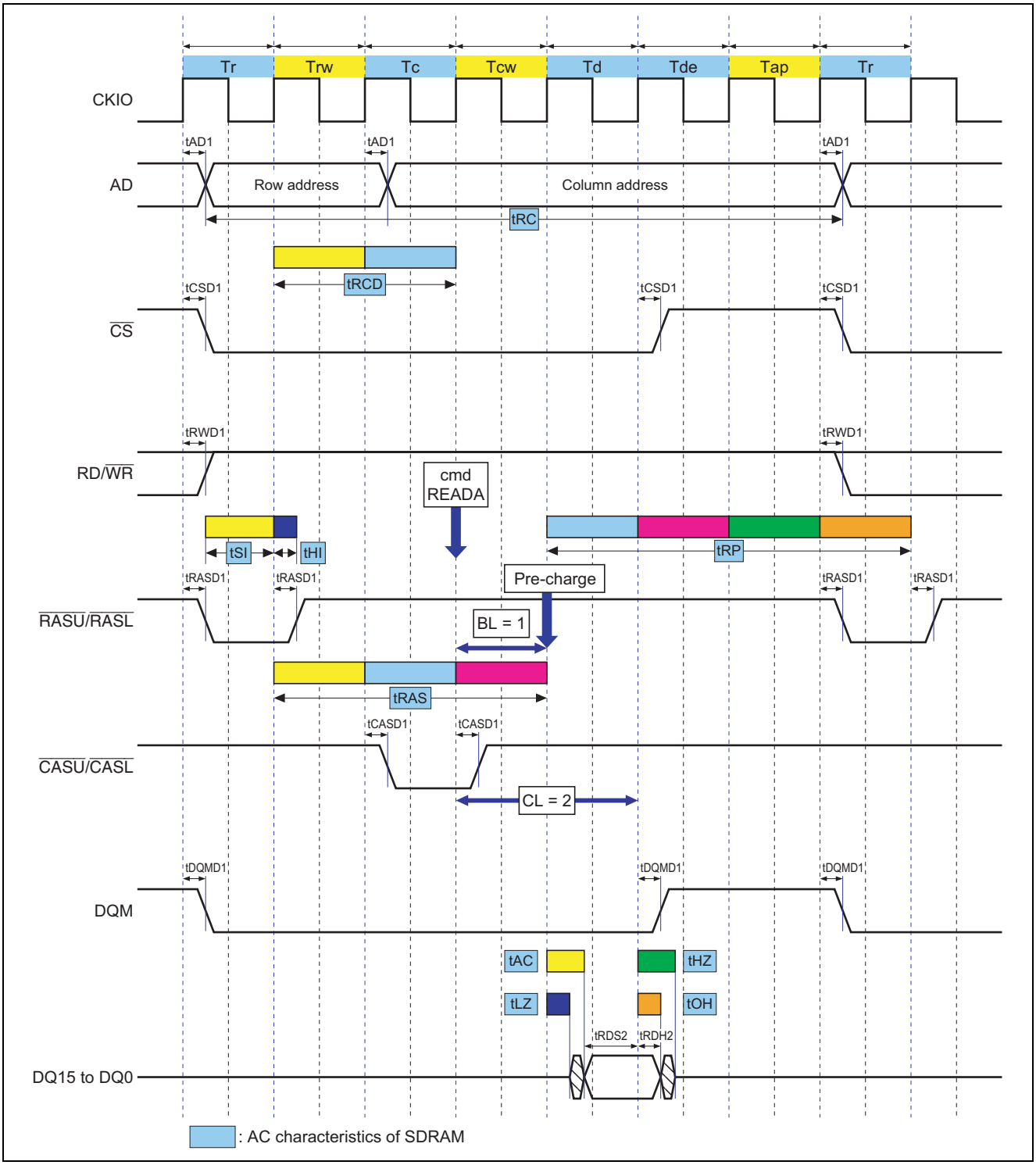


Figure 7 Timing for Single Reading of the SDRAM (CL = 2, and WTRCD = 2, A3CL = 1 and WTRP = 1)

Figure 8 shows the timing for single reading of the SDRAM (CL = 3).

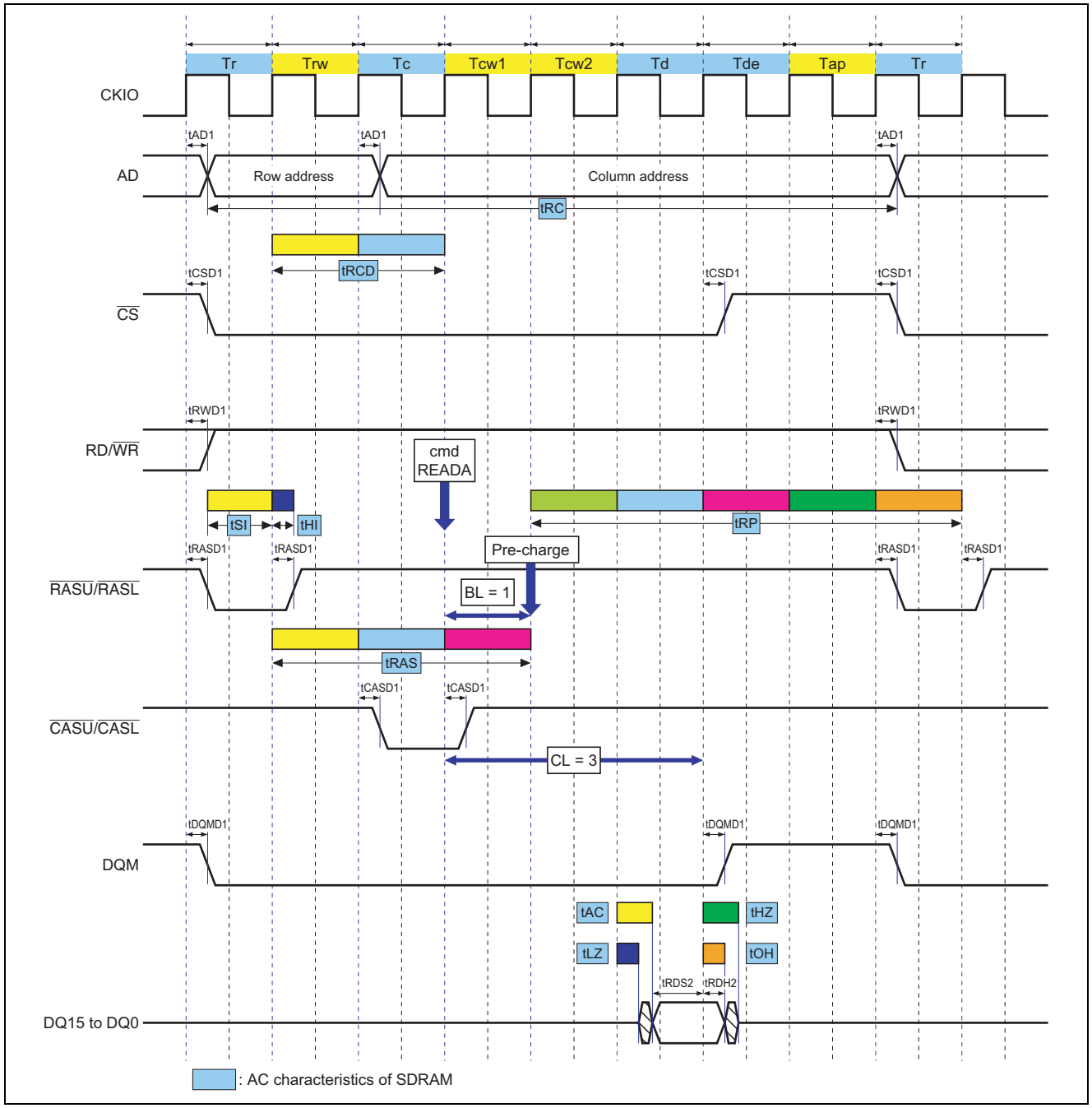


Figure 8 Timing for Single Reading of the SDRAM (CL = 3, and WTRCD = 2, A3CL = 2 and WTRP = 1)

Figure 9 shows the timing for burst reading of the SDRAM (CL = 2).

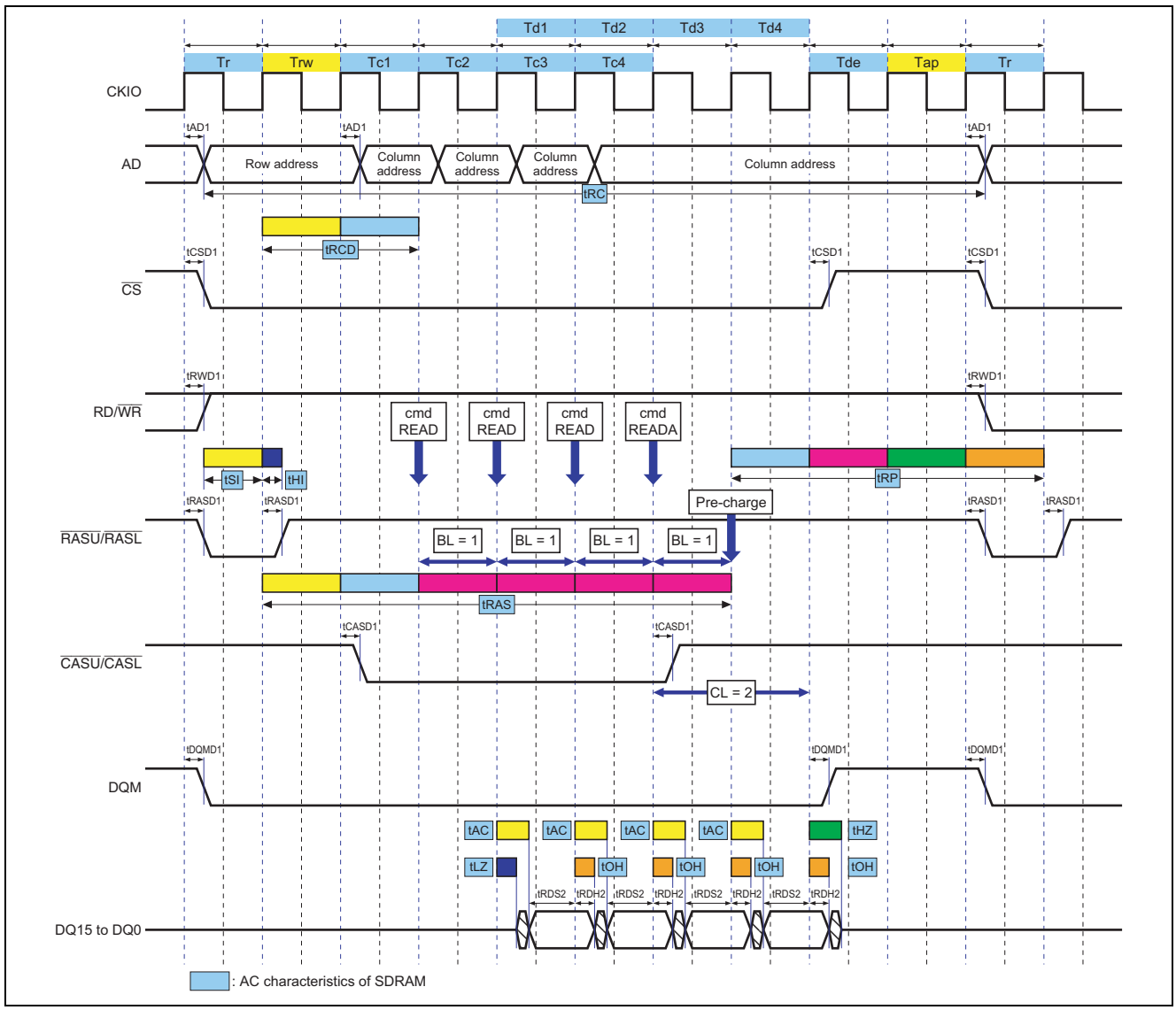


Figure 9 Timing for Burst Reading of the SDRAM (CL = 2, and WTRCD = 2, A3CL = 1 and WTRP = 1)

Figure 10 shows the timing for burst reading of the SDRAM (CL = 3).

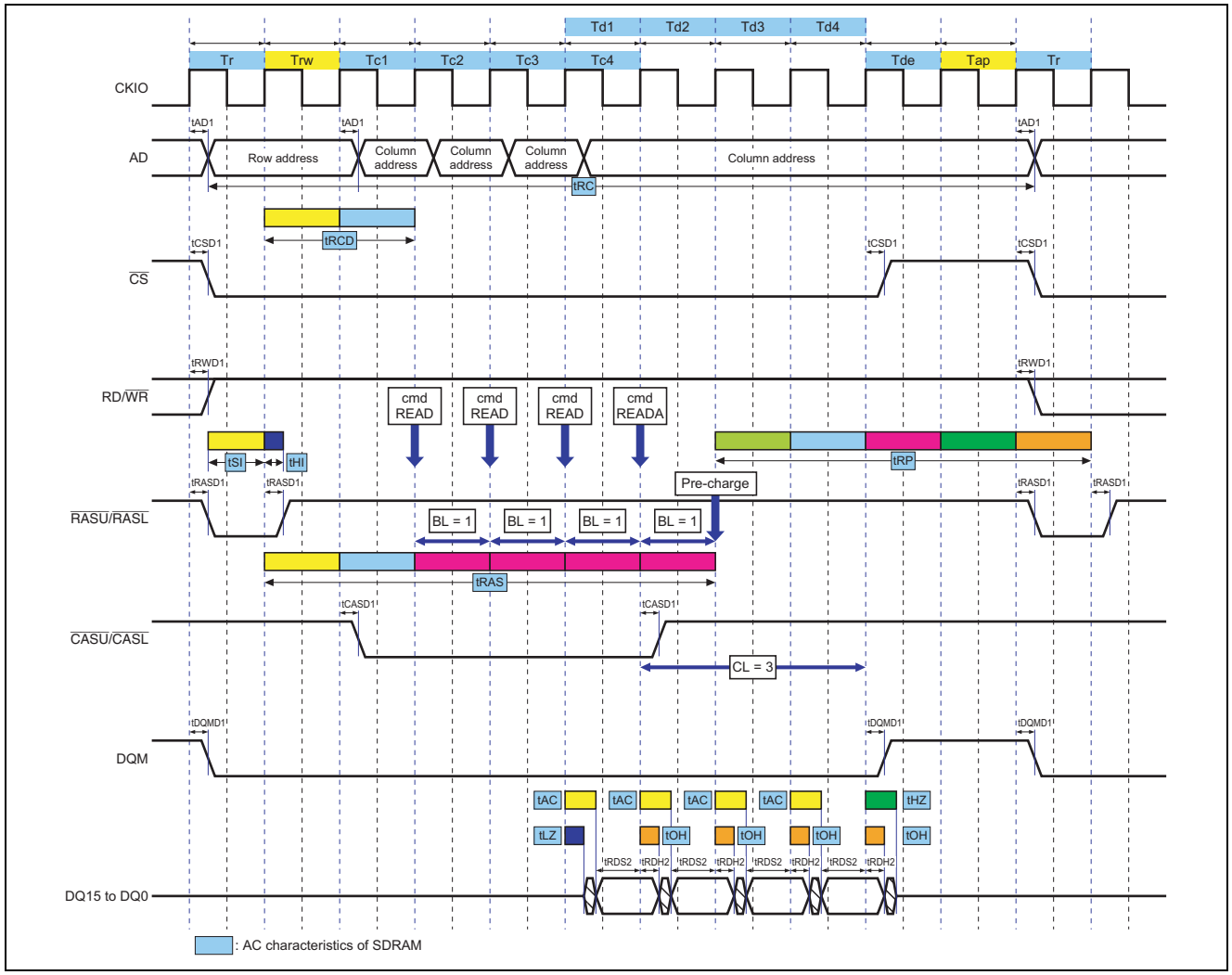


Figure 10 Timing for Burst Reading of the SDRAM (CL = 3, and WTRCD = 2, A3CL = 2 and WTRP = 1)

Figure 11 shows the timing for single writing of the SDRAM.

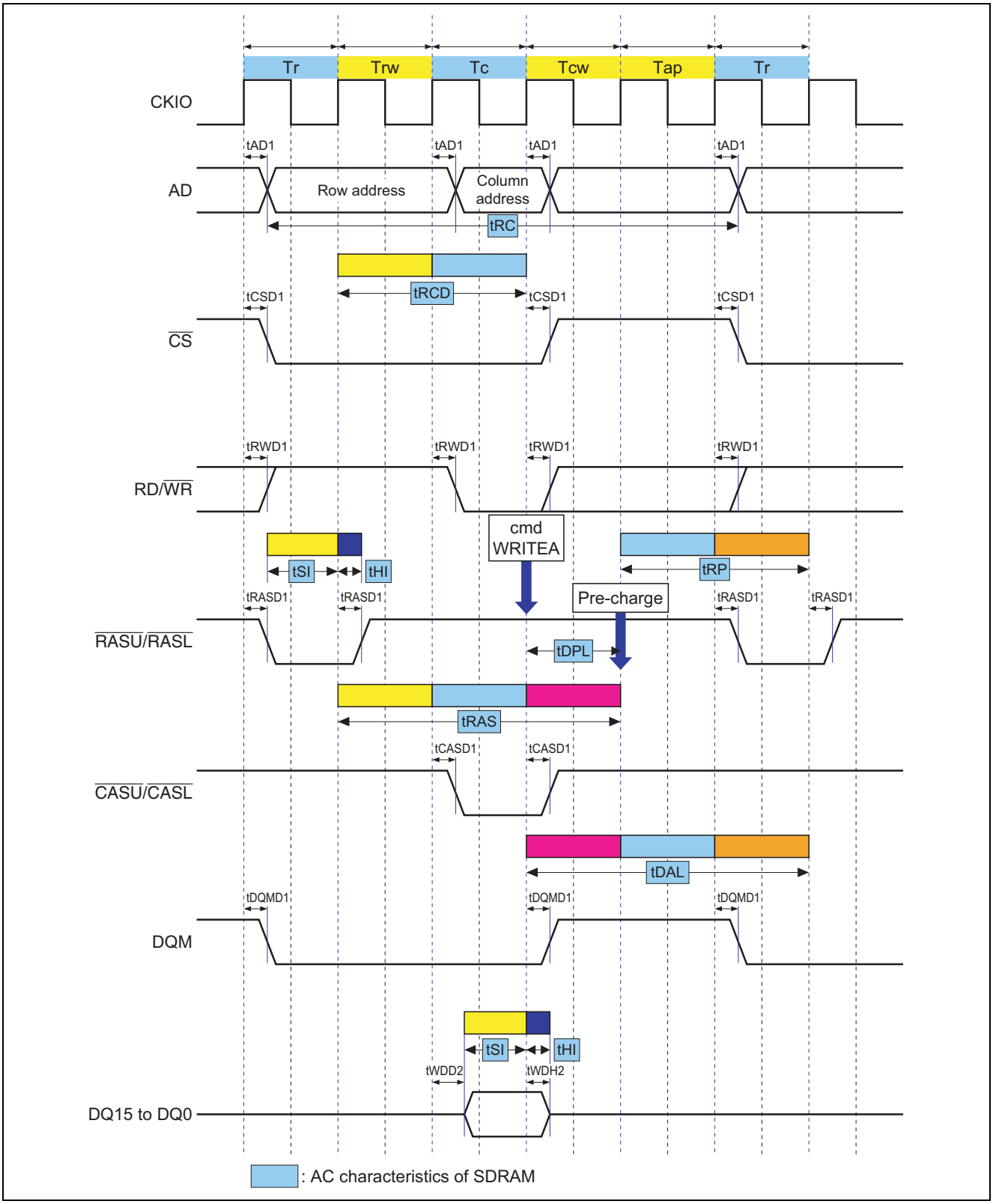


Figure 11 Timing for Single Writing of the SDRAM (WTRCD = 2, WTRP = 1, and TRWL = 1)

Figure 12 shows the timing for burst writing of the SDRAM.

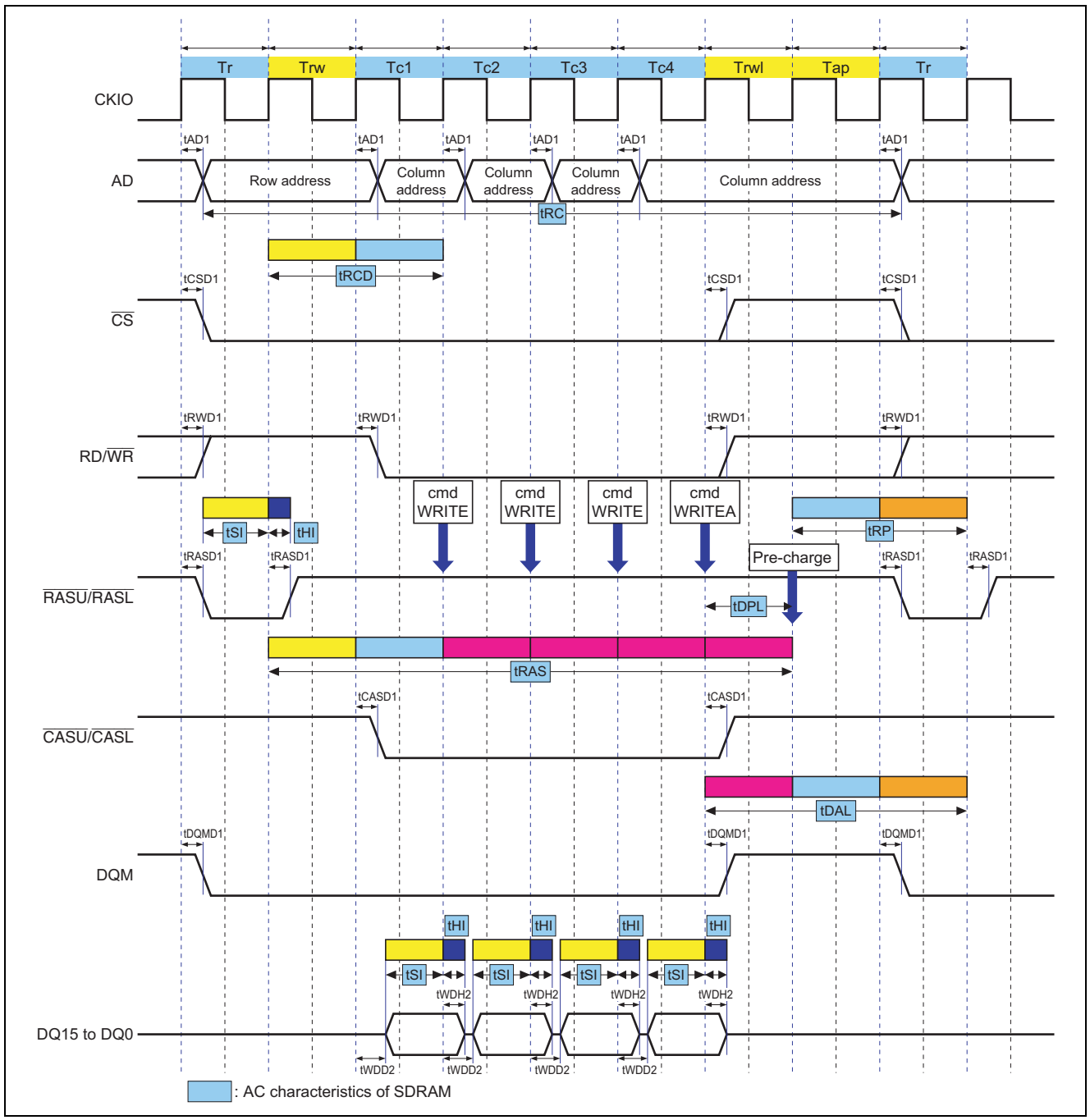


Figure 12 Timing for Burst Writing of the SDRAM (WTRCD = 2, WTRP = 1, and TRWL = 1)

Figure 13 shows timing for refreshing of the SDRAM.

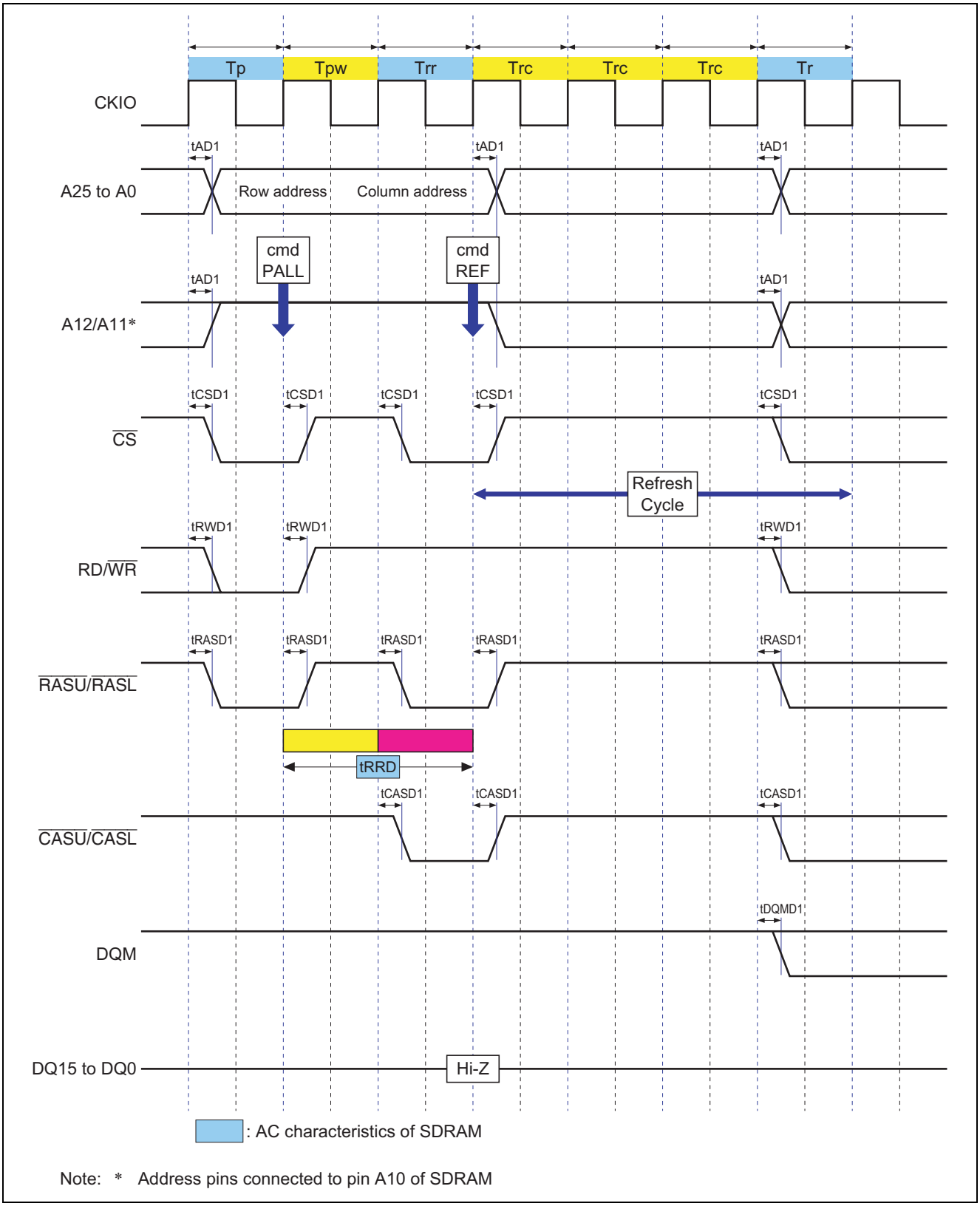


Figure 13 Timing for Refreshing of the SDRAM (WTRP = 1 and WTRC = 1)

3. Documents for Reference

- Software Manual
  SH-2A/SH-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manuals
  SH7263 Group Hardware Manual
  SH7203 Group Hardware Manual
  The most up-to-date versions of the documents are available on the Renesas Technology Website.

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