To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)
Send any inquiries to http://www.renesas.com/inquiry.
Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.

2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.

4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.

5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.

6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
   - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-terrorism systems; safety equipment; and medical equipment not specifically designed for life support.
   - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.
SH7263/SH7203 Groups
Example of BSC Interface Connection to NOR-Type Flash Memory
(16-Bit Data Bus)

Introduction
This application note describes the interface functionality of the bus state controller (BSC) and provides a practical example of connection with asynchronous NOR-type flash memory.

Target Devices
SH7263/SH7203

Contents

1. Specifications......................................................................................................................... 2
2. Description of Sample Application................................................................................... 3
3. Documents for Reference.................................................................................................... 25
1. Specifications

- 32-, 64-, or 128-Mbit NOR flash memory (from Spansion™) is connected to the SH7263 or SH7203 with a 16-bit data-bus width.
- The bus state controller (BSC) of the SH7263 or SH7203 is used to set up conditions for the execution of read and write operations for an external NOR flash memory.

1.1 Module Used

- Bus state controller (BSC)

1.2 Applicable Conditions

- Microcontroller: SH7263/SH7203 (R5S72630/R5S72030) Groups
- Flash memory: 32-Mbit product S29GL032A** (2 Mwords × 16 bits) from Spansion™
  64-Mbit product S29GL064A** (4 Mwords × 16 bits) from Spansion™
  128-Mbit product S29GL128N** (8 Mwords × 16 bits) from Spansion™
- Operating frequencies: Internal clock 200 MHz
  Bus clock 66.67 MHz

1.3 Related Application Notes

The operation of the reference program for this document was confirmed with the setting conditions described in the SH7263/SH7203 Group Hardware Manual. Please refer to the hardware manual with this application note.
2. Description of Sample Application

2.1 Operational Overview of Module Used

The BSC of the SH7263/SH7203 is used to control externally connected NOR flash memory. Table 1 gives specifications of the NOR flash memory used in this sample program.

### Table 1 Specifications of NOR Flash Memory for the SH7263/SH7203

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type no.</td>
<td>S29GL032A** (from Spansion™)</td>
</tr>
<tr>
<td>Configuration</td>
<td>4 MB (2 Mwords x 16 bits x 1)</td>
</tr>
<tr>
<td>Data bus width</td>
<td>16 bits</td>
</tr>
<tr>
<td>Access time</td>
<td>In random access: 90 ns (max.)</td>
</tr>
<tr>
<td></td>
<td>In page reading: 25 ns (max.)</td>
</tr>
<tr>
<td>Boot block</td>
<td>Top-boot and bottom-boot devices identified by the model no.</td>
</tr>
</tbody>
</table>

Figure 1 shows a memory map. Type of memory to be connected and data-bus width are specified by individual CS space. In this sample program, NOR flash memory is connected to the CS0 space.

![Memory Map](image)

**Figure 1 Memory Map (32-/64-/128-Mbit Product)**
Figures 3, 4, and 5 show examples of circuits used to connect NOR flash memory.

SH7263/SH7203 is connected to NOR flash memory with a 16-bit data bus width. To set up NOR flash memory with a data-bus width of 16 bits, the BYTE pin is fixed to the high level. To set up space CS0 of the SH7263/SH7203 for the same bus width, the MD pin is fixed to the low level.

Note: Endian

The SH 7263/SH7203 supports both big endian, in which the most significant byte (MSB) of data is that in the direction of the 0th address, and little endian, in which the least significant byte (LSB) is that in the direction of the 0th address. In the initial state after a power-on reset, all areas will be in big endian mode. Little endian cannot be selected for area 0. However, the endian of areas 1 to 7 can be changed by the setting in the CSnBCR register setting as long as the target space is not being accessed.

![Diagram of Connection between the SH7263/SH7203 and NOR Flash Memory](image)

**Figure 2**  Example of Connection between the SH7263/SH7203 and NOR Flash Memory over a 16-Bit Data Bus
Example of BSC Interface Connection to NOR-Type Flash Memory

(16-Bit Data Bus)

**Figure 3** Circuit Example 1 for Flash Memory Connection (32-Mbit Product/4 MB, 16-Bit Bus)

**Figure 4** Circuit Example 2 for Flash Memory Connection (64-Mbit Product/8 MB, 16-Bit Bus)
Table 2 gives a list of pin functions of the SH7263/SH7203. Since pins A21, A22, A23, and WE0 are initially set for operation as I/O pins, the pin-function controller (PFC) must be used to switch the pin functions.

When a boot program is executed from the NOR flash memory connected to space CS0, the I/O pins of the MCU are in their initial state (operating as input pins), the states of the pins are not fixed so can become undefined and have an adverse effect on the memory. Thus, to ensure correct reading of the specified addresses in space CS0, pins A21, A22, and A23 must be pulled down to the low level by an external resistor. We also recommend the use of external resistors to apply pull-up processing and thus stabilize the operation of control signals (CS0, WE0, and RD).
### Table 2  List of Pin Functions for the SH7263/SH7203

<table>
<thead>
<tr>
<th>SH7263 Pin</th>
<th>I/O</th>
<th>Initial Pin Function</th>
<th>Function in the Circuit Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>A23</td>
<td>Output</td>
<td>I/O pin (PE4)</td>
<td>Address bus (for connection of the 128-Mbit product)</td>
</tr>
<tr>
<td>A22</td>
<td>Output</td>
<td>I/O pin (PE3)</td>
<td>Address bus (for connection of the 64- or 128-Mbit product)</td>
</tr>
<tr>
<td>A21</td>
<td>Output</td>
<td>I/O pin (PE2)</td>
<td>Address bus (for connection of the 32-, 64-, or 128-Mbit product)</td>
</tr>
<tr>
<td>A20 to A1</td>
<td>Output</td>
<td></td>
<td>Address bus</td>
</tr>
<tr>
<td>D15 to D0</td>
<td>Input/output</td>
<td>D15 to D0</td>
<td>Data bus</td>
</tr>
<tr>
<td>RD</td>
<td>Output</td>
<td>RD</td>
<td>Read pulse signal (read data out enable signal)</td>
</tr>
<tr>
<td>WE0</td>
<td>Output</td>
<td>I/O pin (PC4)</td>
<td>Indicates byte write on D15 to D0</td>
</tr>
<tr>
<td>CS0</td>
<td>Output</td>
<td>CS0</td>
<td>Chip selection</td>
</tr>
<tr>
<td>MD</td>
<td>Input</td>
<td>MD</td>
<td>Selects initial values for the CS0 space data-bus width and CS1 to CS7 space data-bus widths. The CS0 space data-bus width cannot be changed after a power-on reset.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MD</th>
<th>Data-bus width</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32 bits</td>
</tr>
<tr>
<td>0</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

(set value in the sample program)
2.2 Procedure for Setting Modules Used

NOR flash memory is read by either of two methods: ① random-access reading and ② page reading. The bus-state controller settings for the two methods are different. The procedures for settings in both methods are described in this section.

Some devices may not support page reading. Furthermore, page reading is also divided into two types, clock synchronous and asynchronous. This application note describes page reading of the asynchronous type.

2.2.1 Procedure for Settings to Use Random-Access Reading

Random-access reading can be used in spaces CS0 to CS7. The TYPE[2:0] bits of the bus control register (CSnBCR, n = 0 to 7) of the space in use are set to "Normal space (B'000)".

Table 3 gives a list of examples for setting the bus state controller with space CS0 in use. For details on the individual registers, see the section on the bus state controller in the SH7263/SH7203 Group Hardware Manual.

Figure 6 shows an example of the procedure for setting the bus state controller.

<table>
<thead>
<tr>
<th>Name of Register</th>
<th>Address</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| CS0 space bus control register (CS0BCR) | H'FFFC 0004 | H'2000 0400    | • IWW[2:0] = B'010  
Idle period between writing and reading and between writing and writing: 2 cycles  
Settings should be made to these bits between writing and writing so as to satisfy the standards for tWPH of NOR flash memory.  
• TYPE[2:0] = B'000  
These bits set the type of memory connected to a space.  
: Normal space  
[Note]  
Writing to the BSZ[1:0] bits (data-bus width specification) in this register is ignored. The MD pin should be used to specify the data-bus width of space CS0.  
Note that settings of bits other than those stated above are not required. Bits other than above should remain in their initial settings. |
| CS0 space wait control register (CS0WCR) | H'FFFC 0028 | H'0000 0B41    | • SW[1:0] = B'01  
Number of delay cycles from address and CS0 assertion to RD and WE assertion: 1.5  
• WR[3:0] = B'0110  
Read access wait cycles: 6  
• WM = B'1  
External wait input is ignored  
• HW[1:0] = B'01  
Delay cycles from RD and Wn negation to address and CS0 negation: 1.5 |
Figure 6   Example 1 of Procedure for Setting Bus State Controller (CS0 Space)
2.2.2 Procedure for Settings to Use Page Reading

Page reading (in asynchronous) can be used for spaces CS0 and CS4. Set the TYPE[2:0] bits of the bus control register (CSnBCR, n = 0 or 4) for the space in use to "Burst ROM (B'001)". To connect burst ROM to the CS0 space, set the TYPE[2:0] bits to burst ROM after changing the settings of the CS0WCR register to those required for the burst ROM in use.

Table 4 gives a list of examples for setting the bus state controller when the CS0 space is in use. For details on individual registers, see the chapter on the bus state controller described in the SH7263/SH7203 Group Hardware Manual.

Figure 7 shows an example of the procedure for setting the bus state controller.

Table 4 Example 2 for Setting Bus State Controller

<table>
<thead>
<tr>
<th>Name of Register</th>
<th>Address</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS0 space bus control register (CS0BCR)</td>
<td>H'FFFC 0004</td>
<td>H'2000 1400</td>
<td>• IWW[2:0] = B'010&lt;br&gt;Idle period between writing and reading and between writing and writing: 2 cycles&lt;br&gt;Settings should be made to these bits between writing and writing so as to satisfy standard of tWPH of NOR flash memory.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• TYPE[2:0] = B'001&lt;br&gt;These bits set the type of memory connected to a space. : Burst ROM (clock asynchronous) [Note]&lt;br&gt;Writing to the BSZ[1:0] bits (data-bus width specification) in this register is ignored. The MD pin should be used to specify the data-bus width of space CS0. Note that settings of bits other than those stated above are not required. Other bits should remain their initial settings.</td>
</tr>
<tr>
<td>CS0 space wait control register (CS0WCR)</td>
<td>H'FFFC 0028</td>
<td>H'0013 03C0</td>
<td>• BST[1:0] = B'01&lt;br&gt;Burst count specification: 2 burst × four times</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• BW[1:0] = B'11&lt;br&gt;Burst wait cycles: 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• W[3:0] = B'0111&lt;br&gt;Access wait cycles: 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• WM = B'1&lt;br&gt;External wait input is ignored</td>
</tr>
</tbody>
</table>
**Figure 7  Example 2 of Procedure for Setting Bus State Controller (CS0 Space)**

- **PCCRL2**: Selects WE0
- **PECRL1**: Selects A21 (for connection of the 32-, 64-, or 128-Mbit product)
- **PECRL2**: Selects A22 (for connection of the 64- or 128-Mbit product)

- Setting of CS0BCR
  - Setting is made for insertion of idle cycles between write and read, and write and write.
  - Memory for connection is selected (normal space)

- Setting of CS0WCR
  - The burst count is set.
  - The number of burst wait cycles is set.
  - The number of access wait cycles is set.
  - External wait mask is specified.

- Setting of CS0BCR
  - Memory for connection is selected (burst ROM).
2.3  Settings of NOR Flash Memory Timing in Sample Program

To connect NOR flash memory, the number of wait cycles that corresponds to the access speed of the flash memory in use must be set. This section describes the main points regarding the settings in the sample program for the cases of random-access reading and page reading.

In this sample program, the bus clock for the SH7263/SH7203 is set to 66.67 MHz (tcyc = 15 ns).

For AC characteristics of NOR flash memory and the SH7263/SH7203, refer to the datasheets of the individual devices.

2.3.1  Reference Examples for Setting Flash Memory with Random-Access Reading in Use (Space CS0)

1. Extension of CSn assertion period

A. Cycles of delay from address and CS0 assertion to RD and WE0 assertion (Th)
   Confirm that tCS (chip enable setup time) for the NOR flash memory in use is satisfied. In this sample program, the number of cycles of delay (Th) is the setting of the SW bits in the CS0 space wait control register (CS0WCR) minus 0.5 cycles (Th = SW – 0.5 cycles). In the following reference example, the setting is for Th = 1.0.
   \[
   tCS(\text{min}) \leq tCS_{\text{min}} - 0.5 \text{ cycles} \tag{P20}
   \]

   \[
   \begin{align*}
   tCS(\text{min}) & \leq tCS_{\text{min}} - 0.5 \text{ cycles} \\
   & \leq (T1 - tSED1_{\text{max}}) + (tcyc \times Tw) + (T2) + (tcyc \times Tf) + (tAD1_{\text{min}}) \tag{P14 P3 P16 P17 P18}
   \end{align*}
   \]

   \[\text{......}(\text{figure 10)}\]

B. Cycles of delay from RD and WE0 negation to address and CS0 negation (Tf)
   Confirm that tAH (address hold time) for the NOR flash memory in use is satisfied. In this sample program, the number of cycles of delay (Tf) is the setting of the HW bits in the CS0 space wait control register (CS0WCR) minus 0.5 cycles (Tf = HW – 0.5 cycles). In the following reference example, the setting is for Tf = 1.0.
   \[
   tAH(\text{min}) \leq (T1 - tSED1_{\text{max}}) + (tcyc \times Tw) + (T2) + (tcyc \times Tf) + (tAD1_{\text{min}}) \tag{P14 P3 P16 P17 P18}
   \]

   \[\text{......}(\text{figure 10)}\]

2. Access wait cycles

Cycles to wait (Tw) between T1 and T2 cycles.

With this setting, confirm that bus timing requirements of the SH7263/SH7203 and NOR flash memory that is in use are satisfied. In this reference example, the setting is for one wait cycle (Tw = 1).

Additionally, T1 and T2 used in the following formula are tcyc.

\[
\text{tRC (read cycle time) of NOR flash memory...}(\text{figure 8)}
\]

\[
\text{tRC(\text{min})} \leq (\text{tcyc} \times Th - tCSD1_{\text{max}}) + (T1) + (\text{tcyc} \times Tw) + (T2 - tRDS1_{\text{min}}) \tag{P5 P2 P3 P4}
\]

Note: The applicable condition was originally tRC (min) \leq \text{tcyc} \times Th + T1 + \text{tcyc} \times Tw + T2 + \text{tcyc} \times Tf. In this sample program, however, we apply tRC = tCE to take as the strictest condition.
• tACC of NOR flash memory (address access time) .................................................................................... (figure 8)
  \[ t_{ACC}(\text{max}) \leq (T1) + (T2 - t_{RDS1\_min}) \]

• tCE of NOR flash memory (CE access time) .................................................................................... (figure 8)
  \[ t_{CE}(\text{max}) \leq (T1) + (T2 - t_{RDS1\_min}) \]

• tOE of NOR flash memory (OE access time) .................................................................................... (figure 8)
  \[ t_{OE}(\text{max}) \leq (T1 - t_{RSD\_max}) + (T2 - t_{RDS1\_min}) \]

• tOH of NOR flash memory (retention time from data output in the previous-cycle) ...................... (figure 8)
  \[ t_{OH}(\text{min}) \leq t_{RDH1\_min} \]

• tWC of NOR flash memory (write cycle time) .................................................................................... (figure 9)
  \[ t_{WC}(\text{min}) \leq (T1 - t_{WED1\_max}) + (T2 + t_{WED1\_min}) \]

• tAS of NOR flash memory (address setup time) ............................................................................. (figure 9)
  \[ t_{AS}(\text{min}) \leq t_{AS\_min} \]

• tWP of NOR flash memory (write pulse width) .................................................................................... (figure 10)
  \[ t_{WP}(\text{min}) \leq (T1 - t_{WED1\_max}) + (t_{WED1\_min}) \]

• tDS of NOR flash memory (data setup time) .................................................................................... (figure 9)
  \[ t_{DS}(\text{min}) \leq (T1 - t_{WDD1\_max}) + (t_{WED1\_min}) \]

• tDH of NOR flash memory (data hold time) .................................................................................... (figure 9)
  \[ t_{DH}(\text{min}) \leq t_{WDH4\_min} \]

3. Wait between cycles of access
This setting is for the insertion of a wait between consecutive cycles of access.
Ensure that this setting satisfies tWPH ("H" write pulse width) for the target NOR flash memory. In this reference example, the number of cycles between writing and reading, and writing and writing, is one.
  \[ t_{WPH}(\text{min}) \leq (T1 - t_{WED1\_max}) + (T1) + (T2 + t_{WED1\_min}) \]
Figure 8 shows read timing 1 for NOR flash memory (1).
Figure 9 shows write timing 1 for NOR flash memory (1).

Figure 9  Write Timing for NOR Flash Memory When SW = 1, WR = 1, and HW = 1 (1)
Figure 10 shows write timing for NOR flash memory (2).
Figure 11 shows write timing for NOR flash memory (3).
2.3.2 Reference Examples for Setting Flash Memory with Page Reading in Use (Space CS0)

1. Extension of CSn assert period
   For page reading in the CS0 space, extension of CSn assert period cannot be set. Therefore, both of the following numbers of cycles of delay are set to 0.5 (fixed): ① cycles of delay from address and CS0 assertion to RD and WE0 assertion (Th), and ② cycles of delay from RD and WE0 negation to address and CS0 negation (Tf).
   In this sample program, settings for numbers of cycles of delay (Th) and (Tf) are the number of cycles minus (fixed) (Th = Tf = 0.5 – 0.5 = 0 cycle). In the following reference example, the setting is Th = Tf = 0.0.
   Ensure that the settings satisfy tCS (chip enable setup time) and tAH (address hold time) requirements for the NOR flash memory that is in use.
   \[
   \text{tCS(min)} \leq \text{tCS \_ min} \\
   \text{tAH(min)} \leq (T1 – tWED1\_max) + (\text{tcyc} \times \text{Tw}) + (T2) + (\text{tAD1\_min}) \\
   \]
   (figure 14)

2. Access wait cycles
   Set wait cycles (Tw) which are inserted into the first access cycles.
   Ensure that this setting satisfies the bus-timing requirements of the SH7263/SH7203 and the NOR flash memory that is in use. In the following reference example, one wait cycle (Tw = 1) is set.
   Furthermore, T1 and T2B used in the following formulae are tcyc.
   - tRC of NOR flash memory (read cycle time) .......................................................... (figure 12)
     \[
     \text{tRC(min)} \leq (T1 – tCSD1\_max) + (\text{tcyc} \times \text{Tw}) + (T2B – tRDS\_min) \\
     \]
     (figure 14)
   - tACC of NOR flash memory (access-access time) .................................................. (figure 12)
     \[
     \text{tACC(max)} \leq (T1 – tAD1\_max) + (\text{tcyc} \times \text{Tw}) + (T2B – tRDS\_min) \\
     \]
     (figure 12)
   - tCE of NOR flash memory (CE access time) ......................................................... (figure 12)
     \[
     \text{tCE(max)} \leq (T1 – tCSD1\_max) + (\text{tcyc} \times \text{Tw}) + (T2B – tRDS\_min) \\
     \]
     (figure 12)
   - tOE of NOR flash memory (OE access time) ......................................................... (figure 12)
     \[
     \text{tOE(max)} \leq (T1 – tRSD\_max) + (\text{tcyc} \times \text{Tw}) + (T2B – tRDS\_min) \\
     \]
     (figure 12)
   - tPACC of NOR flash memory (page access time/the second and subsequent access cycles) .......... (figure 12)
     \[
     \text{tPACC(max)} \leq (T2B – tAD2\_max) + (\text{tcyc} \times \text{Twb}) + (T2B – tRDS\_min) \\
     \]
     (figure 12)
   - tOH of NOR flash memory (retention time for previous cycle data output) ....................... (figure 12)
     \[
     \text{tOH(min)} \leq \text{tRDH3\_min} \\
     \]
   - tWC of NOR flash memory (write cycle time) ....................................................... (figure 13)
     \[
     \text{tWC(max)} \leq (T1 – tAD1\_max) + (\text{tcyc} \times \text{Tw}) + (T2) + (\text{tAD1\_min}) \\
     \]
     (figure 13)
• tAS of NOR flash memory (address setup time)
  \[ t_{AS}(\text{min}) \leq t_{AS\_min} \]  
  \((\text{PB17})\)

• tWP of NOR flash memory (write pulse width)
  \[ t_{WP}(\text{min}) \leq (T1 - t_{WED1\_max}) + (t_{cyc} \times T_w) + (t_{WED1\_min}) \]  
  \((\text{PB14 PB2 PB9})\)

• tDS of NOR flash memory (data setup time)
  \[ t_{DS}(\text{min}) \leq (T1 - t_{WDD1\_max}) + (t_{cyc} \times T_w) + (t_{WED1\_min}) \]  
  \((\text{PB10 PB2 PB9})\)

• tDH of NOR flash memory (data hold time)
  \[ t_{DH}(\text{min}) \leq t_{WDH4\_min} \]  
  \((\text{PB12})\)

3. Wait between access cycles
   This setting is for the insertion of waiting time between consecutive cycles of access.
   With this setting, confirm that \(t_{WPH}\) ("H" write pulse width) of the target NOR flash memory is satisfied. In this reference example, one cycle \((T_{aw} = 1)\) is set as wait cycles between writing and reading, and writing and writing.
   \[ t_{WPH}(\text{min}) \leq (T2 - t_{WED1\_max}) + (t_{cyc} \times T_{aw}) + (t_{WED1\_min}) \]  
   \((\text{PB11 PB15 PB16})\)
Figure 12 shows page read timing for NOR flash memory (1).

![Page Read Timing for NOR Flash Memory When W = 1, BW = 1, and BST = 2 (1)](image)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ACC}$</td>
<td>$PB_1 + PB_2 + PB_3$</td>
</tr>
<tr>
<td>$PB_1$</td>
<td>$T_1 - t_{AD1_{\text{max}}}$</td>
</tr>
<tr>
<td>$PB_2$</td>
<td>$t_{cyc} \times Tw_2$</td>
</tr>
<tr>
<td>$PB_3$</td>
<td>$T_2B - t_{RSD_{3\text{max}}}$</td>
</tr>
<tr>
<td>Note:</td>
<td>$T_1 = T_2 = t_{cyc}$</td>
</tr>
<tr>
<td>$t_{CE}$</td>
<td>$PB_4 + PB_2 + PB_3$</td>
</tr>
<tr>
<td>$PB_4$</td>
<td>$T_1 - t_{CSD1_{\text{max}}}$</td>
</tr>
<tr>
<td>$PB_2$</td>
<td>$t_{cyc} \times Tw_2$</td>
</tr>
<tr>
<td>$PB_3$</td>
<td>$T_2B - t_{RSD_{3\text{max}}}$</td>
</tr>
<tr>
<td>Note:</td>
<td>$T_1 = T_2 = t_{cyc}$</td>
</tr>
<tr>
<td>$t_{OE}$</td>
<td>$PB_5 + PB_2 + PB_3$</td>
</tr>
<tr>
<td>$PB_5$</td>
<td>$T_1 - t_{RSD_{\text{max}}}$</td>
</tr>
<tr>
<td>$PB_2$</td>
<td>$t_{cyc} \times Tw_2$</td>
</tr>
<tr>
<td>$PB_3$</td>
<td>$T_2B - t_{RSD_{3\text{max}}}$</td>
</tr>
<tr>
<td>Note:</td>
<td>$T_1 = T_2 = t_{cyc}$</td>
</tr>
<tr>
<td>$t_{PACC}$</td>
<td>$PB_6 + PB_7 + PB_8$</td>
</tr>
<tr>
<td>$PB_6$</td>
<td>$T_2B - t_{AD2_{\text{max}}}$</td>
</tr>
<tr>
<td>$PB_7$</td>
<td>$t_{cyc} \times Tw_2$</td>
</tr>
<tr>
<td>$PB_8$</td>
<td>$T_2B - t_{RDS_{3\text{max}}}$</td>
</tr>
<tr>
<td>Note:</td>
<td>$T_1 = T_2 = T_2B = Tw_b = t_{cyc}$</td>
</tr>
</tbody>
</table>
Figure 13 shows write timing for NOR flash memory (4).
Figure 14 shows write timing for NOR flash memory (5).

Figure 14 Write Timing of NOR Flash Memory When W = 1 (5)
Figure 15 shows write timing for NOR flash memory (6).

![Write Timing of NOR Flash Memory When W = 1 and Taw = 1](image)

**Figure 15  Write Timing of NOR Flash Memory When W = 1 and Taw = 1 (6)**
Figure 16 shows page read timing for NOR flash memory (2).
3. Documents for Reference

- Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manuals
  SH7263 Group Hardware Manual
  SH7203 Group Hardware Manual
  The most up-to-date versions of the documents are available on the Renesas Technology Website.
Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jun.18.08</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

All trademarks and registered trademarks are the property of their respective owners.
Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.

2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.

3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.

4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)

5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.

6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.

7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems where the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.

8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.

9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.

10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.

12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.

13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.

© 2008. Renesas Technology Corp., all rights reserved.