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Renesas Electronics Corporation

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M16C/62P Group

Example Application for Timer Pulse Output when Timer A is Insufficient

1. Abstract

This document describes the procedure and example usage for performing timer output using timer B and DMAC when timer A is insufficient to produce the timer output.

2. Introduction

The explanation of this issue is applied to the following condition:

Applicable MCU: M16C/62P Group

This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/62P microcomputers. However, some functions may have been modified.

Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Explain of Example Usage

The following shows an example of how to use timer B and the DMAC in the M16C/62P group to produce timer pulse output.

Specification:

- System
 XIN=16MHz, VCC1=VCC2=5V
- DMAC
 DMA request factor=TB0 interrupt request, transfer mode=repeat transfer, transfer unit=8 bit, source address direction=forward (pulse output data), destination address direction=fix (port P0)
- TB0
 timer mode, count source=f1, timer period=1ms (timer value=16000-1)

Operation:

The output level of P0_0 functioning as an output port in DMA transfer is changed each time timer B0 underflows in 1 ms cycle. Figure 1 shows timing chart.

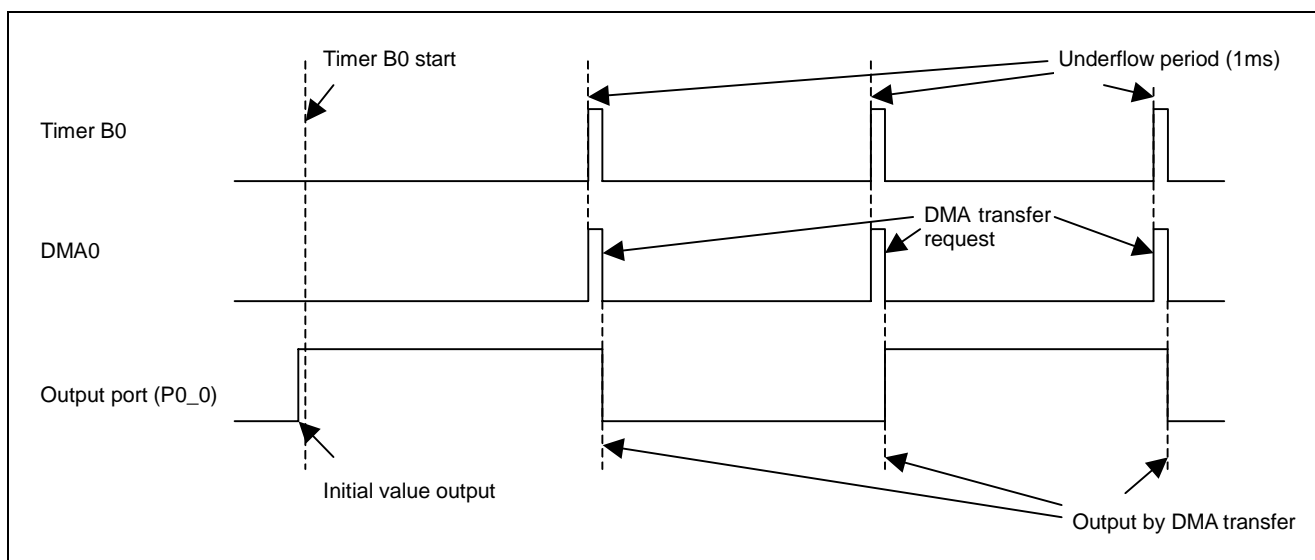
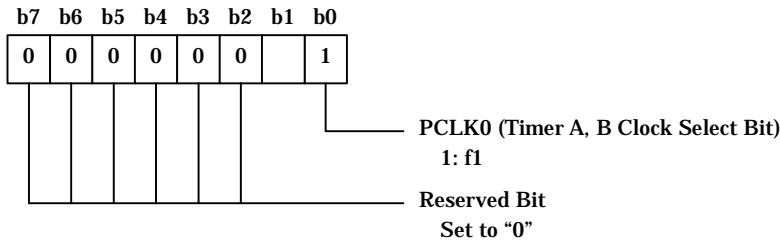


Figure 1. Pulse Output Timing Chart

Note that for reasons of SFR bit assignments, operation in this sample program may involve manipulating some bits whose functions are unused. Make sure the values of these bits are set according to the working condition in the user system.

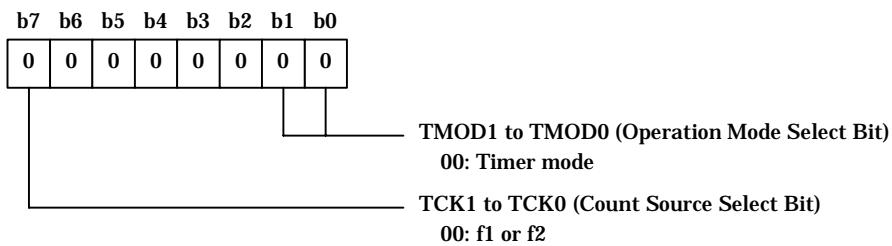
(1) Timer B0 Setting

- Select f1 for the timer A and B clocks using the PCLKR register (peripheral clock select register). Note 1

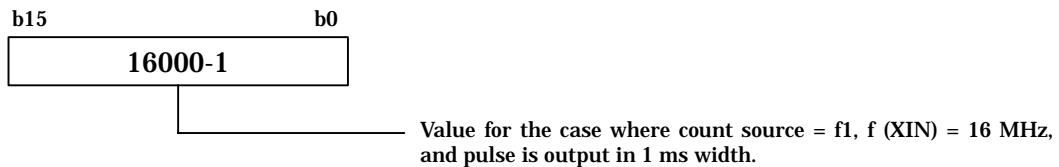


Note 1: Write to this register after setting the PRC0 bit in the PRCR register to "1" (write enable).

- Set up the TB0MR register (timer B0 mode register).

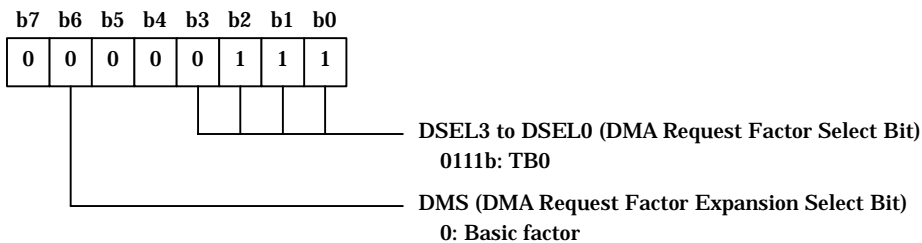


- Set a timer value (pulse output width) in the TB0 register (timer B0 register).

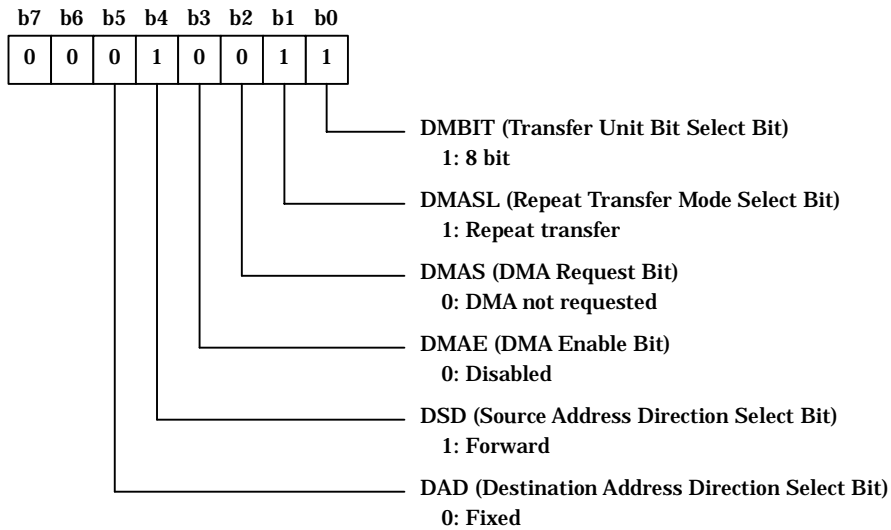


(2) DMAC Setting

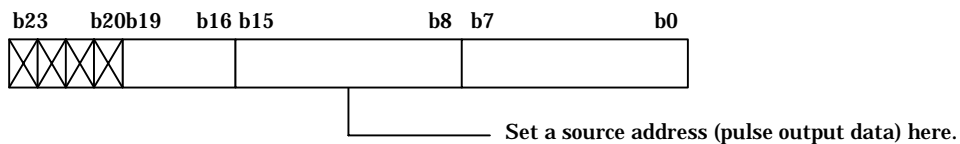
- Set up the DM0SL register (DMA0 request factor select register).



•Set up the DM0CON register (DMA0 control register)



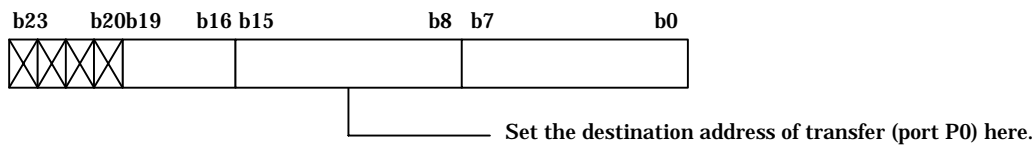
•Set up the SAR0 register (DMA0 source pointer).



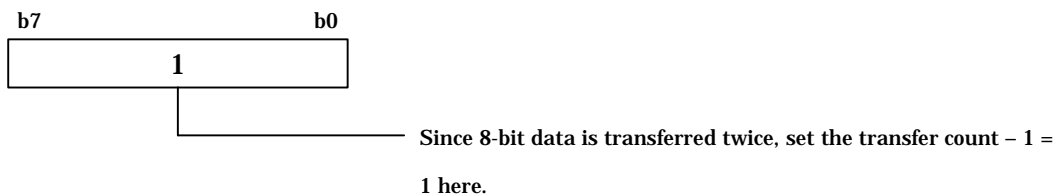
Set the data for pulse output as shown below.

- If initial output = low
char pulse_data[2] = {0x00, 0x01};
- If initial output = high
char pulse_data[2] = {0x01, 0x00};

•Set up the DAR0 register (DMA0 destination pointer)

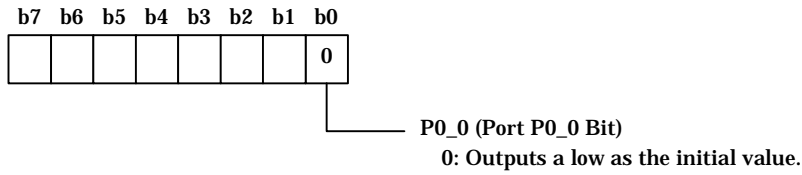


•Set up the TCR0 register (DMA0 transfer counter)

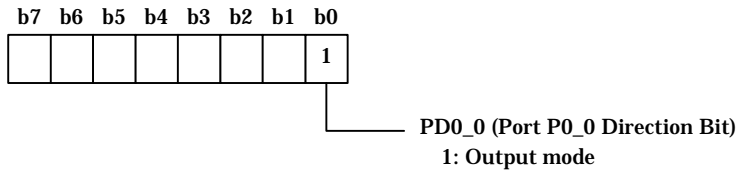


(3) Set the port P0_0 as an output port for pulse output.

- Set up the P0 register (port P0 register)

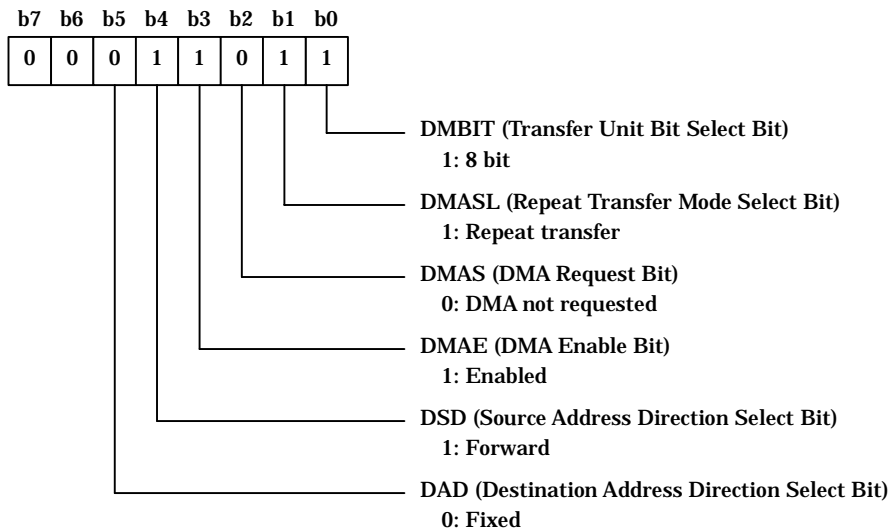


- Set up the PD0 register (port P0 direction register)



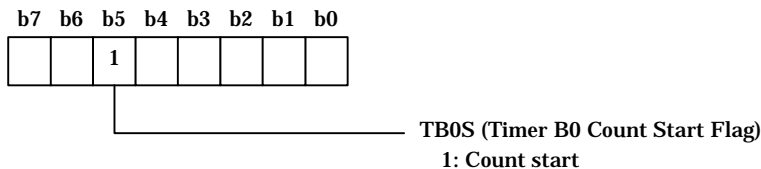
(4) DMA Enable

Set up the DM0CON register (DMA0 control register) newly again (to enable DMA).



(5) Timer B0 Start

Set the TB0S bit in the TABSR register to "1" (to let the timer start counting).



3.1 Precaution

When using timer B and the DMAC in combination to produce timer pulse output, pay attention to the following.

(1) Limitations Due to DMAC Specifications

For reasons of DMAC specifications, the following limitations apply.

- If a DMA request occurs in other interrupt sequence processing, DMA transfer is kept waiting.
- If DMA0 and DMA1 requests occur at the same time, DMA0 is serviced first because it has higher priority and DMA1 is kept waiting.

Therefore, the procedure presented here cannot be used for short-cycle, high-accuracy applications. For such applications, we recommend using timer A preferentially over the other timer.

(2) Pulse Output Delay

- Delay time at start of timer B

For pulse output produced first at start of timer B, the instruction execution time from when the port direction register is set for output to when timer B is made to start constitutes a delay time.

- Delay Time Due to DMA Transfer

Pulse output actually is produced a finite time after a timer B interrupt request occurred, which is equal to the DMA setup time + number of DMA transfer cycles (see paragraph (3) in 3.2). This delay time can be adjusted by adjusting the timer value.

Figure 2 shows an example of pulse output delay when the same timer value is set in timers A and B.

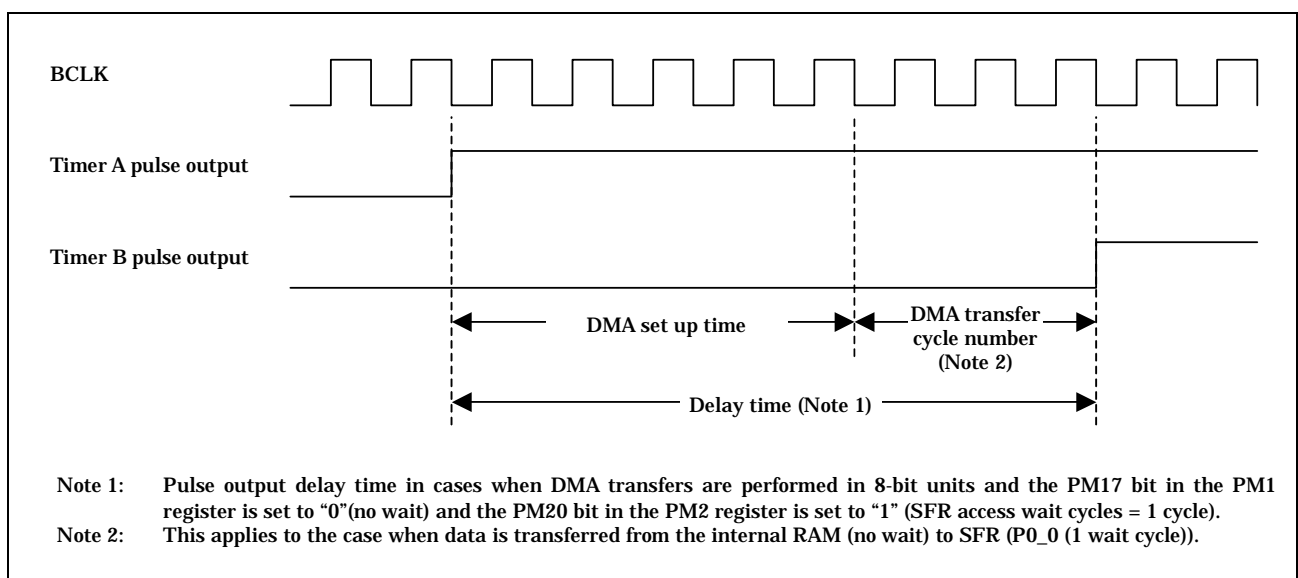


Figure 2.Pulse Output Delay Example

(3) DMA Transfer Cycles

The number of DMAC transfer cycles can be calculated as follows:

Table 1 shows the number of DMA transfer cycles. Table 2 shows the Coefficient j, k.

$$\text{No. of transfer cycles per transfer unit} = \text{No. of read cycles} \times j + \text{No. of write cycles} \times k$$

Table 1. DMA Transfer Cycles

Transfer Unit	Bus Width	Access Address	Single-Chip Mode		Memory Expansion Mode Microprocessor Mode	
			No. of Read Cycles	No. of Write Cycles	No. of Read Cycles	No. of Write Cycles
8-bit Transfers	16-bit	Even	1	1	1	1
		Odd	1	1	1	1
	8-bit	Even	-	-	1	1
		Odd	-	-	1	1
16-bit Transfers	16-bit	Even	1	1	1	1
		Odd	2	2	2	2
	8-bit	Even	-	-	2	2
		Odd	-	-	2	2

Table 2. Coefficient j, k

	Internal Area				External Area						
	Internal ROM, RAM		SFR		Separate Bus			Multiplex Bus			
	No Wait	With Wait	1-Wait (Note 1)	2-Wait (Note 2)	No Wait	With Wait (Note 1)			With Wait (Note 1)		
						1 Wait	2 Waits	3 Waits	1 Wait	2 Waits	3 Waits
j	1	2	2	3	1	2	3	4	3	3	4
k	1	2	2	3	2	2	3	4	3	3	4

NOTES:

1. Depends on the set value of CSE register.
2. Depends on the set value of PM20 bit in the PM2 register.

(4) Limitations on Output Port

Since DMA transfers are performed in 8-bit units, no other pins (P0_1 to P0_7), except P0_0 used for timer pulse output, can be used as output ports.

4. Reference

Renesas Technology Corporation Home Page

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Hardware Manual

M16C/62P Group Hardware Manual Rev.2.30

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6. Sample Programming Code

The following shows a program example of how to use timer B0 and DMA0 to produce the timer output in 1 ms cycle.

Operating Conditions: XIN=16MHz, VCC1=VCC2=5V

```

/*****/
/*
/* M16C/62 Group Program Collection
/*
/* FILE NAME : rjj05b0544_src.c
/* CPU : M16C/62P Group
/* FUNCTION : This program is a sample program which uses Timer-B
/* and DMA and performs a timer pulse output,
/* when Timer-A run short.
/*
/* HISTORY : 2004.04.01 Ver 1.00
/*
/* Copyright (C) 2004. Renesas Technology Corp.
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/* All right reserved.
/*
/*****/

/*****/
/* include file
/*****/
#include "sfr62p.h" // Special Function Register Header File

/*****/
/* Global variable declaration
/*****/
// Timer Pulse Output data.
char pulse_data[2] = {0x01, 0x00};

/*****/
/* Main Program
/*****/
void main(void)
{

    prc0 = 1;
    cml = 0x20; // Set system clock no-divid mode.
    cm0 = 0x08;
    prc0 = 0;

    prcl = 1;
    pml = 0x08; // Set internal-ROM/RAM no-wait.
    prcl = 0;

    prc0 = 1;
    pclkr = 0x03; // Set PCLKR register.
                // <PCLK0> : TA/TB clock = f1
                // <PCLK1> : SI/O clock = f1

    prc0 = 0;

    tb0mr = 0x00; // Set TB0MR register.
                // <TMOD1-0> : Timer mode
                // <TCK1-0> : Count source = f1

    tb0 = 16000-1; // Set TB0 register.
                // Pulse output cycle=1ms(XIN=16MHz)

    dm0sl = 0x07; // Set DM0SL register.

```

```

// <DSEL3-0> : TB0 interrupt request
// <DMS>      : Basic cause

dm0con = 0x13;          // Set DM0CON register.
// <DMBIT> : 8bit
// <DMASL> : Repeat transfer
// <DMAE>  : DMA disable
// <DSD>   : Src  address direction=Forward
// <DAD>   : Dest address direction=Fix

// Set DMA0 Source pointer address.
sar0_addr.byte.low  = (char>(&pulse_data[0]));
sar0_addr.byte.mid  = (char)((unsigned long>(&pulse_data[0]) >> 8));
sar0_addr.byte.high = (char)((unsigned long>(&pulse_data[0]) >> 16));

// Set DMA0 Destination pointer address.
dar0_addr.byte.low  = (char>(&p0);
dar0_addr.byte.mid  = (char)((unsigned long>(&p0) >> 8));
dar0_addr.byte.high = (char)((unsigned long>(&p0) >> 16));

// Set DMA0 transfer counter.
// 2-byte transfer.
tcr0 = 1;

p0 = 0x00;
pd0 = 0x01;          // P0_0 is chosen as a pulse output terminal.

dm0con = 0x1b;      // Set DM0CON register.
// <DMAE> : DMA enable

tb0s = 1;          // TB0 start.

while(1);
}

```

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	2005.01.14	-	First edition issued

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