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Renesas Electronics Corporation

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H8/300H Tiny Series

Entering Subsleep Mode

Introduction
Subsleep mode is entered.

Target Device
H8/3664

Contents

1. Specifications .................................................................................................................. 2
2. Description of Functions Used ........................................................................................ 2
3. Description of Operations .............................................................................................. 4
4. Description of Software .................................................................................................. 5
5. Flowcharts .................................................................................................................... 8
6. Program Listing ............................................................................................................. 10
1. Specifications

- **Subsleep mode is entered.**
- **This LSI goes directly from active mode to subactive mode when a SLEEP instruction is executed while the SSBY bit is set to X (either 1 or 0) in SYSCR1, the LSON and DTON bits are set to 1 and the SMSEL bit is set to X (either 1 or 0) in SYSCR2.**
- **This LSI goes from subactive mode to subsleep mode when a SLEEP instruction is executed while the SSBY bit is cleared to 0 in SYSCR1, the DTON bit is cleared to 0, and the SMSEL and LSON bits are set to 1 in SYSCR2.**
- **Subsleep mode is canceled and this LSI returns to subactive mode on receiving a timer A interrupt.**
- **Timer A interrupt handling controls the LED and counts the number of times a timer A interrupt has been requested. A timer A interrupt occurs every 0.5 s. After a timer A interrupt has been requested for the 120th time, timer A interrupt requests are disabled, and execution stops. The LED is turned on and off every 0.5 s.**
- **After transiting to subactive mode because a timer A interrupt has occurred, the number of times a timer A interrupt has been requested is counted, and the LSI then reenters subsleep mode. This processing is repeated until a timer A interrupt has occurred 120 times.**
- **The LED is connected to the P74 output pin of port 7.**

2. Description of Functions Used

In this sample task, this LSI enters subsleep mode, a power-down mode. Figure 1 shows a diagram of transition to subsleep mode. The subsleep mode functions are described below.

- **This LSI transits directly from active mode to subactive mode when a SLEEP instruction is executed while the SSBY bit is set to X (either 1 or 0) in SYSCR1, the LSON and DTON bits are set to 1 and the SMSEL bit is set to X (either 1 or 0) in SYSCR2. Then when a SLEEP instruction is executed while the SSBY bit is cleared to 0 in SYSCR1, the DTON bit is cleared to 0, and the SMSEL and LSON bits are set to 1 in SYSCR2, this LSI goes from subactive mode to subsleep mode.**
- **In subsleep mode, operation of the on-chip peripheral modules other than timer A, timer V, the watchdog timer, and the I2C bus interface is halted.**
- **As long as the rated voltage is supplied, the contents of the CPU registers, on-chip RAM, and some on-chip peripheral module registers are retained. The I/O ports keep the same states as before the transition.**
- **Subsleep mode is cleared by a timer A, IRQ3 to IRQ0, or WKP5 to WKP0 interrupt, or by input at the RES pin.**
- **In the case of clearing subsleep mode with an interrupt, when an interrupt is requested, subsleep mode is cleared and interrupt handling starts.**
- **Subsleep mode is not cleared if the I bit in the condition code register (CCR) is set to 1 or the requested interrupt is disabled in the corresponding interrupt enable register.**
- **In using the RES pin to initiate the transition from subsleep mode, the IC enters the reset state and cancels subsleep mode when a low level is placed on the RES pin. Once the pulse generator output has become stable, the RES pin is driven high, after which the CPU starts reset exception handling. Since system clock signals are supplied to the entire LSI as soon as the system clock pulse generator starts functioning, the RES pin must be kept low until the pulse generator output is stable.**
- **In this sample task, subsleep mode is cleared by a timer A interrupt. After exit from subsleep mode, a transition is made to subactive mode.**
- **If a SLEEP instruction is executed while the SSBY bit is set to X (either 1 or 0) in SYSCR1, and the SMSEL bit is set to X (either 1 or 0), the LSON bit is cleared to 0, and the DTON bit is set to 1 in SYSCR2 in subactive mode, a direct transition is made to active mode after the waiting time set in the STS2 to STS0 bits in SYSCR1 has elapsed.**
- **The oscillation stabilization waiting time after exit from subactive mode is set by the STS2 to STS0 bits in SYSCR1.**
- **In this sample task, the operating frequency is 16 MHz, and the waiting time is 131,072 states (oscillation stabilization waiting time: 8.2 ms).**
Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated for a transition to subsleep mode.

### Table 1 Function Allocation

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSCR1</td>
<td>Controls power-down mode</td>
</tr>
<tr>
<td>SYSCR2</td>
<td>Controls power-down mode</td>
</tr>
<tr>
<td>PCR7</td>
<td>Sets P74 output pin function</td>
</tr>
<tr>
<td>PDR7</td>
<td>Stores P74 output pin data</td>
</tr>
<tr>
<td>P74</td>
<td>LED output pin</td>
</tr>
<tr>
<td>TMA</td>
<td>Selects the clock time-base function for timer A and sets the TCA overflow cycle</td>
</tr>
<tr>
<td>TCA</td>
<td>8-bit up-counter that overflows every 0.5 s by the clock time-base function</td>
</tr>
<tr>
<td>IRRTA</td>
<td>Indicates whether or not a timer A interrupt request is issued</td>
</tr>
<tr>
<td>IENTTA</td>
<td>Enables timer A interrupt requests</td>
</tr>
</tbody>
</table>
3. Description of Operations

Figure 2 shows this sample task’s principle of operation. The hardware and software processing shown in figure 2 performs a transition to subsleep mode.

![Diagram showing the transition to subsleep mode](image)

**Figure 2  Operation Principle: Transition to Subsleep Mode**
4. Description of Software

4.1 Description of Modules

Table 2 describes the software used in this sample task.

**Table 2 Description of Modules**

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Sets timer A interrupts, port 7, and counter_a, enables interrupts,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>transits to subactive mode, subsleep mode, and active mode.</td>
</tr>
<tr>
<td>LED control</td>
<td>taint</td>
<td>During the timer A interrupt handling routine, controls the LED,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>decrements the 8-bit counter that counts timer A interrupts, and</td>
</tr>
<tr>
<td></td>
<td></td>
<td>disables timer A interrupt requests after 60 s.</td>
</tr>
<tr>
<td>Direct transition</td>
<td>dtint</td>
<td>During the direct transition interrupt handling routine, clears the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>direct transition interrupt request flag.</td>
</tr>
</tbody>
</table>

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 3 describes the internal registers used in this sample task.

**Table 3 Description of Internal Registers**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMA</td>
<td>Timer mode register A: When TMA is set to H'19, timer A is set to the</td>
<td>H'FFA6</td>
<td>H'19</td>
</tr>
<tr>
<td></td>
<td>clock time-base function, and the TCA overflow cycle is set to 0.5 s.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCA</td>
<td>Timer counter A: 8-bit counter that overflows every 0.5 s by clock</td>
<td>H'FFA7</td>
<td>H'00</td>
</tr>
<tr>
<td></td>
<td>time-base and has clock input of PSW output clock</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDR7 P74</td>
<td>Port data register 7 (port data register 74): When P74 is cleared to 0,</td>
<td>H'FFDA</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>the P74 pin output level is low. Bit 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When P74 is set to 1, the P74 pin output level is high.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCR7 PCR74</td>
<td>Port control register 7 (port control register 74): When PCR74 is</td>
<td>H'FFEA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>set to 1, the P74 pin functions as an output pin.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 4</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
### Table 4 Description of Internal Registers (cont)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSCR1 SSBY</td>
<td>System control register 1 (software standby): When SSBY is set to X</td>
<td>H'FFF0</td>
<td>Bit 7</td>
</tr>
<tr>
<td></td>
<td>(either 1 or 0), after execution of a SLEEP instruction, a direct</td>
<td></td>
<td>1 (in this sample</td>
</tr>
<tr>
<td></td>
<td>transition is made to subactive mode or active mode.</td>
<td></td>
<td>task)</td>
</tr>
<tr>
<td>STS2</td>
<td>System control register 1 (standby timer select 2 to 0):</td>
<td>H'FFF0</td>
<td>Bit 6</td>
</tr>
<tr>
<td></td>
<td>When STS2 is set to 1 and STS1 and STS0 are both cleared to 0, the</td>
<td></td>
<td>STS2 = 1</td>
</tr>
<tr>
<td></td>
<td>wait time is set to 131.072 states.</td>
<td></td>
<td>Bit 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>STS1 = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Bit 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>STS0 = 0</td>
</tr>
<tr>
<td>SYSCR2 SMSEL</td>
<td>System control register 2 (sleep mode selection): When SMSEL is cleared</td>
<td>H'FFF1</td>
<td>Bit 7</td>
</tr>
<tr>
<td></td>
<td>to 0, after execution of a SLEEP instruction, a transition is made to</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LSON</td>
<td>System control register 2 (low speed on flag): When LSON is set to</td>
<td>H'FFF1</td>
<td>Bit 6</td>
</tr>
<tr>
<td></td>
<td>1, sleep mode, subsleep mode, or subactive mode (direct transition)</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>is selected as the mode to transit to after execution of a SLEEP</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>instruction.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DTON</td>
<td>System control register 2 (direct transfer on flag): When DTON is set</td>
<td>H'FFF1</td>
<td>Bit 5</td>
</tr>
<tr>
<td></td>
<td>to 1, active mode or subactive mode is selected as the mode to transit</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>to after execution of a SLEEP instruction.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MA2</td>
<td>System control register 2 (active mode clock select 2 to 0:)</td>
<td>H'FFF1</td>
<td>Bit 4</td>
</tr>
<tr>
<td></td>
<td>When MA2, MA1, and MA0 are all set to 1, φOSC/64 is selected as the</td>
<td></td>
<td>MA2 = 1</td>
</tr>
<tr>
<td></td>
<td>clock in active mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MA1</td>
<td></td>
<td>Bit 3</td>
<td>MA1 = 1</td>
</tr>
<tr>
<td>MA0</td>
<td></td>
<td>Bit 2</td>
<td>MA0 = 1</td>
</tr>
<tr>
<td>SA1</td>
<td>System control register 2 (subactive mode clock select 1 and 0:)</td>
<td>H'FFF1</td>
<td>Bit 1</td>
</tr>
<tr>
<td></td>
<td>When SA1 and SA0 are both cleared to 0, φw/8 is selected as the CPU</td>
<td></td>
<td>SA1 = 0</td>
</tr>
<tr>
<td></td>
<td>operating clock in subactive mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SA0</td>
<td></td>
<td>Bit 0</td>
<td>SA0 = 0</td>
</tr>
<tr>
<td>IENR1 IENDT</td>
<td>Interrupt enable register 1 (direct transition interrupt enable):</td>
<td>H'FFF4</td>
<td>Bit 7</td>
</tr>
<tr>
<td></td>
<td>When IENDT is cleared to 0, direct transition interrupt requests are</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IENDT is set to 1, direct transition interrupt requests are</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>enabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IENTA</td>
<td>Interrupt enable register 1 (timer A interrupt enable):</td>
<td>H'FFF4</td>
<td>Bit 6</td>
</tr>
<tr>
<td></td>
<td>When IENTA is cleared to 0, timer A interrupt requests are</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IENTA is set to 1, timer A interrupt requests are</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>enabled.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 4 Description of Internal Registers (cont)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address Setting</th>
</tr>
</thead>
</table>
| IRR1          | IRRDT Interrupt request register 1 (direct transition interrupt request flag):  
When IRRDT is cleared to 0, no direct transition interrupt is requested.  
When IRRDT is set to 1, a direct transition interrupt is requested. | H'FFF6  
Bit 7  
0 |
| IRRTA         | Interrupt request register 1 (timer A interrupt request flag):  
When IRRTA is cleared to 0, no timer A interrupt is requested.  
When IRRTA is set to 1, a timer A interrupt is requested. | H'FFF6  
Bit 6  
0 |

### 4.4 Description of RAM

Table 5 describes the RAM used in this sample task.

### Table 5 Description of RAM

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function</th>
<th>Address Setting</th>
</tr>
</thead>
</table>
| counter_a  | Down-counter for counting the number of timer A interrupts | H'FB80  
Main routine |
| USRF       | END Flag for judging whether or not 60 s has elapsed | H'FB81  
Bit 2  
Main routine |
| ITCNF      | Flag for judging whether or not the timer A interrupt count is even or odd | H'FB81  
Bit 1  
LED control |
| LDONF      | Flag for judging on/off of the LED | H'FB81  
Bit 0  
LED control |
5. Flowcharts

Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 3  Flowchart for Main Routine
LED control

Clear IRRTA to 0

LDONF = 1?

Yes

Set P74 in PDR7 to 1
Clear P74 in PDR7 to 0
Set LDONF in USRF to 1
Clear LDONF in USRF to 0

No

IACTF = 1?

Yes

Decrement counter_a

counter_a = H'00?

No

Invert IACTF

Yes

Clear IENTA to 0 to disable timer A interrupts
Clear ENDF to 0

Interrupt handling

end

Figure 4  Flowchart for Timer A Interrupt Handling Routine

Direct transition

Clear IRRDT to 0

Interrupt handling

end

Figure 5  Flowchart for Direct Transition Interrupt Handling Routine
6. Program Listing

INIT.SRC (Program listing)

```assembly
.EXPORT _INIT
.IMPORT _main

; .SECTION P, CODE
_INIT:
    MOV.W #H'FF80, R7
    LDC.B #B'10000000, CCR
    JMP @_main

; _END
```

```c
#include <machine.h>
```

/****************************************************************************/
/*                                                                     */
/*    H8/300H Tiny Series -H8/3664-                                   */
/*    Application Note                                               */
/*                                                                     */
/*    'Transition to Subsleep Mode'                                    */
/*                                                                     */
/*    Function                                                       */
/*    : Power-Down Mode                                               */
/*    Subsleep Mode                                                   */
/*                                                                     */
/*    External Clock : 16MHz                                          */
/*    Internal Clock : 16MHz                                         */
/*    Sub Clock : 32.768kHz                                            */
/*                                                                     */
/**************************************************************************/
/********************************************************/
/* Symbol Definition                                       */
/********************************************************/

struct BIT {
    unsigned char b7:1;  /* bit7 */
    unsigned char b6:1;  /* bit6 */
    unsigned char b5:1;  /* bit5 */
    unsigned char b4:1;  /* bit4 */
    unsigned char b3:1;  /* bit3 */
    unsigned char b2:1;  /* bit2 */
    unsigned char b1:1;  /* bit1 */
    unsigned char b0:1;  /* bit0 */
};
#define TMA        *(volatile unsigned char *)0xFFA6 /* Timer Mode Register A */
#define TCA        *(volatile unsigned char *)0xFFA7 /* Timer Counter A */
#define PDR7_BIT   (*(struct BIT *)0xFFDA)           /* Port Data Register 7 */
#define P74        PDR7_BIT.b4                       /* Port Data Register 7 bit4 */
#define PCR7_BIT   (*(struct BIT *)0xFFEA)           /* Port Control Register 7 */
#define PCR74      PCR7_BIT.b4                       /* Port Control Register 7 bit4 */
#define SYSCR1     *(volatile unsigned char *)0xFFF0 /* System Control Register 1 */
#define SYSCR1_BIT (*(struct BIT *)0xFFF0)           /* System Control Register 1 */
#define SSBY       SYSCR1_BIT.b7                     /* Software Standby */
#define STS2       SYSCR1_BIT.b6                     /* Standby Timer Select 2 */
#define STS1       SYSCR1_BIT.b5                     /* Standby Timer Select 1 */
#define STS0       SYSCR1_BIT.b4                     /* Standby Timer Select 0 */
#define NESEL      SYSCR1_BIT.b3                     /* Noise Elimination Sampling Frequency Select */
#define SYSCR2     *(volatile unsigned char *)0xFFF1 /* System Control Register 2 */
#define SYSCR2_BIT (*(struct BIT *)0xFFF1)           /* System Control Register 2 */
#define LSON       SYSCR2_BIT.b6                     /* Low Speed On Flag */
#define DTON       SYSCR2_BIT.b5                     /* Direct Transfer On Flag */
#define MA1        SYSCR2_BIT.b3                     /* Active Mode Clock Select 1 */
#define MA0        SYSCR2_BIT.b2                     /* Active Mode Clock Select 0 */
#define SA1        SYSCR2_BIT.b1                     /* Subactive Mode Clock Select 1 */
#define SA0        SYSCR2_BIT.b0                     /* Subactive Mode Clock Select 0 */
#define IENR1_BIT  (*(struct BIT *)0xFFF4)           /* Interrupt Enable Register 1 */
#define IENDT      IENR1_BIT.b7                     /* Direct Transfer Interrupt Enable */
#define IENTA      IENR1_BIT.b6                     /* Timer A Interrupt Enable */
#define IRR1_BIT   (*(struct BIT *)0xFFF6)           /* Interrupt Request Register 1 */
#define IRRDT      IRR1_BIT.b7                       /* Direct Transfer Interrupt Request Flag */
#define IRRTA      IRR1_BIT.b6                       /* Timer A Interrupt Request Flag */

#pragma interrupt (dtint)
#pragma interrupt (taint)
/******************************************************************/
/*     Function Definition                                       */
/******************************************************************/
extern    void    INIT ( void );                       /* SP Set                          */
void      main     ( void );
void      dtint    ( void );
void      taint    ( void );
void      sleep    ( void );

/******************************************************************/
/*     RAM define                                               */
/******************************************************************/
unsigned char    counter_a;
unsigned char    USRF;                              /* User Flag Erea                 */
#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        ENDF        USRF_BIT.b2                  /* End Flag                       */
#define        IACTF        USRF_BIT.b1                 /* Timer A Interrupt Counter Flag */
#define        LDONF        USRF_BIT.b0                  /* LED On Flag                    */

/******************************************************************/
/*     Vector Address                                           */
/******************************************************************/
#pragma    section        V1                            /* VECTOR SECTOIN SET             */
void (*const VEC_TBL1[])(void) = {
    INIT                                                /* 00 Reset                       */
};
#pragma    section        V2                            /* VECTOR SECTOIN SET             */
void (*const VEC_TBL2[])(void) = {
    dtint                                               /* Direct Transfer  Interrupt     */
};
#pragma    section        V3                            /* VECTOR SECTOIN SET             */
void (*const VEC_TBL3[])(void) = {
    taint                                               /* timer A  Interrupt             */
};
#pragma    section                                      /* P                              */
/****************************************************************
/*    Main Program                                      */
****************************************************************/

void    main ( void )
{
    set_imask_ccr(1);          /* Interrupt Disable                     */
    TMA = 0x19;                /* Initialize Timer A Function           */
    IRRTA = 0;                 /* Clear IRRTA                            */
    IENTA = 1;                 /* Timer A Interrupt Enable              */
    IRRDT = 0;                 /* Clear IRRDT                            */
    IENDT = 1;                 /* Direct Transfer Interrupt Enable       */
    SYSCR1 = 0xB0;             /* Initialize Function of Subactive Mode 1 */
    SYSCR2 = 0x7C;             /* Initialize Function of Subactive Mode 2 */
    P74 = 0;                   /* Initialize P74                          */
    PCR74 = 1;                 /* Initialize P74 Output Port            */
    counter_a = 0x3C;          /* Initialize 8bit Timer A Interrupt Counter */
    LDONF = 0;                 /* Initialize LDONF                       */
    IACTF = 0;                 /* Initialize IACTF                       */
    ENDF = 0;                  /* Initialize ENDF                        */
    set_imask_ccr(0);         /* Interrupt Enable                      */
    sleep();                  /* Transition to Subactive Mode          */
    SYSCR1 = 0x00;             /* Initialize Function of Subsleep Mode 1 */
    SYSCR2 = 0x5C;             /* Initialize Function of Subsleep Mode 2 */
do{
    sleep();                                        /* Transion to Subsleep Mode */
} while(ENDF != 1);                                  /* ENDF = "1"? */
SYSCR1 = 0xC0;                                      /* Initialize Function of Active Mode 1 */
SYSCR2 = 0x3C;                                      /* Initialize Function of Active Mode 2 */
sleep();                                            /* Transition to Active Mode */

while(1){
    
}

/********************************************************/
/*     Timer A Interrupt                                */
/********************************************************/
void taint ( void )
{
    IRTTA = 0;                                          /* Clear IRTTA */
    if(LDONF == 1){                                     /* LDONF = "1"? */
        P74 = 0;                                        /* Turn Off LED */
        LDONF = 0;                                      /* Clear LDONF */
    }
    else{                                             /* LDONF = "0" */
        P74 = 1;                                        /* Turn On LED */
        LDONF = 1;                                      /* Set LDONF */
    }
    if(IACTF == 1){                                     /* IACTF = "1"? */
        counter_a--;                                    /* Decrement 8bit Timer A Interrupt Counter */
        if(counter_a == 0x00){                          /* 8bit Timer A Interrupt Counter = H'00? */
            IRTTA = 0;                                  /* Timer A Interrupt Disable */
            ENDF = 1;                                    /* Set ENDF */
        }
    }
    IACTF = ~IACTF;                                     /* Invert IACTF */
}
/********************************************************/
/* Direct Transfer Interrupt */
/********************************************************/
void dtint ( void )
{
    IRRDT = 0; /* Clear IRRDT */
}

Link Address Setting:

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'0000</td>
</tr>
<tr>
<td>CV2</td>
<td>H'001A</td>
</tr>
<tr>
<td>CV3</td>
<td>H'0026</td>
</tr>
<tr>
<td>P</td>
<td>H'0100</td>
</tr>
<tr>
<td>B</td>
<td>H'FB80</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.00</td>
<td>Sep.01.06</td>
<td>All pages</td>
<td>Format has been changed from Hitachi version to Renesas version.</td>
</tr>
</tbody>
</table>
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