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R32C/100 Series

Entering Low-speed Mode

1. Abstract

This document describes and shows an example of exiting PLL mode (high-speed mode) and entering low-speed mode.

2. Introduction

The application described in this document applies to the following MCU:

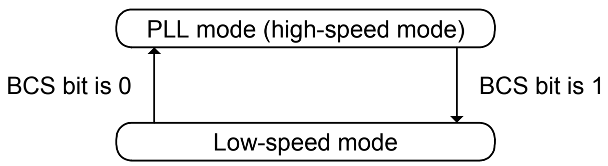
- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

The MCU exits PLL mode (high-speed mode) and enters low-speed mode by changing the BCS bit in the CCR to 1 (see the figure below).

- In PLL mode (high-speed mode), the CPU operates at the maximum operating frequency. The PLL clock divided by 2 is the base clock, and the base clock and CPU clock have the same frequency.
- In low-speed mode, a low-speed clock is used as the base clock source. A low-speed clock can be selected from the main clock divided by 256, the sub clock, and the on-chip oscillator clock divided by 4.



Note: The BCS bit is a bit in the CCR register.

Figure 3.1 Entering Low-speed Mode

4. Settings

This section describes how to exit PLL mode (high-speed mode) and enter low-speed mode.

4.1 Operating Clock

The table below shows the required clock settings.

Table 4.1 Clock Settings

Item	PLL Mode (High-speed Mode)	Low-speed Mode
Main clock (16 MHz)	Oscillating	
Sub clock (32.768 kHz)	Stopped	Oscillating
PLL clock frequency	100 MHz	
Base clock source	PLL clock divided by 2	Sub clock
Base clock frequency	50 MHz	32.768 kHz
CPU clock division ratio	No division	
Peripheral bus clock division ratio	Divided by 2	
Peripheral function clock source division ratio	Divided by 4	
On-chip oscillator	Stopped	

The block diagram for the base clock source is below. Bit settings for setting the base clock source are in Table 4.2.

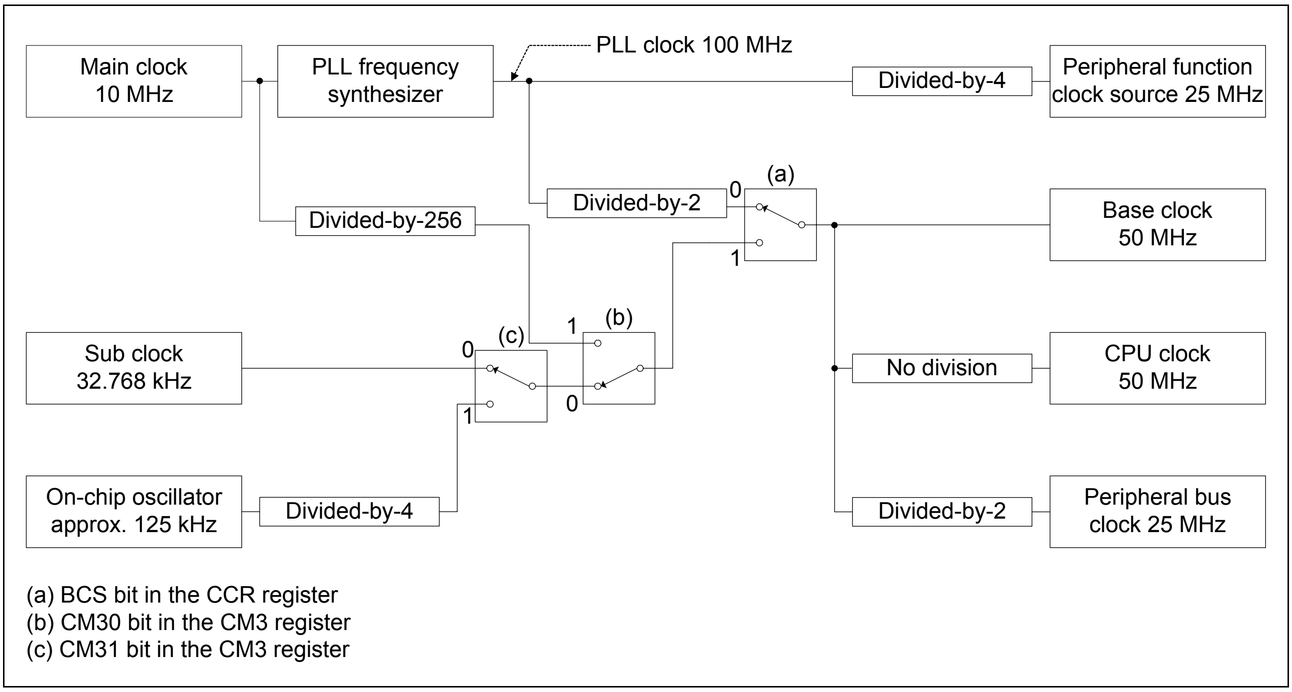


Figure 4.1 Base Clock Source Block Diagram

Table 4.2 Base Clock Source Bit Settings

Register	Bit Symbol	Value	Description
CCR	BCS	1	Select fC, fOCO4, or f256 as the base clock source
CM3	CM30	00b	Select fC as the base clock source (supplemental: fC is selected as the base clock by the low-speed mode base clock select bit)
	CM31		

4.2 Notes on Settings

(1) Rewriting the base clock select bit
When setting the BCS bit (base clock source select bit) in the CCR register to 1, rewrite addresses 0004h to 0007h in 32-bit units.

The asm function is used in this application note. When using an asm function in C, make a statement as in the following example of setting the BCS bit:

```
asm("OR.L  #00000080h,00000004h") ;
```

(2) Using the sub clock
Set the CM04 bit in the CM0 register to 1 (XCIN-XCOUT oscillate function), and wait for sub clock oscillation to stabilize before setting the CM3 register to 00h (fC), and the BCS bit in the CCR register to 1 (fC, fOCO4, or f256).

(3) Sub clock stabilization wait time
Set sub clock oscillation wait time to conform to the user board and oscillator. Below is an example of using timer A0 to measure the sub clock stabilization wait time. The timer cycle is set to 50 ms, and a 1 s wait time is measured by detecting twenty underflows. The following table shows the settings for timer A0.

Table 4.3 Timer A0 Settings

Timer	Operating Mode	Count Source Division Ratio	Count Source	f2n Division Ratio	f2n Clock Source
Timer A0	Timer mode	40000 (1)	f2n	n = 10	Main clock (16 MHz)

Note:
1. This value corresponds to a wait time of 100 ms. Use the formula below to calculate wait time.
Wait time = time for one count source × count source division ratio

$$\frac{2 \times 10}{16 \times 10^{6}} \times 40000 = 0.05 \text{ sec. } (50 \text{ ms})$$

(4) Rewriting protected registers
Registers set in this application note (PM2, CM0, CM3, and CCR) are protected by the protect register. (see table below for details)

The protect function protects important registers from being unintentionally rewritten due to a program runaway. After deasserting the protect function, protected registers can be rewritten.

Table 4.4 The Protect Register and Protected Registers

Register	Write Disabled/Enabled	Protected Registers
PRCR	PRC0 Bit 0: Write disabled 1: Write enabled	CM0 to CM2, and PM3
	PRC1 Bit 0: Write disabled 1: Write enabled	PM0, PM2, CSOP0 to CSOP2, INVC0, INVC1, IOBC and I2CMR
	PRC2 Bit 0: Write disabled 1: Write enabled	PD9, P9_iS (i = 0 to 7), PLC0, and PLC1
PRCR2	PRC27 Bit 0: Write disabled 1: Write enabled	CM3
PRCR3	PRC31 Bit 0: Write disabled 1: Write enabled	VRCR, LVDC, and DVCR
PRR	b7 to b0 Value other than AAh: Write disabled AAh: Write enabled	CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23

4.3 Overview of Settings

The figure below shows the steps for exiting PLL mode (high-speed mode) and entering low-speed mode. Refer to section **4.4 "Detailed Settings"** for detailed settings.

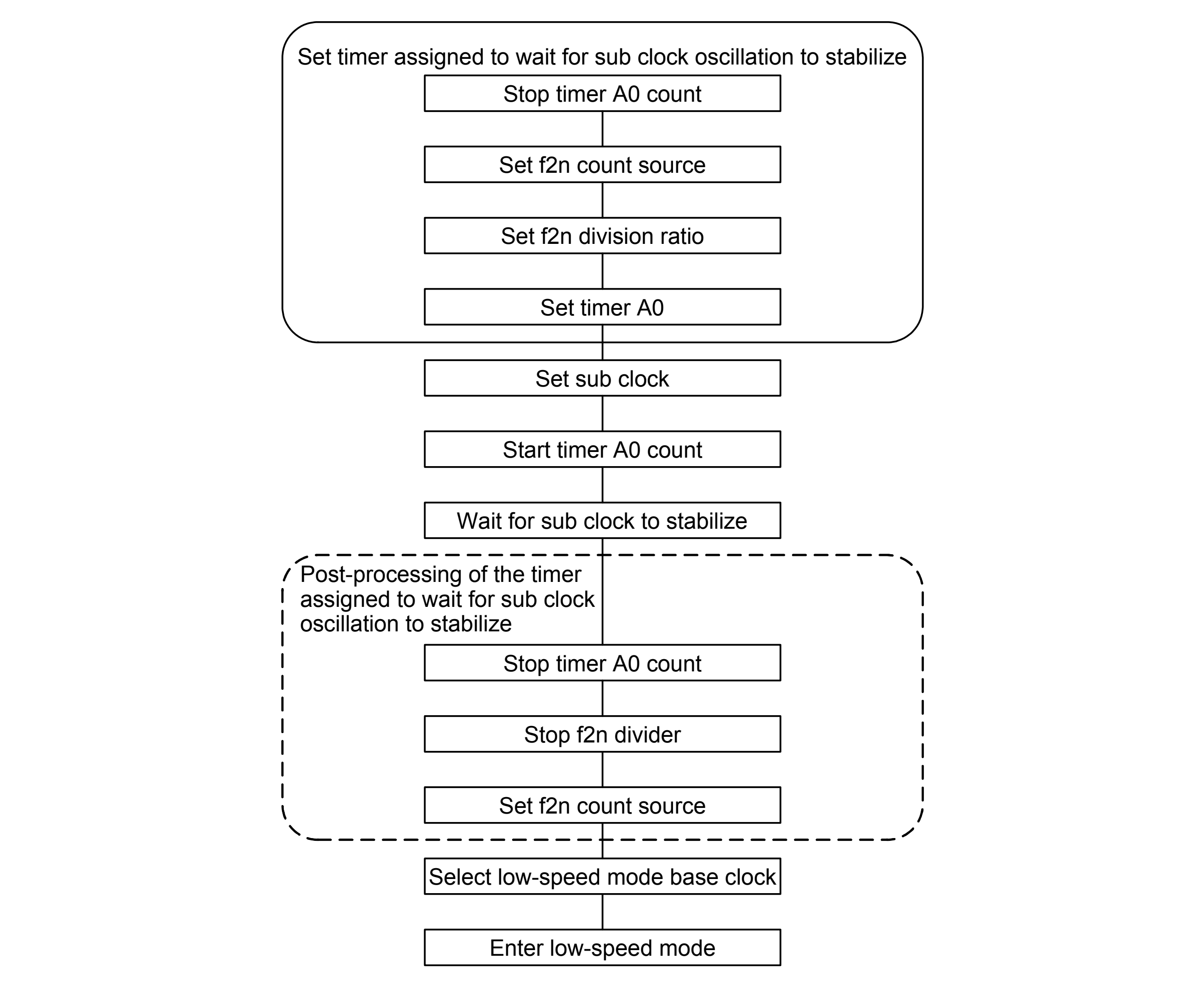


Figure 4.2 Entering Low-speed Mode from PLL Mode

4.4 Detailed Settings

(1) Stop the timer A0 count.

```
b7              b0
[ | | | | | | |0]   Count Start Register (TABSR)
```

Count Start Register (TABSR)

- TA0S — Timer A0 Count Start Bit
  - 0: Count stopped

```
b7              b0
[X|X|X|X|0| | | ]   Interrupt Control Register (TA0IC)
```

Interrupt Control Register (TA0IC)

- IR (1) — Interrupt Request Flag
  - 0: No interrupt requested

Note:
1. Set this bit to 0.

(2) Set the f2n count source.

```
b7              b0
[X|X|X|X|X| |1| ]   Protect Register (PRCR)
```

Protect Register (PRCR)

- PRC1 — Protect Bit 1
  - 1: Write enabled for registers PM0, PM2, CSOP0 to CSOP2, INVC0, INVC1, IOBC and I2CMR.

```
b7              b0
[0|1|0| |0|0| |0]   Processor Mode Register 2 (PM2)
```

Processor Mode Register 2 (PM2)

- Set to 0.
- PM26 — f2n Clock Source Select Bit
  - 1: Main clock
- Set to 0.

```
b7              b0
[X|X|X|X| | |0| ]   Protect Register (PRCR)
```

Protect Register (PRCR)

- PRC1 — Protect Bit 1
  - 0: Write disabled for registers PM0, PM2, CSOP0 to CSOP2, INVC0, INVC1, IOBC and I2CMR.

Note:
1. After setting this bit to 1 (write enabled), make sure to set it to 0 (write disabled).

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(3) Set the f2n division ratio.

b7							b0	
0	0	0	0					**Count Source Prescaler Register (TCSPR)**

- Set to 0.
- CST [1] — Divider Operation Enable Bit: 0: Divider stopped

b7							b0	
0	0	0	0	1	0	1	0	**Count Source Prescaler Register (TCSPR)**

- CNT3 to CNT0 [2] — Divide Ratio Select Bit: 1010b: Divided-by-20
- Set to 0.
- CST — Divider Operation Enable Bit: 0: Divider stopped

b7							b0	
1	0	0	0	1	0	1	0	**Count Source Prescaler Register (TCSPR)**

- CNT3 to CNT0 — Divide Ratio Select Bit: 1010b: Divided-by-20
- Set to 0.
- CST — Divider Operation Enable Bit: 1: Divider enabled

Notes:
1. Set this bit to 0 (divider stopped) before rewriting bits CNT3 to CNT0.
2. Assuming the value for these bits is n, the main clock or PLL clock divided by 2n becomes f2n. When n = 0, there is no division.

Continued on next page

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(4) Set timer A0.

b7 b0

1	0	0	0	0	0	0	0

Timer A0 Mode Register (TA0MR)

- TMOD1 to TMOD0: Operation Mode Select Bit
  00b: Timer mode
- Set to 0.
- MR2 to MR1: Gate Function Select Bit
  00b: No gate function
- MR3: Set to 0.
- TCK1 to TCK0: Count Source Select Bit
  10b: f2n

b15 b0

39999

Timer A0 Register (TA0) (1)

- Timer Mode
  39999: Divided by 40000

Notes:
1. Write to/Read this register in 16-bit units.
2. Set wait time to conform to the user board and oscillator.

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(5) Set the sub clock.

b7 b0
0 0 _ _ _ _ _ _ **Port P8 Direction Register Register (PD8)**

Bit	Setting
PD8_6	Port P8_6 Direction Bit 0: Input port
PD8_7	Port P8_7 Direction Bit 0: Input port

b7 b0
X _ 0 X X X X X **Protect Register (PRCR)**

Bit	Setting
b4 to b0	Set to 0.
PU25	P8_4 to P8_7 Pull-up Control Bit 0: No pull-up
b7	Set to 0.

b7 b0
X X X X X _ _ 1 **Protect Register (PRCR)**

Bit	Setting
PRC0	Protect Bit 0 1: Write enabled for registers CM0, CM1, CM2, and PM3

b7 b0
0 _ 0 1 1 _ _ _ **System Clock Control Register 0 (CM0)**

Bit	Setting
CM03	XCIN-XCOUT Drive Level Select Bit 1: High
CM04	Port XC Switch Bit 1: XCIN-XCOUT oscillation function
CM05	Main Clock (XIN-XCOUT) Stop Bit 1: Oscillating
Set to 0.	

b7 b0
X X X X X _ _ 0 **Protect Register (PRCR)**

Bit	Setting
PRC0 (1)	Protect Bit 0 1: Write disabled for registers CM0, CM1, CM2, and PM3

Note:
1. Set this bit to 0 (write disabled) after setting it to 1 (write enabled).

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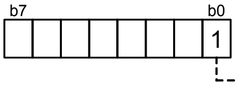
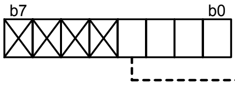
(6) Start the timer A0 count.



Count Start Register (TABSR)

TA0S — Timer A0 Count Start Bit
1: Count started

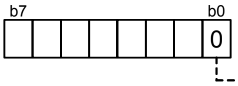
(7) Wait for sub clock oscillation to stabilize. The counter increments each time the IR bit in the TA0IC register becomes 1, until it reaches the specified value.



Timer A0 Interrupt Control Register (TA0IC)

IR — Interrupt Request Flag
0: No interrupt requested
1: Interrupt requested

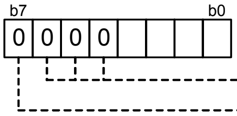
(8) Stop the timer A0 count.



Count Start Register (TABSR)

TA0S — Timer A0 Count Start Bit
0: Count stopped

(9) Stop the f2n divider.



Count Source Prescaler Register (TCSPR)

Set to 0.

CST — Divider Enable Bit
0: Divider stopped

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(10) Set the f2n count source.

b7 b0: X X X X X X 1 _ — **Protect Register (PRCR)**

- PRC1 — Protect Bit 1
  - 1: Write enabled for registers PM0, PM2, CSOP0 to CSOP2, INVC0, INVC1, IOBC and I2CMR

b7 b0: 0 0 0 _ 0 0 _ 0 — **Processor Mode Register 2 (PM2)**

- Set to 0.
- PM26 — f2n Clock Source Select Bit
  - 0: Peripheral function clock source
- Set to 0.

b7 b0: X X X X X X 0 _ — **Protect Register (PRCR)**

- PRC1 (1) — Protect Bit 1
  - 0: Write disabled for registers PM0, PM2, CSOP0 to CSOP2, INVC0, INVC1, IOBC and I2CMR

Note:
1. This bit must be set to 0 (write disabled) after setting it to 1 (write enabled).

(11) Select the low-speed mode base clock.

b7 b0: 1 X X X X X X X — **Protect Register 2 (PRCR2)**

- b6 to b0 — Set to 0.
- PRC27 — CM3 Protect Bit
  - 1: CM3 register write enabled

b7 b0: X X X X X X 0 0 — **Low-speed Mode Clock Control Register (CM3)**

- CM31 and CM30 — Low-speed Mode Base Clock Select Bit
  - 00b: fC
- b7 to b2 — Set to 0.

b7 b0: 0 X X X X X X X — **Protect Register 2 (PRCR2)**

- b6 to b0 — Set to 0.
- PRC27 (1) — CM3 Protect Bit
  - 0: CM3 register write disabled

Note:
1. This bit must be set to 0 (write disabled) after setting it to 1 (write enabled).

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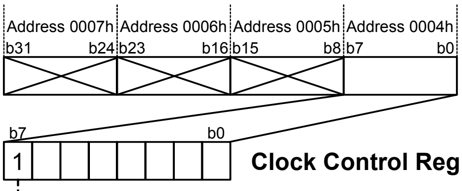
(12) Enter low-speed mode.

b7 b0
AAh

Protect Deassert Register (PRR)

Controls protection over registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23
AAh: Write enabled



Clock Control Register (CCR)

BCS — Base Clock Source Select Bit
1: fC, fOCO4, or f256

b7 b0
00h

Protect Deassert Register (PRR)

Controls protection over registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23
Value Other than AAh: Write disabled

Notes:
1. When setting this bit to 1, write to addresses 0004h to 0007h in 32-bit units.
2. After setting this register to AAh (write enabled), it must be rewritten with a value other than AAh (write disabled).

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5.1 Explanation

In the sample program, while the sub clock is oscillating, after entering slow-speed mode from PLL mode (high-speed mode), the MCU switches between PLL mode (high-speed mode) and low-speed mode in 3 sec. intervals. The program is configured to output H to the P0_7 bit in PLL mode (high-speed mode) and output L to the P0_7 bit in low-speed mode.

In the sample program, timer A0 is used to secure the wait time (1 sec.) from when the sub clock is oscillated until it becomes stabilized. Timer A1 counts the time between switching from PLL mode to low-speed mode, and is measured in 3 sec. intervals.

The table below shows the timer A0 and A1 settings in the sample program. Figure **5.1** shows an example of sample program operation.

Table 5.1 Timer A0 and A1 Settings in the Sample Program

Item	Timer A0	Timer A1
Operating mode	Timer mode	Timer mode
Count source division ratio	40000	1024
Count source	f2n (n = 10)	fC32
f2n clock source	Main clock (16 MHz)	N/A
Timer cycle	50 ms	1 sec.
Application	Used to measure the wait time until the sub clock stabilizes.	Used as the counter for counting the time between switching modes.

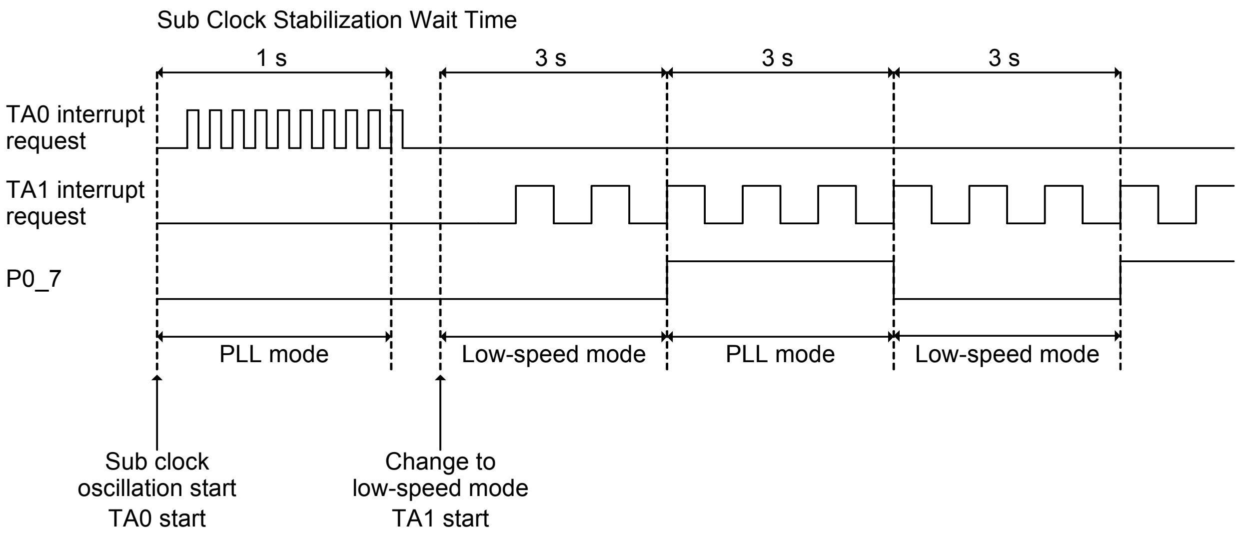
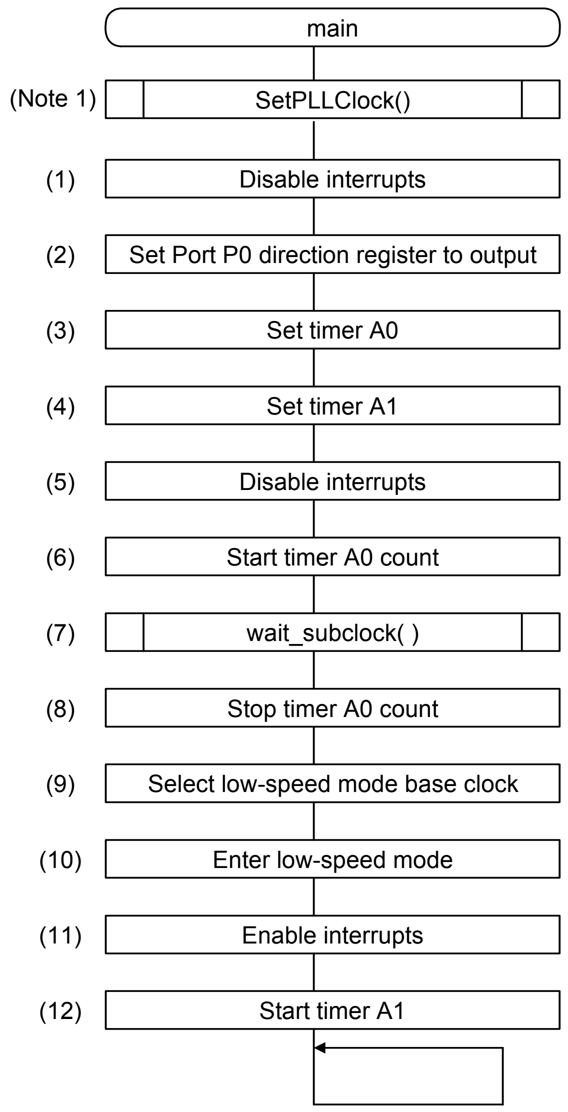


Figure 5.1 Operation of the Sample Program

5.2 Flowcharts

The sample program is comprised of a main function, a sub clock stabilization wait function, and a timer A1 interrupt function. In the following flowcharts, numbers in parenthesis ((1) to (23)) correspond to the sample program flow numbers.



Note:

1. For the SetPLLClock function setting, refer to the hardware manual.

Figure 5.2 Main Function Flowchart

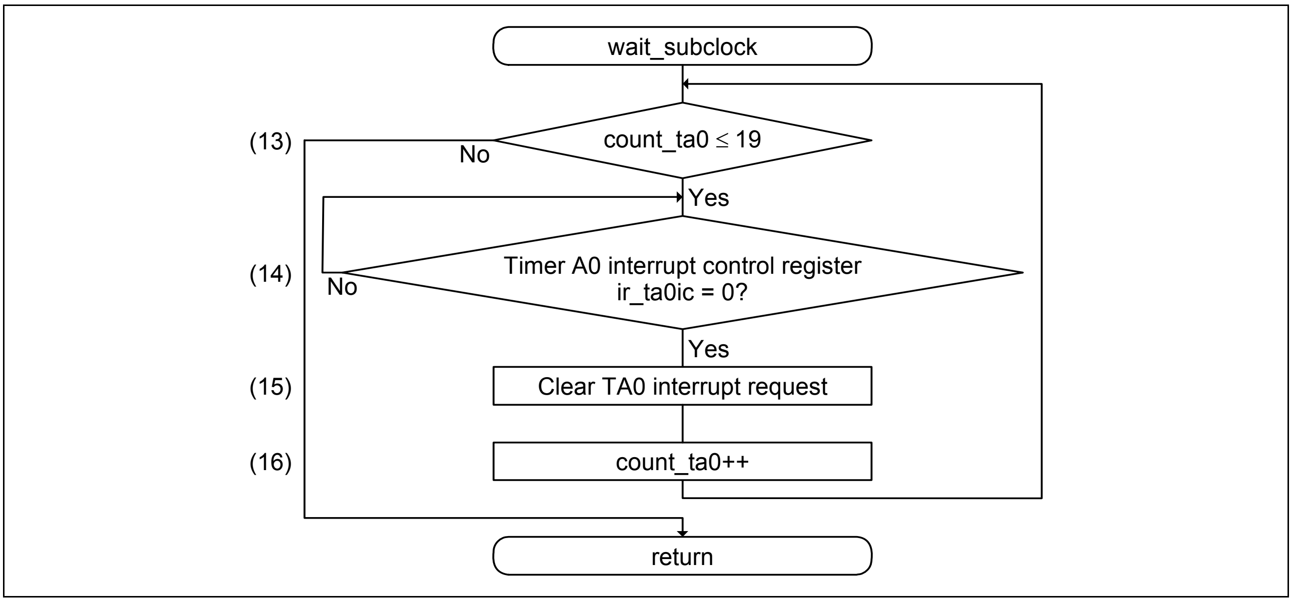


Figure 5.3 Sub Clock Stabilization Wait Function Flowchart

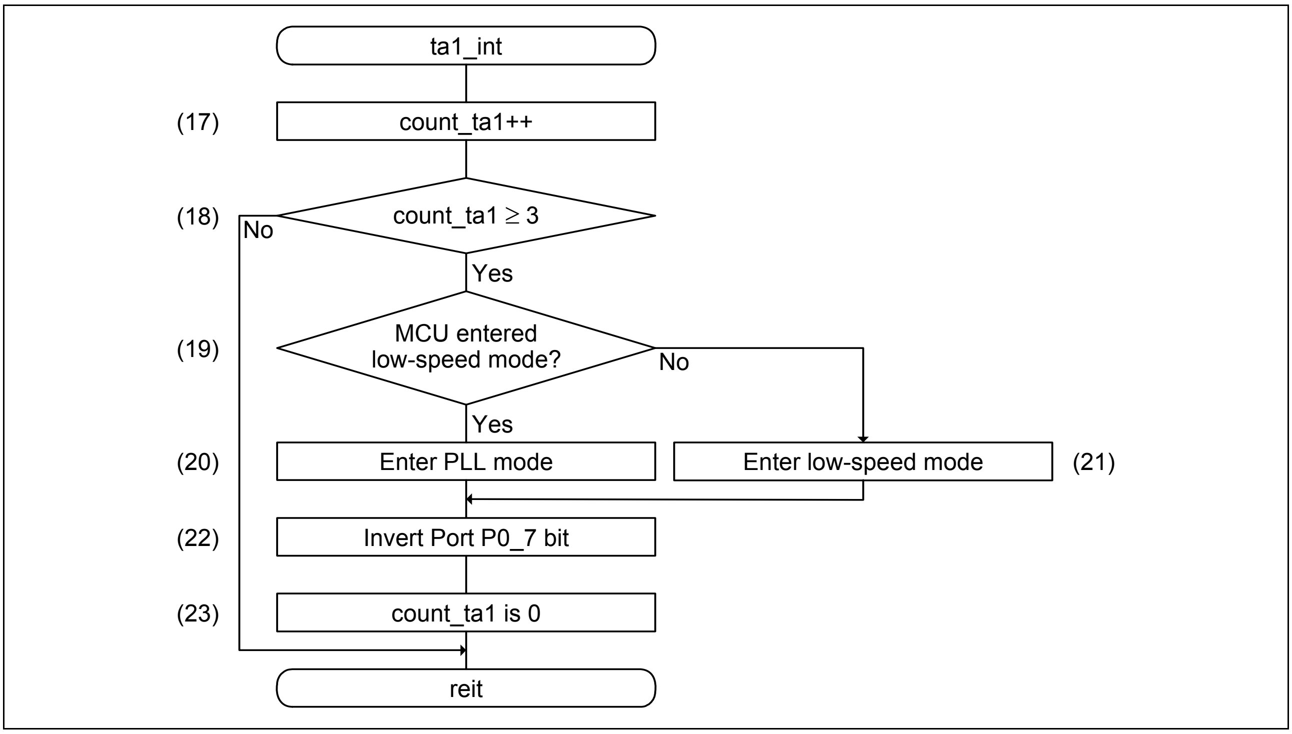


Figure 5.4 Timer A1 Interrupt Function Flowchart

6. Reference Documents

Hardware Manual: R32C/118 Group Hardware Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual: R32C/100 Series C Compiler Ver.1.02 User's Manual Rev. 1.00
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Revision History	Entering Low-speed Mode

Revision	Date	Page	Summary
1.00	Jan. 29, 2010	—	Initial release

Notes regarding these materials