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Renesas Electronics Corporation

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H8SX Series

Enhancement with the Bit-Manipulation Instruction

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

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1. Overview

The H8SX series has an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series. Furthermore, in addition its instruction set has been enhanced to improve CPU performance. The enhancement of the instruction set has greatly improved coding efficiency compared to the conventional series. This coding efficiency leads to benefits such as a reduction in the amount of ROM required to store programs, as well as the shortening of each instruction fetch cycle. This application note describes the "enhancement with the bit-manipulation instruction", which is an enhanced instruction set item.

2. Configuration

The "enhancement with the bit-manipulation instruction" is described below. The conventional H8/300, H8/300H, and H8S series have no dedicated instruction for the assignment of bit-defined variables. With the H8SX series, however, a bit-manipulation instruction is added to enable the efficient assignment of bit-defined variables. For example, to assign the three low-order bits of a bit-defined variable to the three high-order bits of another defined variable with the conventional H8S series, masking and shifting of the variables is necessary, resulting in a large program size and long processing time. The addition of the bit-manipulation instruction means that this operation can be performed with only one instruction.

![Diagram](image)

*Figure 1  Enhancement with the Bit-Manipulation Instruction*
3. Sample Program

3.1 Flowchart

The sample program shown below is very simple, and will allow you to understand the descriptions of "enhancement with the bit-manipulation instruction", an enhanced instruction set item.

As a comparison with the H8S series, the results of compilation are shown. This example is for reference only, because the instruction code length generated in the compilation of an application-level program greatly depends on the source program and compile conditions.

```
Start

Set 4 bits of val1 in 4 bits of val2

Set 6 bits of val1 in 6 bits of val2

End
```

bit_shift
3.2 Program Listing

/**************************************************************/
/* Include File                                                */
/**************************************************************/
#include <machine.h>

/**************************************************************/
/* Function Prototype                                          */
/**************************************************************/
void bit_shift(void);

/***************************************************************/
/* RAM allocation                                              */
/**************************************************************/
struct
{
  unsigned long tmp1 :4;
  unsigned long bit27:1;
  unsigned long bit26:1;
  unsigned long bit25:1;
  unsigned long bit24:1;
  unsigned long bit23:1;
  unsigned long bit22:1;
  unsigned long bit21:1;
  unsigned long bit20:1;
  unsigned long bit19:1;
  unsigned long bit18:1;
  unsigned long bit17:1;
  unsigned long bit16:1;
  unsigned long bit15:1;
  unsigned long bit14:1;
  unsigned long bit13:1;
  unsigned long bit12:1;
  unsigned long bit11:1;
  unsigned long bit10:1;
  unsigned long bit9 :1;
  unsigned long bit8 :1;
  unsigned long bit7 :1;
  unsigned long bit6 :1;
  unsigned long tmp2 :6;
}val1;
struct
{
  unsigned short bit15:1;
  unsigned short bit14:1;
  unsigned short bit13:1;
  unsigned short bit12:1;
  unsigned short bit11:1;
  unsigned short bit10:1;
  unsigned short bit9 :1;
  unsigned short bit8 :1;
  unsigned short bit7 :1;
  unsigned short bit6 :1;
}val2;
3.3 Comparison of the H8S Series with the H8SX Series

The result of compilation (assembly code) with the H8S series is shown below.

```assembly
P
00000000  _bit_shift:          ; section
00000000    STM.L    (ER2-ER3),@-SP
00000004    MOV.L    #_val1,ER3
0000000A    MOV.L    @ER3,ER0
0000000E    AND.L    #-6,ER0
00000014    OR.L    #268435398,ER0
0000001A    MOV.L    ER0,@ER3
0000001E    MOV.W    #4,R1
00000022    JSR    @$BFUL$3:24
00000026    MOV.W    R0,R1
00000028    MOV.L    #_val2,ER0
0000002E    MOV.W    #772,R2
00000032    JSR    @$BFINI$3:24
00000036    mov.B    @(3:16,ER3),R0L
0000003A    AND.B    #63,R0L
0000003C    EXTU.W    R0
0000003E    EXTU.L    ER0
00000040    MOV.W    R0,R1
00000042    MOV.L    #_val2,ER0
00000048    MOV.W    #2054,R2
0000004C    JSR    @$BFINI$3:24
00000050    LDM.L    @SP+,,(ER2-ER3)
00000054    RTS

B
00000000   _val1:          ; section
00000000    .RES.W  2 ; static: val1
00000004   _val2:          ; static: val2
00000004    .RES.W  1

The result of compilation (assembly code) with the H8SX series is shown below.

P
00000000  _bit_shift:          ; section
00000000    PUSH.W  R2
00000002    MOV.B    #15:8,R0L
```

```c
/* Function Definition(Main Program) */
void bit_shift(void)
{
    val1.tmp1 = 0x0F;
    val1.tmp2 = 0x3A;

    val2.tmp3 = val1.tmp1;
    val2.tmp4 = val1.tmp2;
}
```
Enhancement with the Bit-Manipulation Instruction

00000004  BFST   R0L,#240,@_val1:32
0000000C  MOV.B  #58:8,R0L
00000016  BFST   R0L,#63,@_val1+3:32
0000001E  EXTU.L #2,ER0
00000020  MOV.W  R0,R1
00000022  MOV.B  @_val2:32,R0H
00000028  MOV.B  R1L,R0L
0000002A  SHLL.B R0L
0000002C  AND.B  #30:8,R0L
00000030  OR.B   R0L,R0H
00000032  MOV.B  R0H,@_val2:32
00000038  BFLD   #63,@_val1+3:32,R0L
00000040  EXTU.L #2,ER0
00000042  MOV.B  @_val2+1:32,R2H
00000048  MOV.B  R0L,R2L
0000004A  SHLL.B #2,R2L
0000004C  AND.B  #3:8,R2H
0000004E  OR.B   R2L,R2H
00000050  MOV.B  R2H,@_val2+1:32
00000056  POP.W  R2
00000058  RTS

B

00000004  .val1:                  ; section
00000000  .RES.W     2                ; static: val1
00000004  .val2:                  ; static: val2
00000004  .RES.W     1
Table 1 lists the results of compilation with the H8S series, while Table 2 lists the results obtained with the H8SX series.

**Table 1  Results of Compilation (H8S Series)**

<table>
<thead>
<tr>
<th>Instruction Length</th>
<th>H8S series</th>
<th>Instruction</th>
<th>Execution state count</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>In bytes</td>
<td>Total State count</td>
</tr>
<tr>
<td>MOV.L</td>
<td>#_val1,ER3</td>
<td>6</td>
<td>50* 3</td>
</tr>
<tr>
<td>MOV.L</td>
<td>@ER3,ER0</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>AND.L</td>
<td>#6,ER0</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>OR.L</td>
<td>#268435398,ER0</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>MOV.L</td>
<td>ER0,ER3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>MOV.W</td>
<td>#4,R1</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>JSR</td>
<td>@$BFUL$3:24</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>MOV.W</td>
<td>R0,R1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>MOV.L</td>
<td>#_val2,ER0</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>MOV.W</td>
<td>#772,R2</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>JSR</td>
<td>@$BFINIS3:24</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

* The number of size states for the standard library BFUL and BFN2 are not included.

**Table 2  Results of Compilation (H8SX Series)**

<table>
<thead>
<tr>
<th>Instruction Length</th>
<th>H8SX series</th>
<th>Instruction</th>
<th>Execution state count</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>In bytes</td>
<td>Total State count</td>
<td>Total</td>
</tr>
<tr>
<td>BFLD</td>
<td>#240, @_val1:32,R0L</td>
<td>8</td>
<td>34</td>
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<tr>
<td>EXTU.L</td>
<td>#2, ER0</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>MOV.W</td>
<td>R0,R1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>MOV.B</td>
<td>@_val2:32,R0H</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>MOV.B</td>
<td>R1L,R0L</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>SHLL.B</td>
<td>R0L</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>AND.B</td>
<td>#30:8,R0L</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>AND.B</td>
<td>#225:8,R0H</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>OR.B</td>
<td>R0L,R0H</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>MOV.B</td>
<td>R0H, @_val2:32</td>
<td>6</td>
<td>1</td>
</tr>
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</table>
## Revision Record

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<th>Page</th>
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<td>Sept.19.03</td>
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<td>First edition issued</td>
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